THE EFFECTS OF ESR OUTPUT-CAPACITOR ON CCM BUCK AND BOOST CONVERTER BY USING PULSE-TRAIN-CONTROL TECHNIQUE

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***ABSTACT*:**

In this project deals with pulse-train (PT) control technique for Boost and Buck converters. In this PT control of switching dc–dc converters operating in continuous conduction mode (CCM). The PT control technique has been proposed for to improve the transient performance of switching dc-dc converters. The output voltage of converters having ripples to minimize that by connect the equivalent series resistor (ESR) output capacitor. The effect of equivalent series resistor (ESR) output capacitor is to reduce the output voltage ripple. The larger ERS will result in a large output voltage ripple.

Keywords: **Buck&Boost, PTcontrol, ESR**

1. INTRODUCTION

In order to improve the transient performance of switching dc–dc converters, control techniques without error amplifiers and their corresponding compensation networks, such as hysteretic control or constant on-time (COT) control technique are highly preferred. Pulse- train (PT) control technique, has been proposed for switching dc–dc converters. In the PT controller, the output-voltage regulation of switching dc–dc converters is achieved by applying high- or low-power control pulses with preset duty ratios, rather than by adjusting the duty ratio of the control pulse cycle by cycle as the conventional PWM technique does. For PT control, more input power is delivered to the load to increase the output voltage during the high-power control- pulse cycle, and less input power is delivered to the load to decrease the output voltage during the low-power control-pulse cycle. The PT control of switching dc–dc converters operating in discontinuous conduction mode (DCM) is thus quite straightforward, as its input energy is completely delivered to the load in one switching cycle. Therefore, the PT control of switching dc–dc converters operating in DCM has been studied thoroughly and up to now, almost all of the works on PT control are focused on switching dc–dc converters operating in DCM, with few research works reported on the PT control of switching dc–dc converters operating in continuous conduction mode (CCM). However, in high-power applications, DCM operation will cause higher current stress and larger output- voltage ripples

2. PROPOSED CONCEPT:

In order to improve the transient performance of switching dc–dc converters, control techniques without error amplifiers and their corresponding compensation networks, such as hysteretic Control or constant on-time (COT) control technique, are highly preferred.

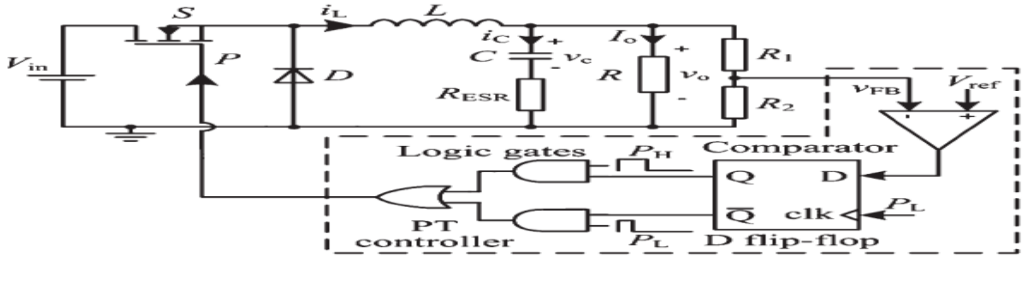


Fig 1 proposed buck converter

In recent years, a novel control technique, called as pulse train (PT) control technique, has been proposed for switching dc–dc converters. Without an error amplifier and its corresponding compensation network, the PT controller is simple to design and benefits from excellent control performance. In the PT controller, the output-voltage regulation of switching dc–dc converters is achieved by applying high- or low-power control pulses with preset duty ratios, rather than by adjusting the duty ratio of the control pulse cycle by cycle as the conventional PWM technique does.

For PT control, more input power is delivered to the load to increase the output voltage during the high-power control pulse cycle, and less input power is delivered to the load to decrease the output voltage during the low-power control-pulse cycle. The PT control of switching dc–dc converters operating in discontinuous conduction mode (DCM) is thus quite straight forward, as its input energy is completely delivered to the load in one switching cycle. Therefore, the PT control of switching dc–dc converters operating in DCM has been studied thoroughly, and up to now, almost all of the works on PT control are focused on switching dc–dc converters operating n DCM, with few research works reported on the PT control of switching dc–dc converters operating in continuous conduction mode (CCM). However, in high-power applications, Cooperation will cause higher current stress and larger output voltage ripples, which restrict the DCM converter to low-power applications. In higher power applications, switching dc–dc converters operating in CCM are preferred and required.

It is known that for PT-controlled CCM buck converters, the inductor currents at the beginning and end of each switching cycle are not the same, which means that the inductor stores or releases energy in each switching cycle. Thus, the control performance of PT-controlled CCM buck converters is quite different from that of PT-controlled DCM buck converters, and the PT control of CCM buck converters is more complicated.

In this paper, a PT-controlled buck converter operating in CCM is studied, and an undesired low-frequency oscillation phenomenon is found. PT control is essentially a ripple-based control, as reported in and the output-capacitor equivalent series resistance (ESR) greatly affects the control performances of the converters. The effect of the ESR output capacitor on the low-frequency oscillation of PT-controlled buck converters is analyzed. An inductor-current ripple injection feedback circuit is adopted to eliminate the low-frequency oscillation. The studies presented in this paper give a useful guideline for the design of PT-controlled CCM buck converters.

However, as discussed below, for PT-controlled CCM buck converters, the inductor will store or release energy in each switching cycle, which makes the control performance of PT-controlled CCM buck converters quite different from that of PT-controlled DCM buck converters.

2.1 Review of PT Control Technique

Pulse train control is nothing but to get continuous train of pulses with different duty ratios but same frequency.

Here two pulses are need one is high power control pulse (P_H) and low power control pulse (P_L). The P_H *and* P_L pulses are depends upon the V_{ref} value.

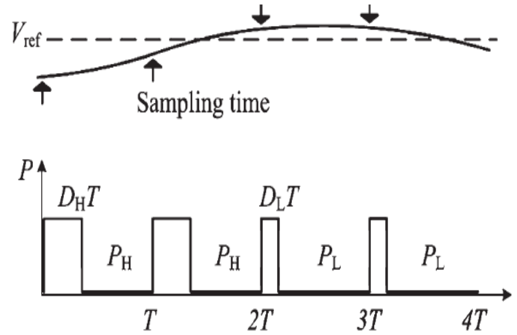


Fig. 2 Desired operation waveforms of the PT-controlled buck converter.

Fig.2 shows the PT-controlled buck converter, where $R_{ESR}$is the ESR of the output capacitor and $P_H$and $P_L$are presethigh- and low-power control pulses with the same frequency butdifferent duty ratios, which can be generated by digital chips or analog circuits. It can be known from Fig. 1 that the PT controller is simple, with only a comparator and a few logic devices.

Fig.2 shows the desired operation waveforms of the PT-controlled buck converter. Its operation principle can be depicted as follows. At the beginning of each switching cycle, the output voltage $V_O$is sampled and compared with the reference voltage V_{ref} to determine whether $P_H$or $P_L$should be selectedas active control pulse. When the feedback voltage V_{fb} is lower than V_{ref},$P_H$is selected to increase V_O; otherwise, $P_L$is chosento decrease V_O.

For PT-controlled DCM buck converters, at the beginning and end of each switching cycle, the energy variation in the inductor is zero, i.e., the inductor does not store or release any energy in each switching cycle. Thus, the input energy in one switching cycle is completely delivered to the load .When $P_H$is applied, the input energy is larger than the energy consumed by the load, and the excess input energy charges the output capacitor to make the output voltage increase. On the other hand, when P_L is applied, the input energy is less than the energy consumed by the load, and the output capacitor is discharged to provide energy to the load, which makes the output voltage decrease. It is easy to know that the desired operation waveforms shown in Fig. 2 can be ensured. Therefore the output voltage of the PT-controlled DCM buck converter can be well regulated.

However, as discussed below, for PT-controlled CCM buck converters, the inductor will store or release energy in each switching cycle, which makes the control performance of PT-controlled CCM buck converters quite different from that of PT-controlled DCM buck converters.

Fig.3 shows three different PWM signals. Fig.3 shows a PWM output at a 10% duty cycle. That is, the signal is on for 10% of the period and off the other 90%. Below fig.3 shows PWM outputs at 50% and 90% duty cycles, respectively. These three PWM outputs encode three different analogue signal values, at 10%, 50%, and 90% of the full strength. If, for example, the supply is 9V and the duty cycle is 10%, a 0.9V analog signal results.

Normal PWM involves starting a counter which counts up to its maximum value and then reverses, counts back to zero and then repeats. This can be visualized as a saw tooth waveforms shown in Fig.4

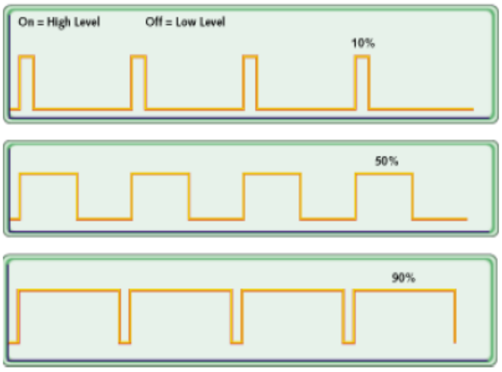


Fig 3 PWM signals of varying duty cycles

In order to create output pulses whose mark: space ratio changes the output compare register (Ref) is loaded with a value so that when the count reaches that value the Output is reversed.

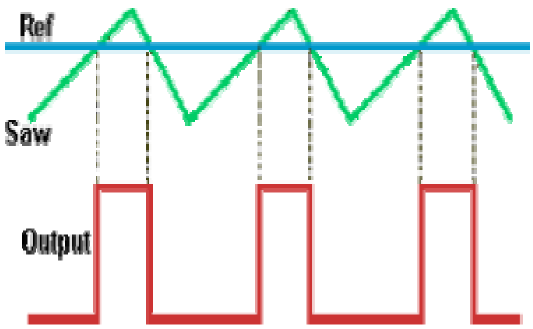


Fig 4 saw tooth waveforms

As the value of Ref reduces so the width of the pulses increase and as Ref increase then the width of the pulses will decrease.

2.3 Analysis of Output-Voltage Variation with P_H *and* P_L pulses applied

It is well known that for buck converters, the output-voltage variation from the beginning to the end of one switching cycle is made up of two terms, the voltage variation across the output capacitor and its ESR, i.e. the output-voltage variation in the n^{th} switching cycle can be given as

Output voltage across the ESR output capacitor is

$$V_O = V_C + V_{ESR} \qquad 2.1$$

Change in voltage is

$$\Delta V_O = \Delta V_C + \Delta V_{ESR} \qquad 2.2$$

The output-voltage variation in the n^{th} switching cycle can be given as

$$\Delta V_O(nT) = \Delta V_C(nT) + \Delta V_{ESR}(nT) \qquad 2.3$$

$$V_L = L\frac{di_L}{dt} \qquad 2.4$$

$$I_C = C\frac{dv_C}{dt} \qquad 2.5$$

From above equation v_C can be written as

$$V_C = \frac{1}{C}\int I_C dt \qquad 2.6$$

Here,

$$I_C = i_L - I_O$$

V_C Valve is substitute in above equation that becomes

$$\Delta V_O(nT) = \frac{1}{C}\int_{(n-1)T}^{nT}(i_L - I_O)\,dt + \Delta i_L(nT)R_{ESR}$$
2.7

The corresponding voltage variations in then^{th} switching cycle

$$\Delta V_O(nT) = V_O(nT) - V_O[(n-1)T] \qquad 2.8$$

$$\Delta V_C(nT) = V_C(nT) - V_C[(n-1)T] \qquad 2.9$$

$$\Delta V_{ESR}(nT) = V_{ESR}(nT) - V_{ESR}[(n-1)T] \; 2.10$$

Inductor-current variation in the n^{th} switching cycle

$$\Delta i_L(nT) = i_L(nT) - i_L[(n-1)T] \qquad 2.11$$

Substituting V_L valve that becomes

$$V_L = V_{in}DT - V_O T$$

$$V_L = (V_{in}D - V_O)T \qquad 2.12$$

We know that $V_L$is

$$V_L = L\frac{di_L}{dt}$$

$$\frac{di_L}{dt} = \frac{V_L}{L} \qquad 2.13$$

P_H *and* P_L are applied corresponding as

$$\therefore \Delta i_L(nT) = \frac{(V_{in}D - V_O)}{L}T \qquad 2.14$$

When the P_H is applied to

$$\Delta i_L(nT) = \frac{(V_{in}D_H - V_O)}{L}T \qquad 2.15$$

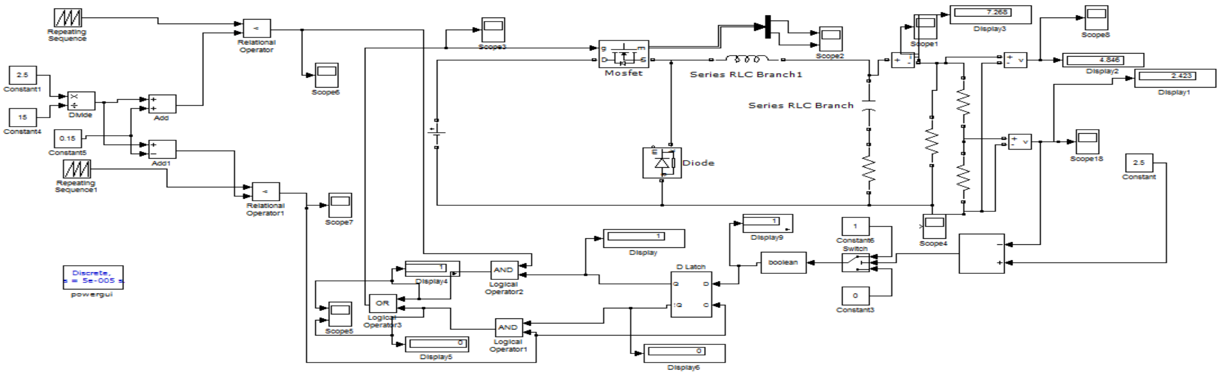
When the P_L is applied to

$$\Delta i_L(nT) = \frac{(V_{in}D_L - V_O)}{L}T \qquad 2.16$$

Where V_O is the dc output voltage and D_H and D_L are the corresponding duty ratios of P_H and P_L, respectively. In the design of the PT-controlled CCM buck converter, D_H and D_L should be chosen to satisfy $V_{in}D_L < V_O < V_{in}D_H$. Thus it can be known that when P_H is applied $\Delta I_L(nT) > 0$, and when P_L is applied $\Delta I_L(nT) < 0$, which means that theinductor will store energy when P_H is applied and release energy when P_L is applied, i.e., the inductor participates in energy delivery, which makes the control more complicated.

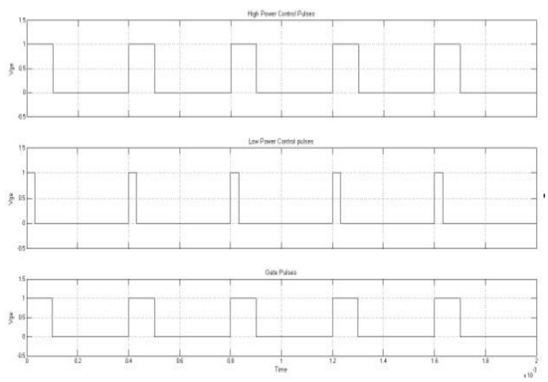
3. SIMULATION RESULTS

3.1 Simulation diagram of proposed buck converter

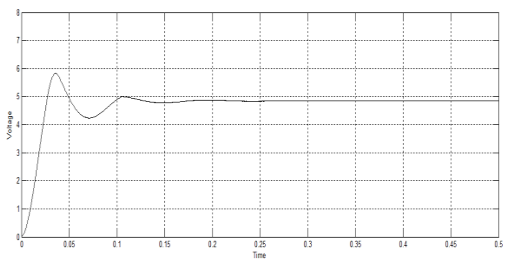


The above simulation diagram P_H *and* P_L are the high and low power control pulses. If output voltage value is greater than the reference value then the P_L is ON state and P_H is OFF state. When the output voltage less than reference voltage then P_H is ON state and P_L is OFF state. The equivalent series resistor (ESR) values are 6mΩ and 20mΩ. the reference value is 2.5v and the average output voltage value is 2.47v.

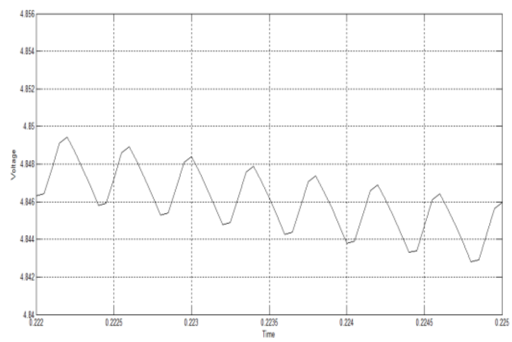
3.2 PT control pulses for buck converter



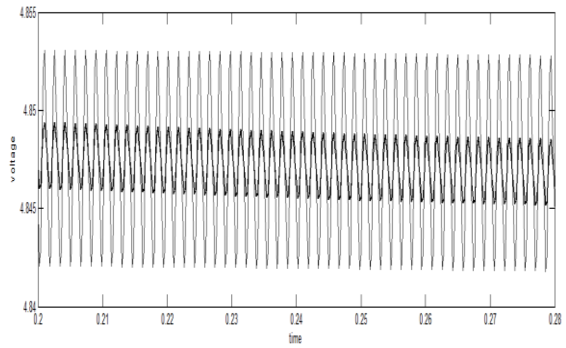
Output voltage waveforms at ERS is 6mΩ



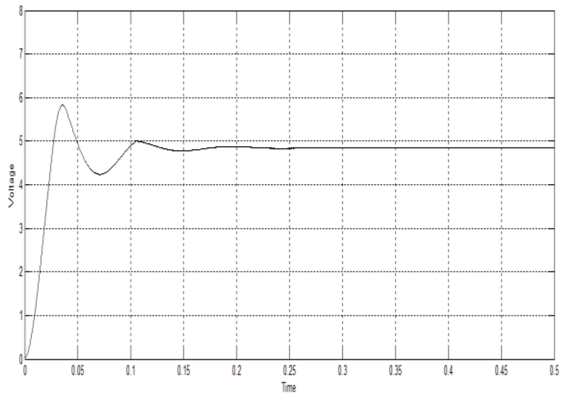
Output voltage ripple analyzed waveforms ERS is 6mΩ



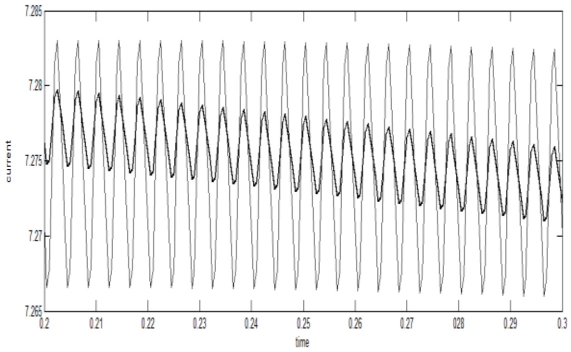
Output voltage waveforms ESR values at 20mΩ and 6mΩ



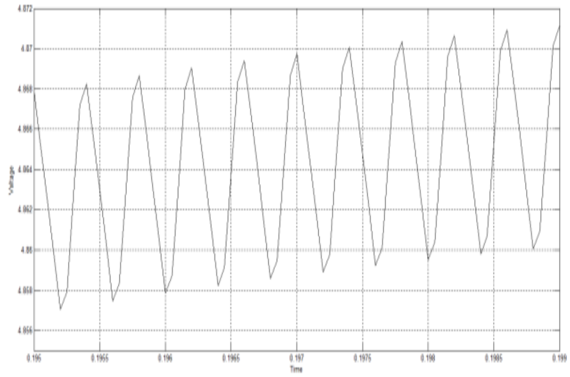
Output voltage waveforms ESR at 20mΩ



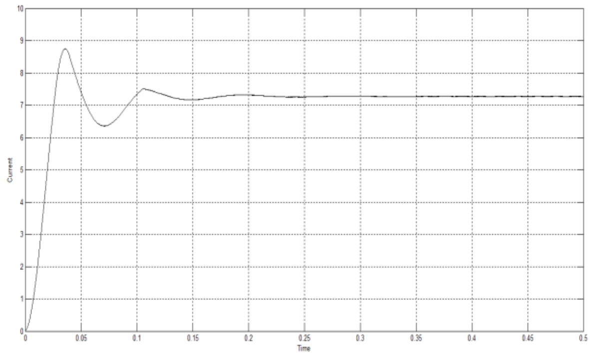
Output current waveforms ERS values at 20mΩ and 6mΩ



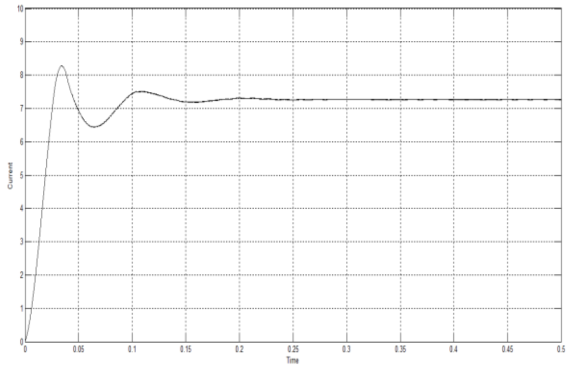
Output voltage ripple analyzed waveforms ESR at 20mΩ



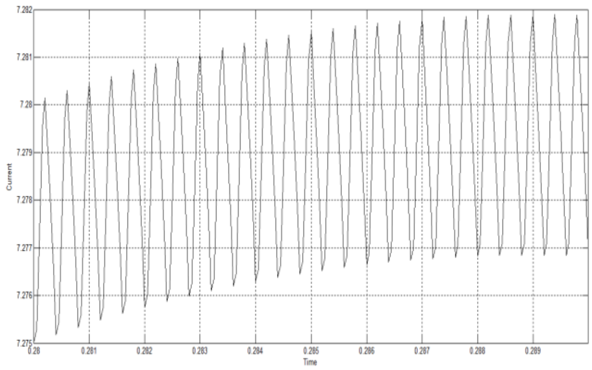
Output current waveforms ESR at 6mΩ



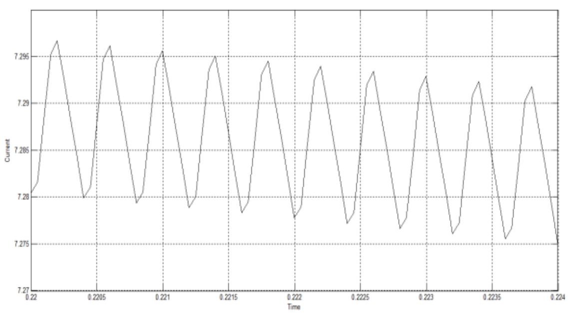
Output current waveforms ESR at 20mΩ



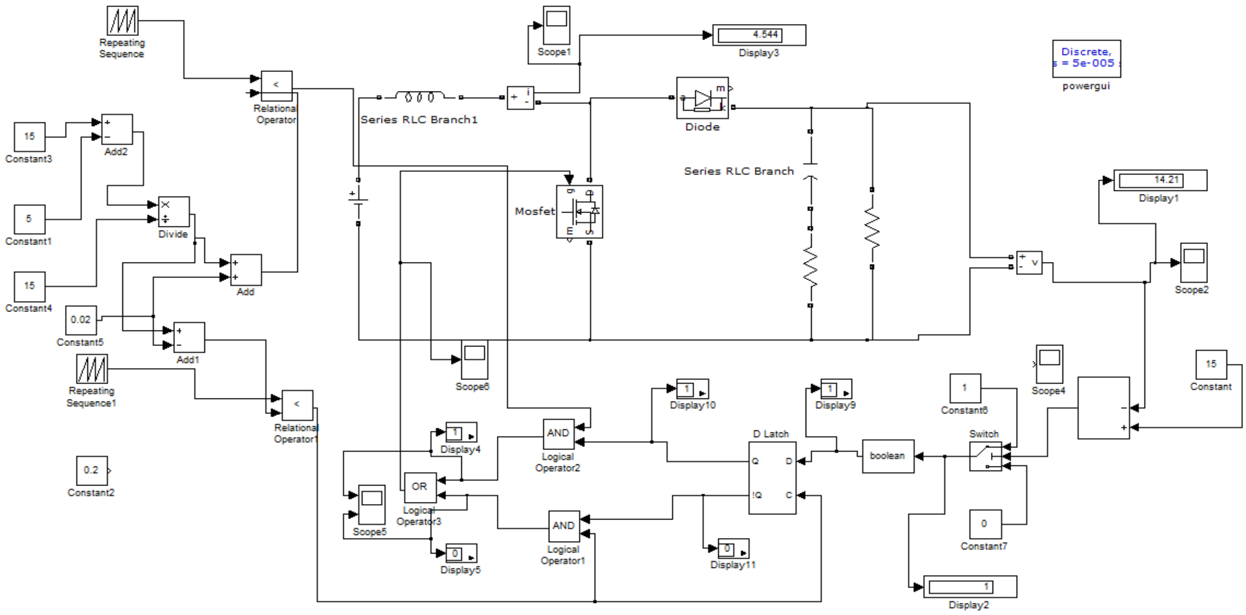
Output current ripple analyzed waveforms ESR at 6mΩ



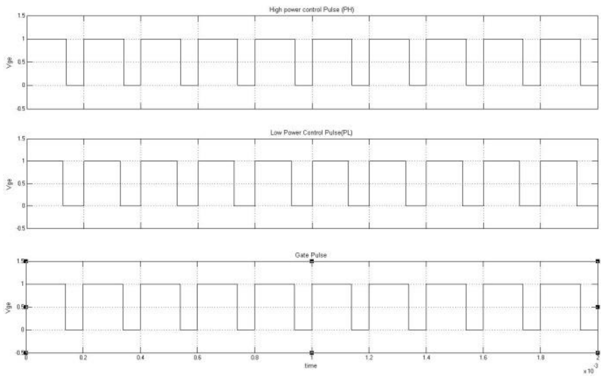
Output current ripple analyzed waveforms ESR at 20mΩ



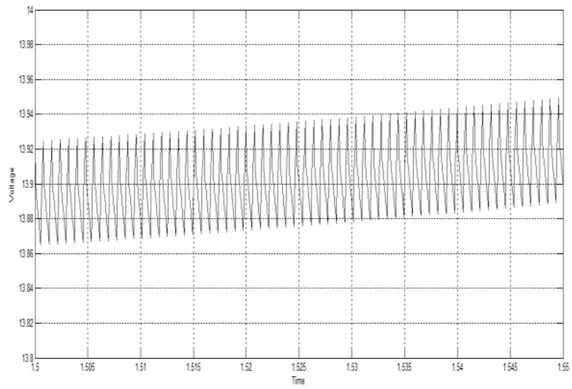
3.3 Simulation diagram of proposed boost converter



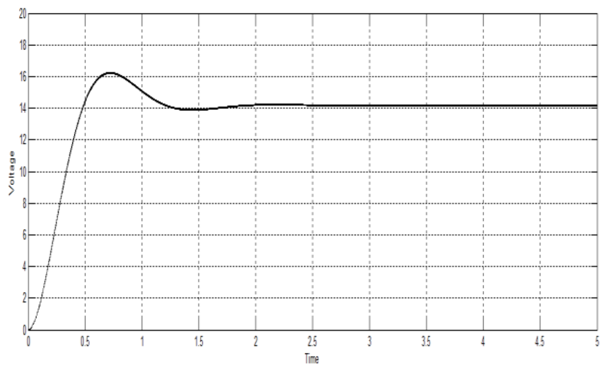
3.4 PT control pulses for boost converter



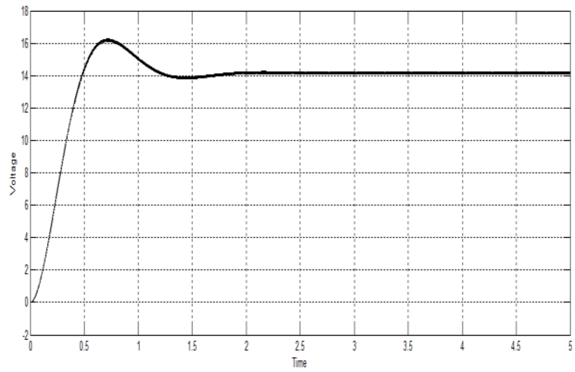
Output voltage ripple analyzed waveforms ESR at 6mΩ



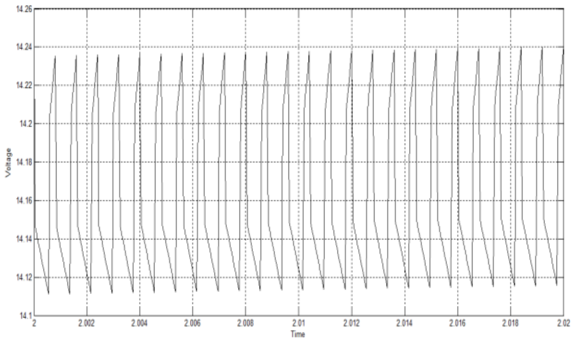
Output voltage waveforms ESR at 6mΩ



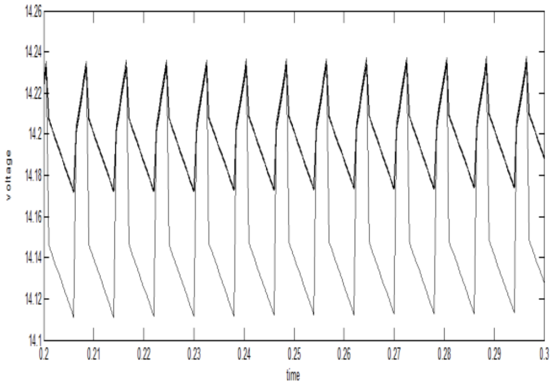
Output voltage waveforms ESR at 20mΩ



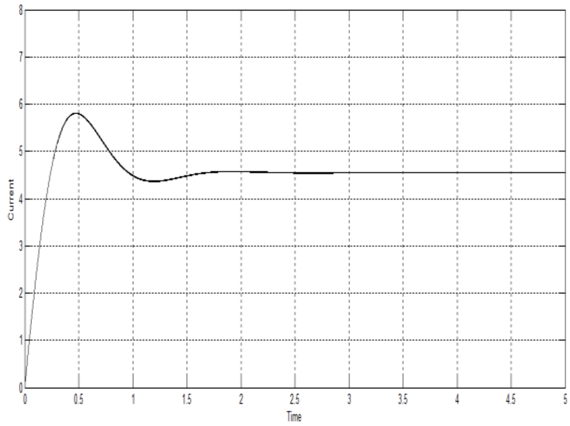
Output voltage ripple analyzed waveform ESR at 20mΩ



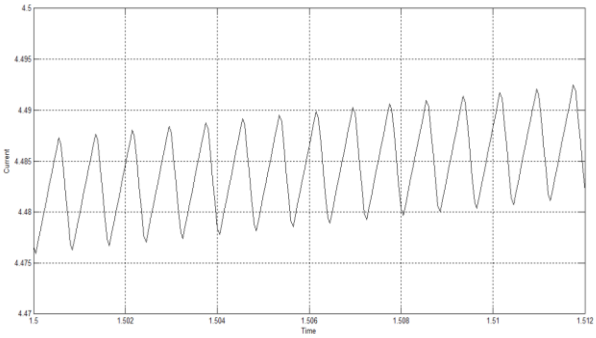
Output voltage waveforms ESR values at 20mΩ and 6mΩ



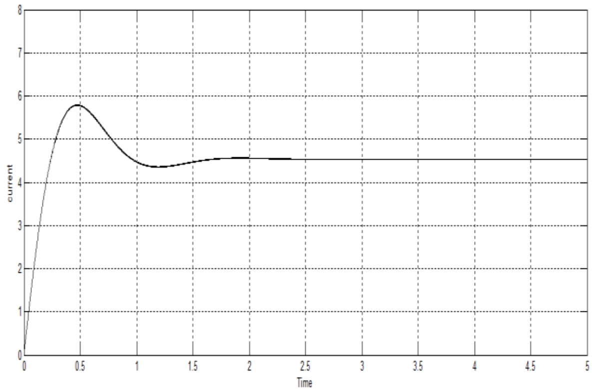
Output current waveforms ESR at 6mΩ



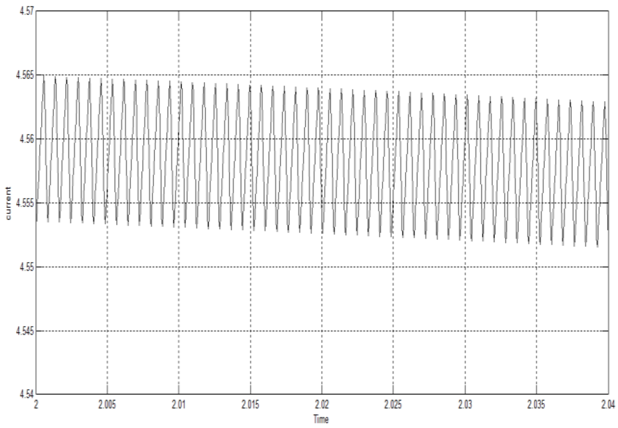
Output current ripple analyzed waveforms ESR at 6mΩ



Output current waveform ESR at 20mΩ



Output current ripple analyzed waveforms ESR at 20mΩ



CONCLUSION

PT-control technique for CCM Buck and Boost converter has done. The effect of ESR output capacitor on the oscillations has been analyzed. It has been found that the oscillation will happen when the ESR output capacitor is small and disappear when ESR output capacitor is large. finally output voltage and current waveforms are analyzed.

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