Phase shifted carrier PWM control technique of a series parallel switched multilevel dc-link inverter topology

$B.Ramakrishna\ singh^{\#1}$, $Y.Kusumalatha^{*2}$
#,* Department of Electrical and Electronics Engineering,
#,* Lakkireddy Balireddy College of Engineering, Mylavaram; Krishna (Dt); A.P, India.

Abstract- The use of multilevel inverter (MLI) appears to experience an increasing trend in view of the extensive automation in industries. A good number of MLI topologies are in use over the past four decades. The variable voltage and frequency requirements emphasize the need and elaborate the increasing trend of using multilevel inverters (MLI) in modern drives and utility applications. The multilevel inverter [MLI] is a promising inverter topology for high voltage and high power applications. This inverter synthesizes several different levels of DC voltages to produce a stepped AC output that approaches the pure sine waveform. The conventional MLI requires more number of switches as the level increases and also switching losses and cost also increases. In order to address the above concerns, this paper presents a new series parallel switched multilevel dc-link inverter (SPMLDCLI) topology with reduced number of switches for a particular voltage level. By appropriately choosing a ratio for the voltage sources (V0: Vn) and connecting them in series/parallel, a particular level in the output voltage is generated and hence the name SPSMLDCLI. Finally the proposed technology is verified by using MATLAB/SIMULINK software and the corresponding results are presented.

***Keywords*—Dc link inverter, multilevel, phase shift carrier PWM.**

I.INTRODUCTION

Multilevel Converters are a very interesting solution for medium and high voltage applications. Because of its characteristic of synthesize a sinusoidal voltage on several DC levels. The better topology for power quality and transmission systems applications is the cascade multilevel inverters [1, 2]. However, this topology presents a problem that consists in the use of several DC sources. In the last years multilevel inverters have had a great relevance in transmission and distribution systems, due to its general structure which synthesizes a sinusoidal voltage in many voltages levels. There are a host of MLI topologies that continue to receive great attention and each inherit their own merits based on count of switches, capacitors, diodes and the number of output levels produced from a fixed number of sources [3,4]. The emergence of a new class of MLIs based on a multilevel dc-link (MLDCL) and a bridge inverter to reduce the number of switches, clamping diodes or capacitors appears to be a breakthrough in multilevel power conversion applications [5]. The MLDCLI can be formed by connecting a MLDCL which provides a dc voltage with the shape of approximating the rectified shape of a dictated sinusoidal wave, with or without pulse width modulation, to the bridge inverter, which in turn alternates the polarity to produce an ac voltage. These inverters significantly reduce the number of switches and gate drivers as the number of voltage level increases. However, these structures do not entail a satisfactory operation with unequal voltage sources. It thus perpetuates the need for better structures with the ability to produce still higher number of levels using unequal voltage sources and further component reduction. The cascaded MLI with different voltages [6] in the dc buses of each H-bridge cell envisions the next in line called the hybrid multilevel power inverter. It is possible to synthesize more levels than that with a symmetric topology [7] if the voltage level of each dc bus is properly chosen with the same number of switches. Among the asymmetric multilevel inverters, cascaded multilevel H-bridge inverter with different dc voltage sources is particularly attractive as it is free from capacitor voltage balancing but the power devices are subjected to unequal voltage stress [8, 9]. Multilevel topologies using bulk capacitors as a medium to synthesize voltage levels lead to unbalanced voltage levels [10]. It augurs the need for an adequate control or modulation strategy to balance the voltage in the different capacitors of each topology. It prevents the usage of existing control strategies of MLIs and an alternate solution of innovative topologies that eliminate the capacitor based voltage media. Multilevel inverter technology has gained significance in the area of medium- voltage energy control as well. The number of achievable voltage levels is limited not only due to voltage unbalance hut also due to voltage clamping requirement. circuit layout and packaging constraints. It is general1 preferable to use a suitable control strategy than to opt for higher-level inverter topology to achieve a better quality of output. Therefore three types of low frequency regular sampled PWM strategies based on an a equalization approach suitable for multilevel inverter are preferred. Which guarantee lower THD with equal number of switching and enable easy digital implementation. The performance of this SPMLDCLI is investigated through MATLAB based simulation over a range of viable modulation indices.

2. PROPOSED TOPOLOGY

The generalized structure of the proposed SPSMLDCLI topology contains voltage sources in the ratio Vo:Vn = 1:3, switches and a diode along with a H-bridge, that offers a minimum of fifteen levels is shown in Fig. 1. While the switches Sa, Sb, Sc, Sa1, Sb1, Sc1, San, Sbn and Scn form the dc-link circuit, the switches S1, S2, S3 and S4 constitute the H-bridge inverter. The part of the circuit enclosed between the dotted lines acts as the parent cell and is the obligatory structure in the dc-link part. The structure external to the parent cell is named as a teen cell and every addition of a teen

cell gives way to raise six levels and there by avails the benefit to extend to the desired level. The modes of operation of the basic fifteen levels SPSMLDCLI are explained with V0:V1:V2 = 1:3:3 to elicit the complete working of the power module.

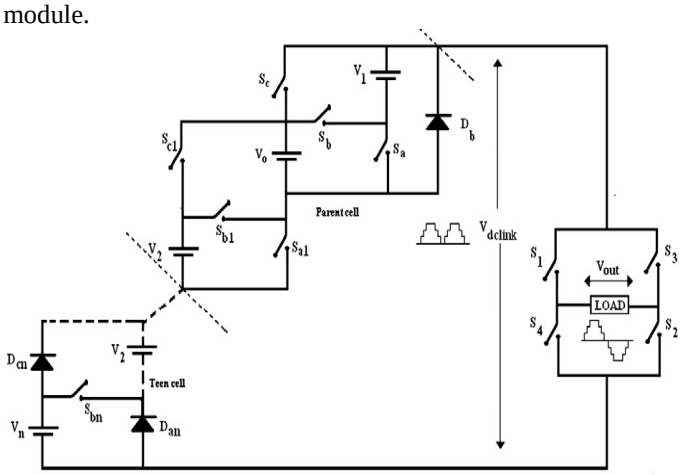

Fig. 1. Generalized structure of SPSMLDCLI.

The switches S1, S2 and S3, S4 in the H-bridge are turned on alternatively, while both Sa1 and Sc in the dc-link part are allowed to conduct to arrive at the first level of voltage as seen in Fig. 2.

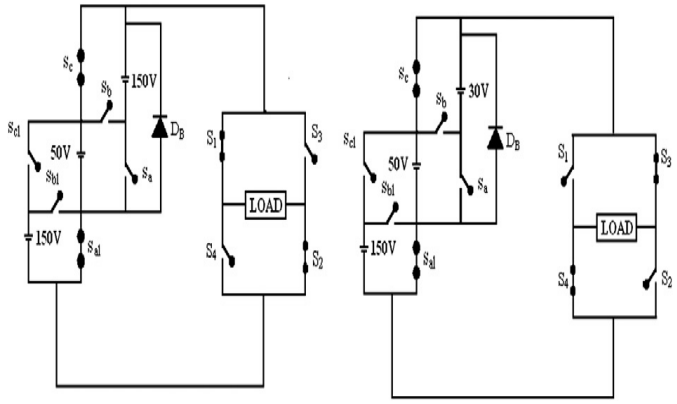

Fig. 2. SPSMLDCLI operating mode-level 1(±50 V).

In addition to the H-bridge, when the switch Sc1 in the dc link conducts, the topology lands at the second level as observed from Fig. 3.

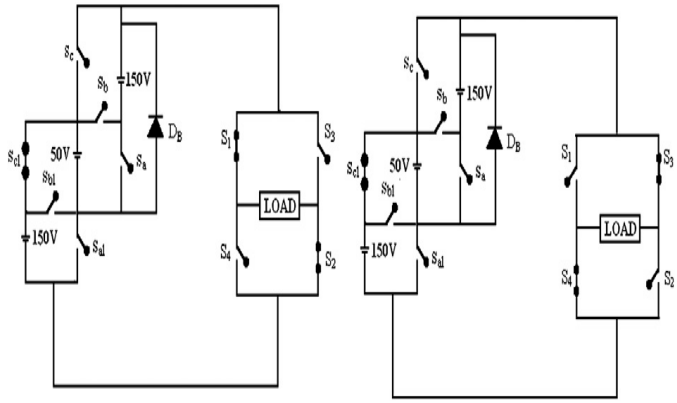

Fig. 3. SPSMLDCLI operating mode-level 2(±100 V).

The mode diagrams for the subsequent levels are shown in Figs. 4–8.

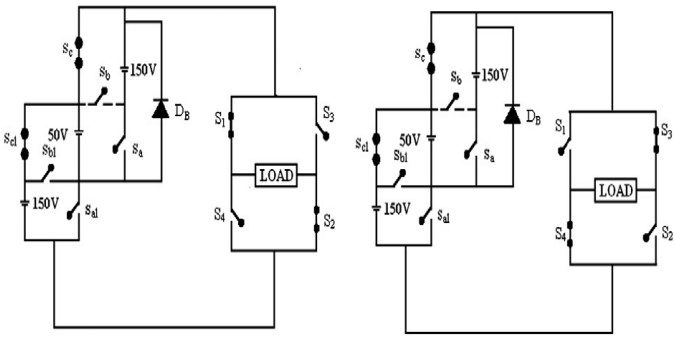

Fig. 4. SPSMLDCLI operating mode-level 3(±150 V).

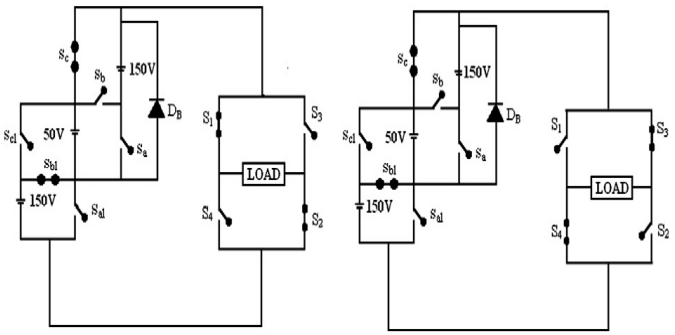

Fig. 5. SPSMLDCLI operating mode-level 4(±200 V).

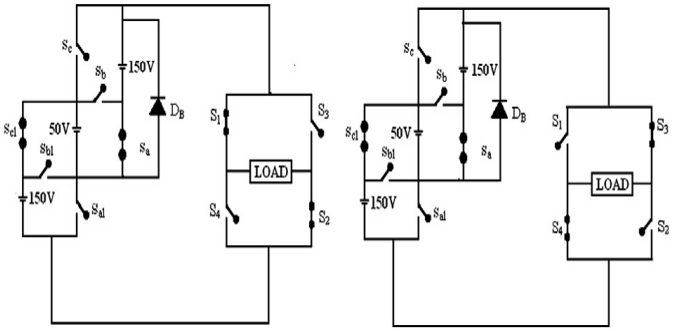

Fig. 6. SPSMLDCLI operating mode-level 5(±250 V).

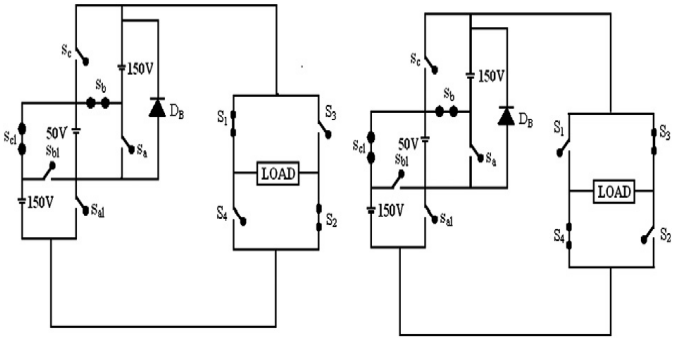

Fig. 7. SPSMLDCLI operating mode-level 6(±300 V).

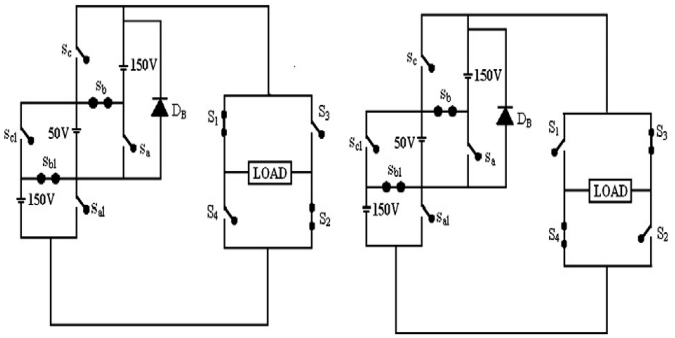

Fig. 8. SPSMLDCLI operating mode-level 7(±350 V).

Accordingly the status of the switches are pictured for the remaining levels and the sequence for synthesizing different voltage levels in the fifteen level SPSMLDCI is summarized in Table 1.

Table 1: Switching sequence for 15 level.

Voltage level	Switches										
	S_a	S_b	S_c	S_{a1}	S_{b1}	S_{c1}	D_B	S_1	S_3	S_2	S_4
+7		√			√			√		√	
+6		√				√		√		√	
+5	√					√		√		√	
+4			√		√		√	√		√	
+3			√			√		√		√	
+2						√	√	√		√	
+1			√	√				√		√	
0				√			√	√	√	√	√
-1			√	√					√		√
-2						√	√		√		√
-3			√			√			√		√
-4			√		√		√		√		√
-5	√					√			√		√
-6		√				√			√		√
-7		√			√				√		√

The entries in Table 2 compare the switch and source requirements for the fifteen level topology with the existing MLI topologies to highlight the reduction in the count.

Table 2: Comparison between topologies for 15 level.

Multilevel inverter structure	Cascaded H-bridge	Diode clamped	Flying capacitor	Multilevel dc-link inverter			Proposed
				Cascaded half bridge	Diode clamped	Flying capacitor	
Main switches	28	28	28	18	18	18	10
Bypass diodes	-	-	-	-	-	-	1
Clamping diodes	-	24	-	-	12	-	-
DC split capacitors	-	6	6	-	6	6	-
Clamping capacitors	-	-	12	-	-	6	-
DC sources	7	1	1	7	1	1	3
Total	35	59	47	25	37	31	14

It is evident from the Table 2 that the number of power devices required is only ten which is 76% less when compared with the basic MLI topologies and 44% with MLDCLIs. It is equally significant to note that the difference in the total component count stands at forty-five when it is compared with a similar conventional case. The precise number of levels of output voltage that a SPSMLDCLI can synthesize is expressed using a relation (2 (3n+1)) where n is the number of voltage sources excluding V0, if arranged in the ratio V0: Vn = 1:3. The available power switches where a simple switch and an anti parallel diode are patched to permit regeneration experience a specific phenomenon of inter-looping and consequently create two circulating current paths as indicated with different colours in Fig. 9.

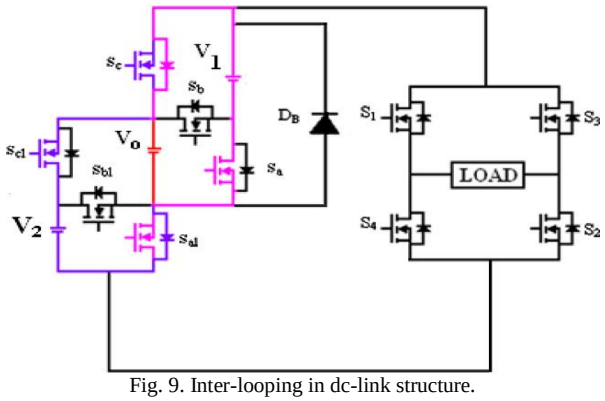

Fig. 9. Inter-looping in dc-link structure.

It may lead to a possible distortion in the output voltage and deviate away from the ideal waveform. The problem can however be eliminated by replacing the switches with IGBT switches as shown in figure 10.

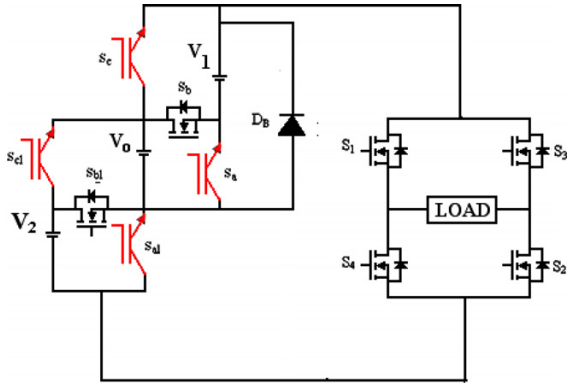

Fig. 10. Eliminating inter-looping with IGBTs.

IV. RESULTS AND DISCUSSION

Case (i): proposed MLI without PWM technique:

The following figure 11 shows the matlab/simulink diagram of the proposed SPSMLDCLI with generic switches without pwm technique.

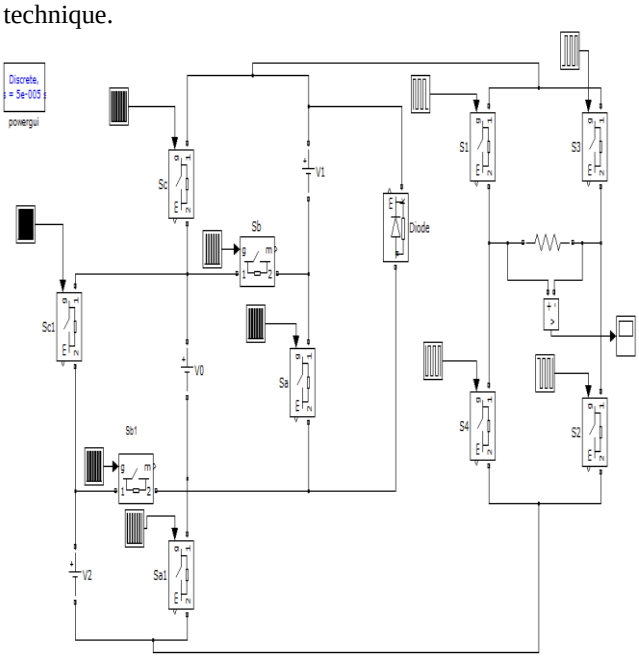

Fig 11: mat lab/Simulink diagram of the proposed SPSMLDCLI with generic switches

The following figure 12 shows the output voltage of proposed SPSMLDCLI, which has fifteen levels.

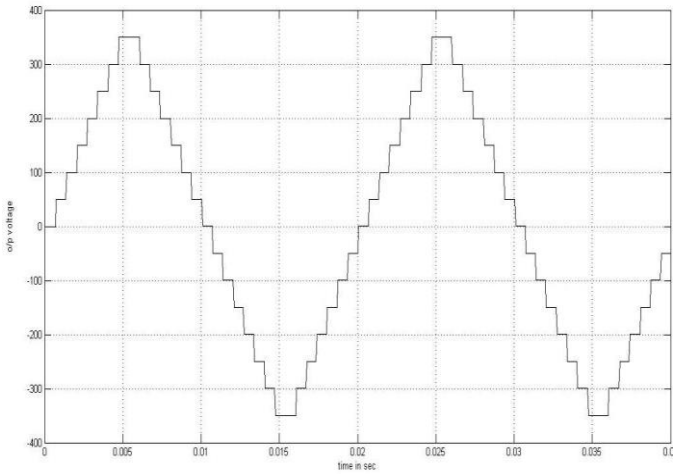

Fig 12 : output voltage waveform of proposed fifteen level without PWM Technique

The above figure contains positive output voltage magnitude having (+1 to +7) levels as indicated in the modes of operation and switching sequence table, and negative output voltage magnitude having (-1 to -7) levels with respect to the time. Zero level is also including in the fifteen levels which can be operated as shown in the switching sequence of the fifteen level multilevel inverter table. The following figure 13 and 14 shows the switching signals and harmonic spectrum for the proposed inverter.

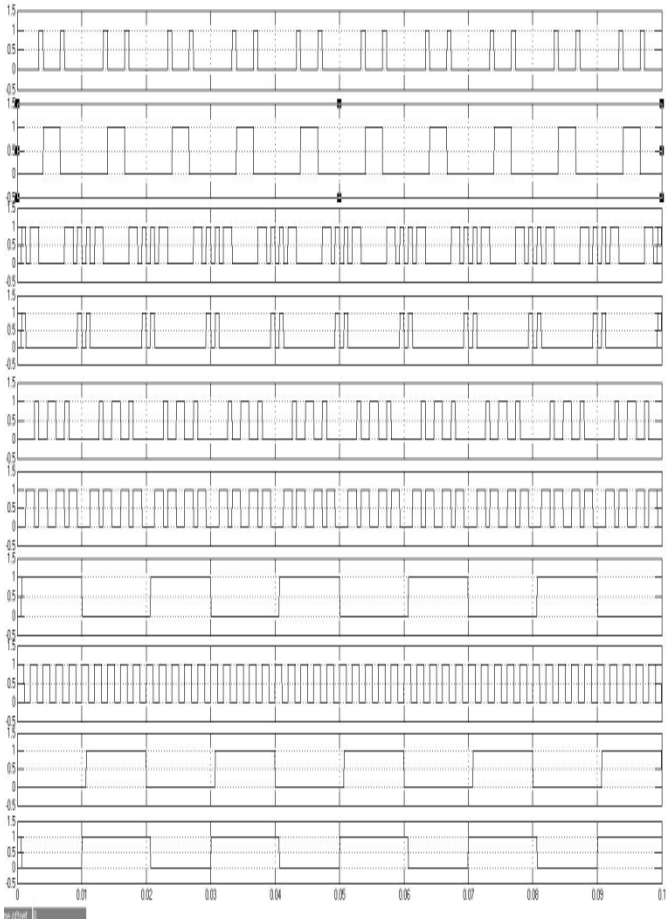

Fig 13: switching signals for the proposed inverter

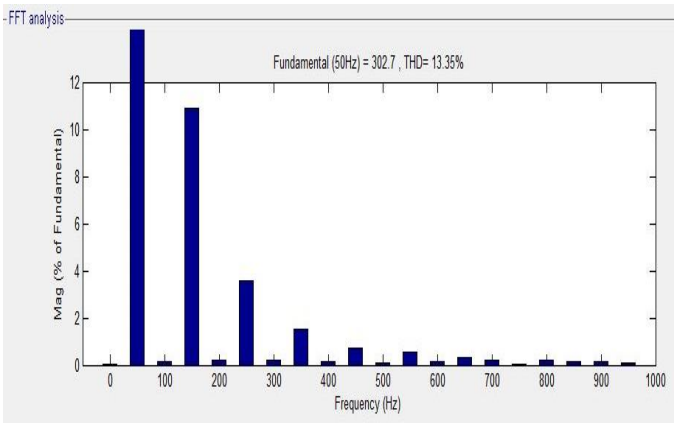

Fig 14: THD of the proposed inverter without PWM technique

As shown in the above figure THD of the output waveform is 13.35% and order of the harmonic content is third order. Lower order harmonics are much complicated to reduce. In order to reduce harmonic content of the in the output waveform we must increase the harmonic order due to higher order harmonics are easily reduced. In case of any PWM technique can be applied to the Multi level inverter we get reduced harmonic content Output voltage waveform and reduced Total Harmonic distortion (THD) of the Multi level Inverter. From the fig 14 the THD content of the output voltage waveform is 13.36%.

Case (ii): proposed MLI with phase shifted carrier PWM technique:

The Simulink model of the proposed converter for implementing carrier phase shift PWM technique is shown in the Fig. 15

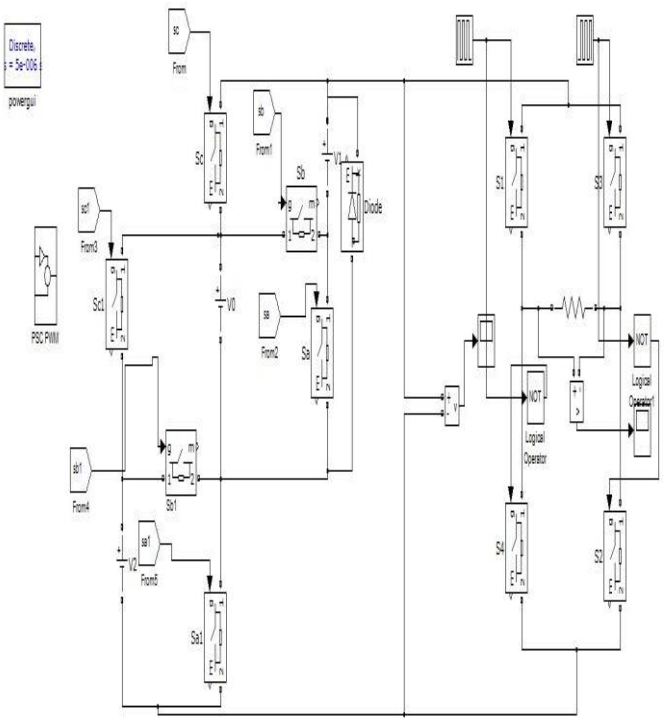

Fig. 15 Simulink model of the Proposed Converter using Phase shifted PWM technique

In Phase Shifted PWM, all the triangular carriers have the same frequency and same peak-peak amplitude .but there is a phase shift between any two adjacent carrier waves. For m Voltage levels (m-1) carrier signals are required and they are phase shifted with an angle of θ= (360°/m-1). The gate signals are generated with proper comparison of carrier wave and modulating signal. In case of phase shift PWM technique, the carriers are horizontally displaced. This introduces a new parameter θ (phase shift angle) for controlling the output voltage. The output voltage is found to be greatly dependent on the phase shift angle. The performance of the inverter can be enhanced by carrier phase shift PWM technique. The following figure 16 and 17 shows matlab implementation and corresponding switching signals of phase shifted carrier PWM technique.

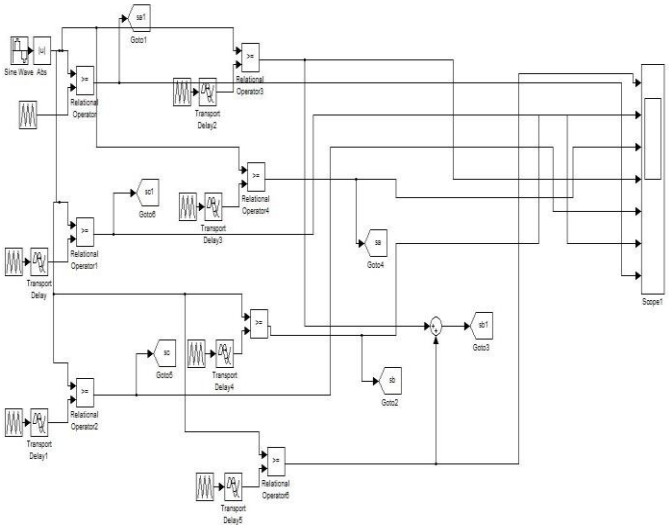

Fig 16: Switching model of the Phase Shifted PWM Simulink model (sub block)

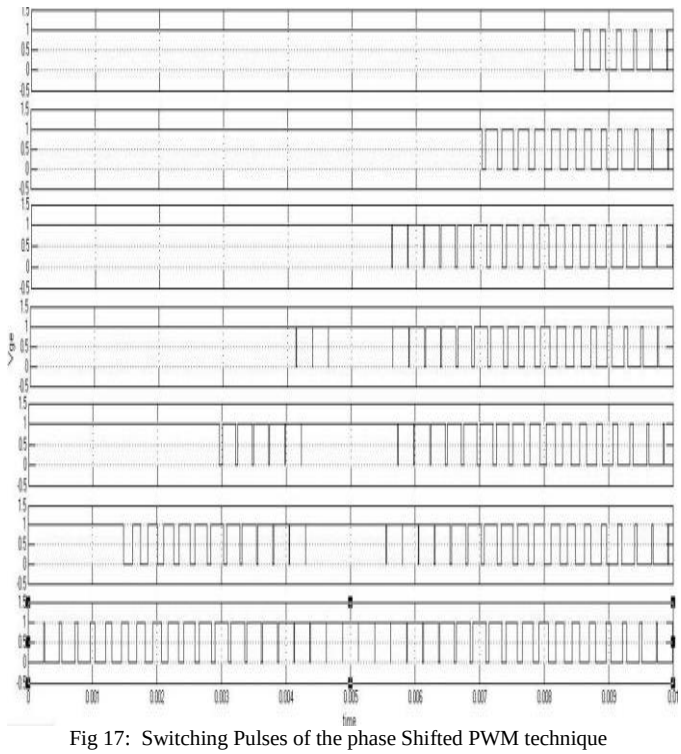

Fig 17: Switching Pulses of the phase Shifted PWM technique

The following figure 18 and 19 shows the output voltage waveform of the proposed MLI with phase shifted carrier PWM technique waveform e and harmonic spectrum analysis. From the figure 19, the THD content of the output voltage waveform is 7.73%. From the above results as the inverter is controlled by the PWM technique THD content decreases drastically.

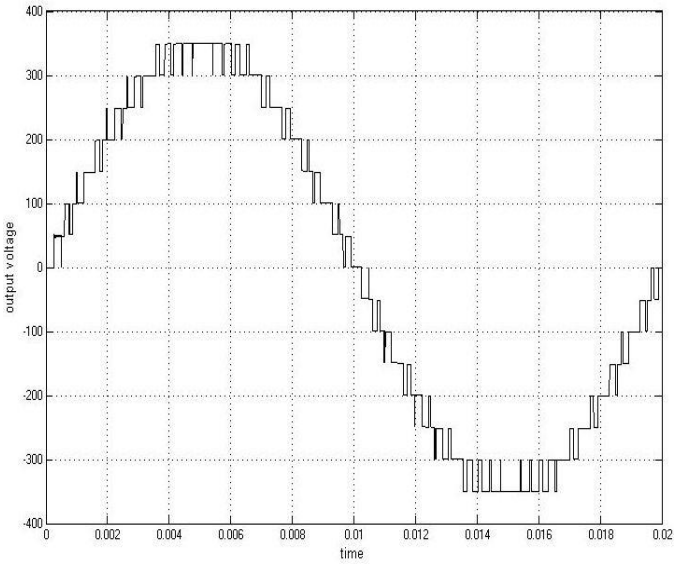

Fig 18: output voltage waveform of proposed fifteen level with PWM technique

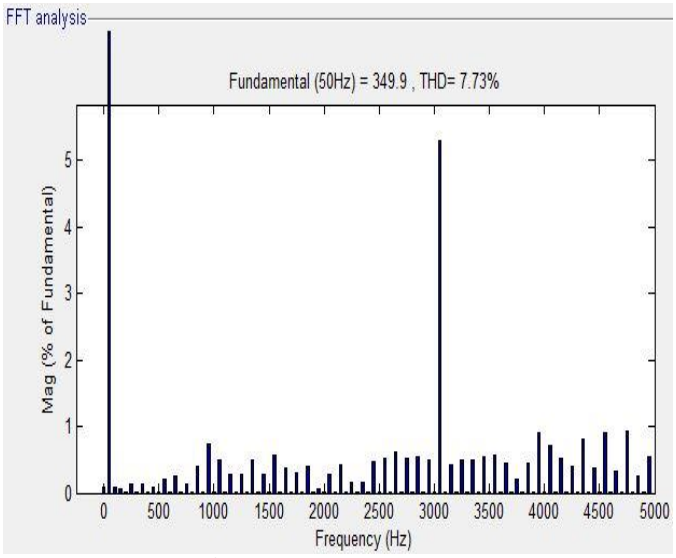

Fig 14: THD of the proposed inverter with PWM technique

V. CONCLUSION

A new multilevel inverter topology with reduced number of switches is proposed in this paper. Proposed inverter with phase shifted carrier PWM and without PWM technique is also presented. This inverter uses only six switches to get fifteen level voltages across the load. From the simulation results the THD content is less when phase shifted carrier PWM technique employed compared to without PWM technique. The proposed inverter can also be used to integrate the renewable energy sources with existing grid.

REFERENCES

[1] Fang ZhengPeng ,Jih-Sheng Lai, and Rodriguez, J."Multilevelinverters: a survey of topologies,controls, and applications",*Industrial Electronics,IEEE Transactions*,Vol. 49, issue:4, pp. 724-738, Aug 2002.
[2] S. Khomfoi, L. M. Tolbert**,** "Multilevel Power Converters," *Power Electronics Handbook, 2nd Edition Elsevier, 2007, ISBN 978-0-12- 088479-7,* Chapter 17, pp. 451-482.
[3] Lezana P, Rodriguez J, Oyarzun DA. *Cascaded multilevel inverter with regeneration capability and reduced number of switches*. IEEE Trans Ind Electron 2008;55(3):1059–65.
[4] Hinago Y, Koizumi H. A single-phase multilevel inverter using switched series/ parallel dc voltage sources. IEEE Trans Ind Electron 2010;57(8):2643–50.
[5] Gui-Jia Su. Multilevel dc-link inverter. IEEE Trans Indus Appl 2005;41(3): 848–54.
[6] Veenstra M, Rufer A. Control of a hybrid asymmetric multilevel inverter for competitive medium-voltage industrial drives. IEEE Trans Ind Appl 2005; 41(2):655–64.
[7] Ruiz-Caballero DA, Ramos-Astudillo RM, Mussa SA, Heldwein ML. Symmetrical hybrid multilevel dc–ac converters with reduced number of insulated dc supplies. IEEE Trans Ind Electron 2010;57(7):2307–14.
[8] Manjrekar MD, Lipo TA. A hybrid multilevel inverter topology for drive applications. Proc IEEE Int Conf 1998;2:523–9.
[9] Manjrekar MD, Steimer PK, Lipo TA. Hybrid multilevel power conversion system: a competitive solution for high-power applications. IEEE Trans Ind Appl 2000;36(3):834–41.
[10] Marchesoni M, Tenca P. Diode-clamped multilevel converters: a practicable way to balance DC-link voltages. IEEE Trans Ind Electron 2002;49(4):752–65.

