LOW SIZE AND LOW POWER CONSUMPTION WIRELESS CAPSULE ENDOSCOPY

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Abstract:- The wireless capsule endoscopy having low energy consumption as well as the hardware which is required to it will be less as compared to other endoscopy This technology is based on detection of GI Fact To detect the tumor or any abnormality in GI tract can easily detect and give the compressed image of this tract .The cross like burst error can be avoided by using FEC. In this endoscopy the compressor is significant because it uses the column Rice algorithm instead of Huffman table. This compressor is based on discrete cosine transform. By using FEC retransmission of data can not be necessary. Because due to the FEC the compression of image will done. Therefore the size of image decreases this gives the significance building the memory. As compared to previous system. size of FPGA chip is 65mm which is low power. Therefore this system is FPGA based

Keywords:- Image compression, low power design, wireless Capsule endoscopy (WCE).

I. INTRODUCTION

Wireless Capsule endoscopy is a way to record images of digestive tract for use of medicine. This technique was invented in Japan the first Capsule endoscope was introduced by imaging ltd. Now much , more companies and U.S. food and drug Administration (FDA),The capsule is the size and shape of a pill the system consists of a sensor array or electrode, which are attached to patients abdomen. These are connected to data recorder. The capsule having size 26 X11 mm and consists optical done, a lens, several light emitting diodes, a semiconductor, transmitter and an antenna. The primary use of capsule endoscopy is to examine areas of the small intestine and GI tract to record the images.

The activities are first capsule travels through the escophagus, stomach and small intestine it takes photographs rapidly. The photographs are transmitted by the radio transmitter to small receiver that is wornon the waist of the patient who undergoing the capsule endoscopy. The p^H, temperature can be detected by using WCE

At the transmission side of WCE using the single image of QVGA (320X240 pixels, 8 bits per pixel). The VGA having 2.45 mb amount having 640 X 480, 8 bits per pixel. The QVGA has 64kb amount if images. The data transmitter has a 2~3 Mb/s. Wireless capsule endoscope is flexible endoscope the complexity is less. It contain CMOS camera which acquires two images per second. The life of battery is 8 hours. The compression factor is in 5 to 20 range. The compression is lossy compression. The image is not JPEG or MPEG because the complexity is huge in it therefore it uses the CFA (color filter array) to work on it.

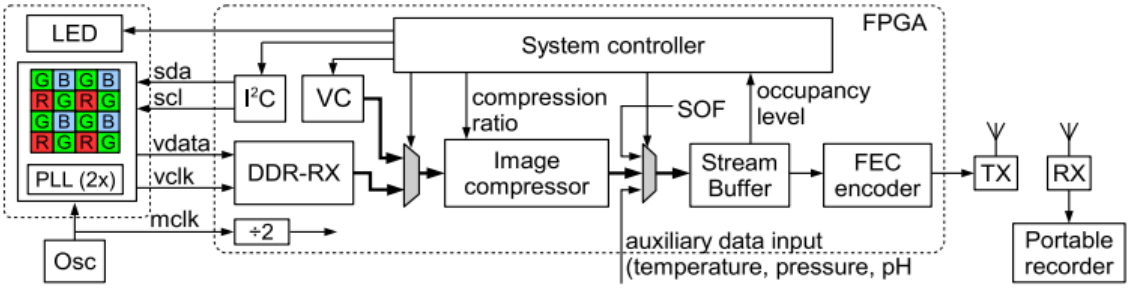

Fig.1. Simplified block diagram of Wireless Capsule Endoscopy (7)

II. SYSTEM OVERVIEW

The System implementation is as shown in fig. The block diagram of wireless capsule endoscope. It contains the custom CMOS image sensor with CFA an LED based illumination module an FPGA chip implementing all image and data processing tasks, a radio data transmitter and an external receiver.

In the fig (1) the CMOS sensor which gives the images to FPGA chip. The delivery of these images is fast of data rate is at low voltage differential double data rate. The V_{clk} and V_{data} lines are used for the serial interface. This serial interface is guaranteed by LVDS –DDR. This type of interface is reduces the leakage of current. The data will receive serially using V_{clk} and V_{line} then it converted into parallel by using DDR -RX interface. The rate of bit stream is higher than data rate of radio transmitter therefore the readout of compressor output image pixels. Stream buffer is used to store this compressor output. The compression of image is controlled by system controller. This controller maximizes the quality of image by adjusting compression factor.

Bit-error-rate (BER) is used at the receiver side because it can prevents the error and it can kept below 10^{-8} .To lower BER the FEC codes are used. These FEC is based on Reed-Soloman algorithm. This algorithm has three characteristics like length, dimension and minimum distance of code. It can correct 16 error in transmission bytes in every 255 length of Rs frames. The last part of Rs frame used to carry the non-image data to determine PH and temperature measurements.

This fig.1.show overall process of WCE in which image compression in transmitting the image of GI tract. The discrete cosine transform (DCT) is used to decrease the complexity. The Golomb- Rice algorithm is used on entropy encoder. The hardware implementation is done in silicon area therefore costly RAM is not required. The clock frequency is halved where operating rate is 24 fps with QVGA image is halved where operating rate is 24 fps with QVGA image is halved where operating rate is 24 fps with QVGA image.

III. IMAGE COMPRESSION

In this lossy compression is done. This WCE designed to size, consumable power and available transmission bandwidth. This WCE captures the color images of GI tract. The receiver data represents in one- third of the original image intensities. Due to lossy compression some data must be lost this data recovered by interpolation. The received image under goes some processing for reduction of noise. Any physical injury is occurred in GI tract this can detected by WCE and take image of low resolution.

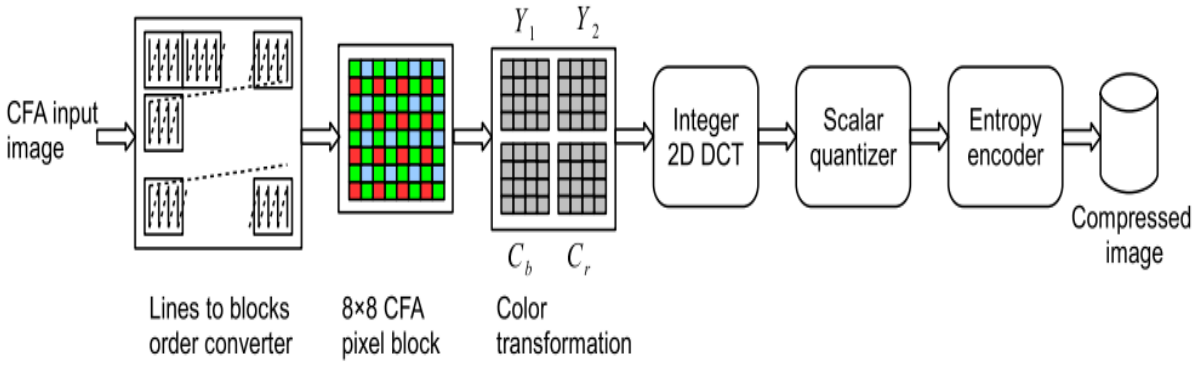

Fig.2. Transform based image coder (7)

The image compression is as shown in fig. (2). The color interpolation can be performed at a CFA digital cameras. It will help to construct full color image without increasing the image information content triples the amount of compressed data. In the compression color interpolation and does not increase amount of data. This can perform at receiver side with the help of various algorithms. The compressed image divides into separate NxN pixel blocks. Then each pixel block undergoes the 2-D DCT transformation. Then resulting coefficients are quantized and encoded using a dedicated low-complexity, low-memory encoder.

The steps involved in compression of data are as follows:

A. Conversion of Progressive Pixel Scan to Block-Wise Order

B. Color and Structure Transformation

C. Image Transformation

D. Coefficient Encoding

A. Conversion of progressive pixel scan to Block- Wise Order

The image can be stored in low cost off chip memory . The readout of image is line by line this may cause a problem in storage therefore image can stored temporarily. CMOS sensors are responsible to the design therefore the image compressor operate on small non overlapping image blocks. Wise the output image can compressed because the storage of image is off chip. The off chip memory having the power and space limitations. The on chip static memory i.e. SRAM has more costly than off chip but the storage of image lines can easily done. For the linear arrangements of image lines, some converters are used.

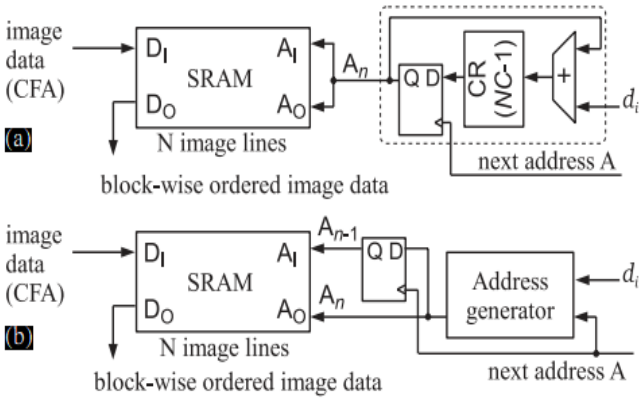

Fig.3.Linear to block-wise order converter (7)

The fig.3. shows the converter operation in this number of rows i.e. N=3 lines and Number of columns i.e. C=12 pixels. This fig shows the SRAM storing of image in the form of rows and columns. The rows gives the lines present in

image and columns gives the pixel present in image by using this the column wise readout can easily done.

In the column wise readout at initial the buffer will getting filled line by line if the buffer will fulfilled then it start the column wise readout like 0,12,24,1…..The readout process ends with current conversion and then it start the new buffer. In this conversion process the system clocks frequency must be doubled and the interruption in readout can not be allow these are the draw backs of this conversion.

The conversion of linear to block wise is as shown in fig. This conversion is called in place. In these conversion NxC pixels can be taken into consideration. The storage of images in this buffer. This algorithm starts when buffer is full. Single write in operation gives singles readout. Then as previous the buffer can be fulfilled .The block wise arrangement is done and then the column wise readout. In this algorithm the address of current position is set at read write operation of previous one.

The another one algorithm is used in this conversion i.e. dual port SRAM buffer. In this the converter can work one pixel per clock cycle but sometime this dual part SRAM can not support to memory read/work operation. At same address and same clock frequency.

B. Color and structure transformation

The big shows the color and structure transformation in this R(Red), G(Green),B(Blue) color which represent the single value for each pixel but the compression of this R,G,B, can not independently done. Therefore the color and structure transformation is done. By using this color transformation (CT) the down sampling of RGB done. Therefore for the better compression map the CFA color space into a space.

The transformation of R, G, B to the luma and chroma component. The green is converted into luminance i.e. Y and the blue and Red is converted into chrominance Cb and Cr

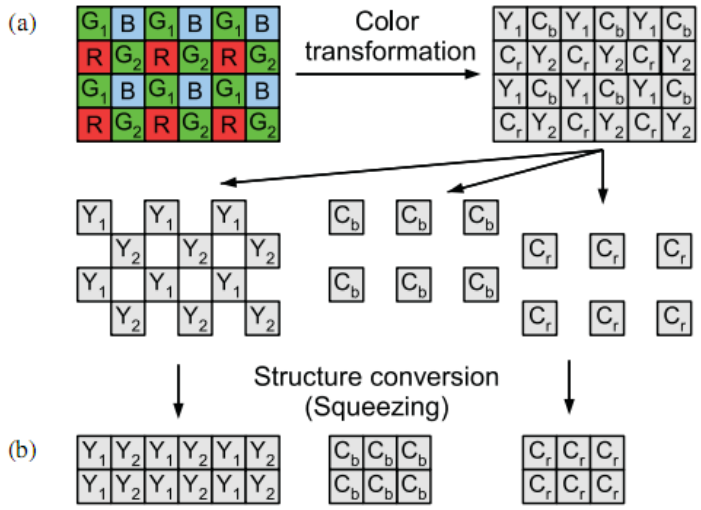

Fig.4. Image after (a) color transformation and (b) structure conversion. (7)

respectively. The R G B array gives the Cb and Cr array as shown in Fig.4.(a). The each luminance can be removed from as well as the both chroma component can be separated out. In this if any empty pixel occurred then this pixel can be removed. The separation of luma and chorma component is called structure separation and structure conversion .

In structure conversion as shown in fig.4. (b)the too rectangular array is products in which one is of odd luma pixel (Y1) and another is of even luma pixel (Y2). The Cb and Cr also products the array. In the array arising effect can be generated. To avoid this arising the low pass filter is used.

C. Image Transformation

In reducing the interpixel correlation the linear orthogonal transformation can be done. It is highly effective because neighboring pixels in natural images are straggly correlated with each other. The type of transformation and size (N) can decide the packing efficiency of transformation. In this transformation the DCT is

used. The size of N can choose by considering the block wise order converter. If the implementation make efficient then it requires the power of 2. This power is taken into consideration which is size N. the natural image has 16x16 DCT having 9.45dB and 8x8 DCT having 8.82 dB We use the 16x16 DCT having 9.45 dB because it gives more packing efficiency than 8x8 DCT.

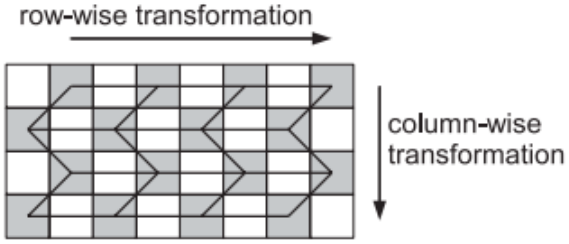

Fig.5. 2-D block transformation of luma component (7)

CFA image compression apply on 8x8 DCT. The second pixel in the image where chroma is present is empty i.e Cb and Cr. Due to this empty pixel this 8x8 DCT can be equivalent to 4x4 block with full color image. This transformation is not easy in luminance because the distance between neighboring component of luma is 2 in row wise transformation and it is >2 is column wise transformation.

In this image transformation 2-D DCT is transform separately into 1-D row wise transform and 1-D column wise transform. Therefore, hardware complexity can be reduces. The 4x4 blocks are used instead of 8x8 blocks therefore size of blocks can be reduces. Therefore, this algorithm gives the hardware efficient algorithm. The transformation of 2D-DCT image form a new image in every 16 clock cycles.

D. Coefficient Encoding

With the increasing block size the coefficient quantization become more visible .If we use 4x4 DCT it gives low complexity ,low memory which is efficient in encoding. Due to this low complexity here we use the AGR algorithm instead of Huffman table . The AGR algorithm requires the low power. In this encoding the run length encoding is used .

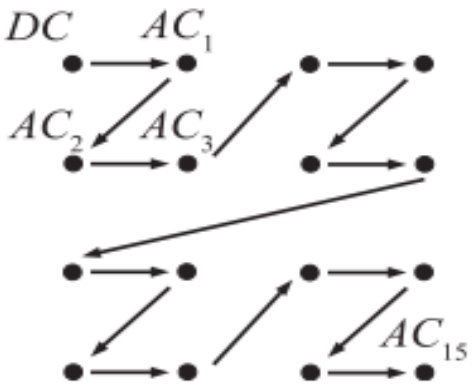

Fig.5. Scanning 4x4 image block transformation (7)

As shown in fig.5 the AC and DC component are present each component has a different statistical properties .The AC component scanned zig zag order. DC is starting coefficient in image the correlation of this component with its adjacent having strong correlation. Every DC coefficient clustered with low frequency coefficient . After scanning the AC coefficient it can converted into intermediate sequence of symbol (z, v). z is zero value and non zero coefficient symbol is (0, 0).

IV. COMPRESSION RESULTS

The result of compression is taking into consideration with the help of comparison between the previous compression results as well as JPEG, JPEG 2000 and CFA scheme. The WCE images gives the high quality, full color images. In the evaluation of reconstruction of images can be defined by using peak signal to noise ratio which is defined as

$$\mathrm{PSNR}(dB) = 10\log_{10}\frac{255^2}{\left\langle (x_i - \hat{x}_i)^2 \right\rangle}$$

$$PSNR = 10\log_{10}\frac{I_{\max}^2}{D},$$

I_{max} is the maximum intensity of image, and D is defined as,

$$D = \frac{1}{M \cdot N}\sum_{m=0}^{M-1}\sum_{n=0}^{N-1}(\hat{x}_{m,n} - x_{m,n})^2.$$

Where M, N- size of image , $X_{m,n}$ – pixel value in original image, $\hat{x}_{m,n}$ corresponding pixel value of reconstructed image.

The value of PSNR is fixed and due to this the compressed image can produced. This compression of image can produced .This compression of image can be calculated by

taking the ratio of size of original image to the reconstructed image. Using this the calculation of compression is introduces due to the various algorithm and encoder.

Algorithm	Measure	(a)	(b)	(c)	(d)	(e)	(f)
JPEG	PSNR	33.08	34.16	34.31	35.43	36.08	36.94
	CR	9.12	9.86	12.26	13.36	15.95	17.74
JPEG2000	PSNR	33.13	34.18	34.10	35.39	36.06	36.93
	CR	4.74	5.03	15.84	16.81	24.05	30.55
Work [22]	PSNR	33.09	34.19	34.33	35.39	36.03	36.88
	CR	9.67	10.65	9.58	10.57	14.95	17.02
This work CT (7)	PSNR	33.09	34.19	34.33	35.39	36.03	36.88
	CR	10.15	11.13	10.24	10.97	16.10	18.46
This work CT (8)	PSNR	33.10	34.19	34.33	35.39	36.03	36.88
	CR	10.49	11.20	10.70	10.97	16.29	18.18

Table 1.Compression results of test images (7)

Due to the image transformation and color and structure conversion the unwanted pixels like empty pixels can be eliminated therefore number of pixels can be reduces. As the PSNR value is higher then the smooth image can be obtain high compression ratio. The following table shows the compression between the JPEG , JPEG 2000 and CT . In this table the values of PSNR and CR are compared with each other.

System	Clock Frequency	On-chip Memory Size	Power/Energy Consumption	Technology
Work [15] (8 fps, QVGA)	40 MHz	732 Kb	6.2 mW, (1.8 V) 0.77 mJ/image frame	ASIC 180 nm
Work [20] (8 fps, QVGA)	20 MHz	746 Kb	1.3 mW, (0.95 V) 0.16 mJ/image frame	ASIC 180 nm
Work [22] (24 fps, QVGA)	24 MHz	107 Kb = 40 Kb (pixel buffer) + 64 Kb (stream buffer) + 3 Kb (Huffman tables)	9.6 mW, (1.2 V) 0.4 mJ/image frame	FPGA 65 nm
This work (24 fps, QVGA)	12 MHz	84 Kb = 20 Kb (pixel buffer) + 64 Kb (stream buffer)	7 mW, (1.2 V) 0.29 mJ/image frame	FPGA 65 nm

Table 2. Comparison between other WCE systems (7)

V. IMPLEMENTATION RESULT

By using above all algorithm step in compression of image and encoder can gives the small size FPGA chip is 65 nm having low power consumption. The capsule contain 5 circular 1chips having diameter 10 nm. These 5 chips are as shown in fig 6. The power consumption of FPGA is nearly 12 mW at the running compressor and if the compressor is off then this value becomes 5.8 mW. The interfacing of DDR-LVDS having frequency 48 MHz and time 8.2ms. The total consumption of power at normalized phase is 0.29mJ and 0.16 mJ per image frame.

In the implementation of LED module 4 LED's are mounted. This 4 LED's consumes 50mW power. The imager consumes 40 mW power whereas 5mW consumed by radio transmitter and finally the FPGA core can consumes 7 mW.

By using the RS algorithm the unnecessarily retransmission of frame is avoided. Using AGR algorithm the power consumption decreases therefore BER reduces which is nearly 10^{-3}. Therefore reduction in power and hardware can achieves and efficient transmission can also achieve.

As shown in Table 2 the comparison of this WCE with other WCE considering the parameters like clock frequency, on chip memory, power and the technology which is used in WCE i.e whether it is ASIC or FPGA. The implementation of WCE using 5 circular plates gives the capsule this implementation is shown in fig.6.

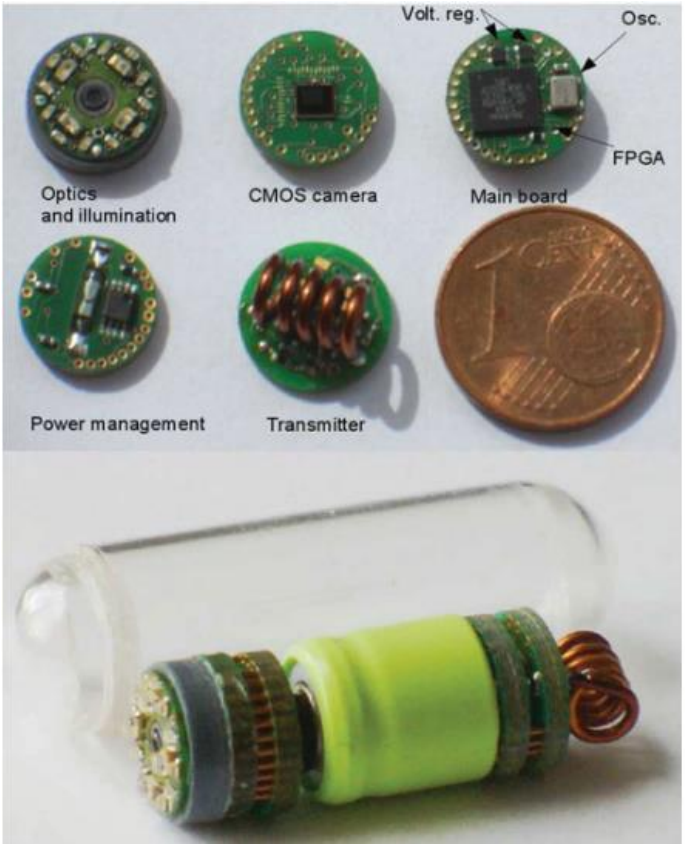

Fig.6. Implementation of WCE (7)

VI. CONCLUSION

The wireless capsule endoscope can be implemented as per efficiency requirement. The low power and hardware efficient endoscopy can be archived by using this FPGA chip. The FEC can correct the error and various transformation and conversion reduces the size of images. The output images is in form of QVGA which has clock frequency 12 MHz. The off chip memory is used in WCE. The retransmission of unnecessarily data can avoided and recovery of data is fast in this due to FEC encoding. To energy consumption in WCE is nearly 0.29 mJ for every compressed image. Therefore , WCE gives high compression ratio, lower energy and small amount of on-chip memory.

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