A 1.5v CMOS Fuzzifier Using Adaptive Biasing

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Abstract*— A versatile low-voltage CMOS Fuzzifier circuit with a trapezoidal transconductance characteristic and independently programmable slope, height and horizontal position is designed in 0.35μm standard CMOS technology .The proposed circuit uses adaptive biasing linearization techniques to achieve wide tuning range. Simulation results using HSPICE and level 49 parameters (BSIM3v3) that verify the functionality of circuit with 1.5 V supply are presented.

***Keywords*— Fuzzifier, Transconductor, Low-voltage, Low-power, Adaptive Biasing, Fuzzy.**

I. INTRODUCTION

Zadeh proposed in 1965 a logic with fuzzy truth, connection and rules of inference, which was named Fuzzy logic. This approach has been successfully applied in many fields, like automatic process control and expert system and pattern recognition.

The fundamental operation in fuzzy logic is fuzzification which consists of the determination of the degree of association of a variable to a fuzzy set [1] and is implemented by means of fuzzifier. This circuit provides a nonlinear relation that measures the compatibility of an object with the concept represented by a fuzzy set. Usually, fuzzifiers have a triangular or trapezoidal shape and, in order to guarantee general application, it needs to have programmable parameters (horizontal position, height, width and edge slope). [2] (Fig.1)

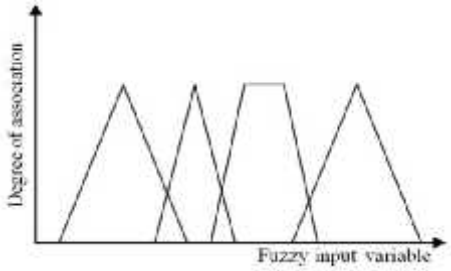

Fig 1. Fuzzification of an input variable using membership function

For designing Fuzzifiers three generally methods exist; voltage-mode, current-mode and transconductance-mode circuits. Input and output signals are voltages in voltage-mode circuits and currents in current-mode circuits.

Transconductance-mode circuits have a voltage input signal and a current output signal. This latter choice is often preferred as the distribution of the input signals and the combination of the output Signals are simplified. Using these techniques several interesting CMOS fuzzifier have been reported. [3]- [7] Often in the applications which fuzzifier in transconductance mode is used, the input transconductor determine the overall linearity of the system. Modern fabrication technologies and wireless applications also require low supply voltage and low power consumption, which make it difficult to achieve transconductors with high linearity and low supply voltage over a reasonable input range.

Consequently, multiple circuit techniques have been proposed in literature to improve the linearity of MOS transconductors.[8]- [11] The reported linearization techniques include: cross-coupling of multiple differential pairs, adaptive biasing, source degeneration (using resistor or MOS transistor), shift level biasing, series connection of multiple differential pairs and pseudo-differential stages(using transistor in the triode region or in saturation).

In this paper, we report a versatile circuit for the implementation of CMOS transconductance-mode fuzzifier circuit. The circuit uses supply voltages 1.5V which significantly lower than most previous proposals. The circuit uses the adaptive biasing techniques to improve the linearity.

Furthermore, it can be employed for all applications where a highly accurate voltage to current conversion should be realized.

The adaptive biasing linearization technique has been briefly reviewed in section 2 and the proposed high-linear MOS transconductor is introduced in this section, also the dc transconductance characteristic of the proposed circuit is presented in this Section.

The proposed fuzzifier is presented in section 3 and several simulation results are presented in section 4. Conclusion is presented in section 5.

II. CMOS IMPLEMENTATION OF FUZZIFIER CIRCUIT

In this section, a new circuit for the generation of trapezoidal functions is described. In the following, the proposed circuit will be presented starting from the linear transconductor used. Then, the circuitry needed to generate the trapezoidal shapes will be added.

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A. Linear Transconductor Design

Considering quadratic *i* - v characteristics for the MOS transistors and neglecting the channel length modulation effect, the simple differential MOS transconductor has a transfer characteristic given by

$$i_o = \sqrt{2KI_o}\,v_i\sqrt{1-\frac{v_i^2 K}{8I_o}} \quad (1)$$

Where k represents the transconductance parameter ($k = \mu C_{ox}\frac{W}{L}$).

Better linearity can be achieved for large effective gate-to-source voltages $V_{GSeff} = V_{GS} - V_{TH}$. For low-voltage applications this constitutes a major drawback Furthermore, large transconductance values can be obtained only by using large bias currents and large area transistors; however this changes cause to enlarge the power consumption and active area.

One of the topologies for linearization of the transfer characteristic of MOS transconductors is using the adaptive biasing current source.[12]

The idea is using a dynamic bias current containing an input dependent quadratic component to cancel the nonlinear term in equation (1). Hence, if the bias is defined as equation (2),

$$I_o = I_o' + \frac{kv_i^2}{8} \quad (2)$$

And put this equation in equation (1) the transfer characteristic becomes linear and could be realized according to equation (3)

$$i_o = \sqrt{2kI_o'}\,v_i \quad (3)$$

B. The novel low-voltage circuit for generating the adaptive bias current

Fig. 2 shows the new low-voltage circuit for generating the adaptive bias current.

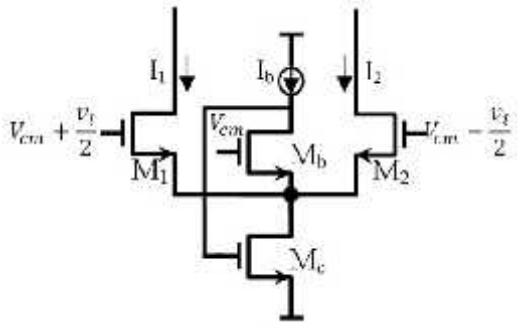


Fig. 2 Adaptive bias current generator

Assuming the same sizes for M_1, M_2, it can be easily shown that:

$$I_1 = \frac{1}{2}k_1\left(V_{cm} + \frac{v_i}{2} - V_{cm} + V_{GSb} - V_{th}\right)^2 = \frac{1}{2}k_1\left(\frac{v_i}{2} + V_{GSb} - V_{th_b}\right)^2 \quad (4)$$

Where k_1 is the transconductance parameter of input devices, M_1 and M_2, ($k_1 = k_2 = \mu C_{ox}\frac{W_1}{L_1}$)

Similar attempt for I_2 terminates to equation (5):

$$I_2 = \frac{1}{2}k_2\left(\frac{-v_i}{2} + V_{GSb} - V_{th}\right)^2 \quad (5)$$

Replacing V_{GSb} as a function of the bias current I_b

$$V_{GSb} = V_{th} + \sqrt{\frac{2I_b}{\mu C_{ox}\frac{W_b}{L_b}}} \quad (6)$$

The following expression result:

$$I_1 = \frac{1}{2}k_1\left(\frac{v_i}{2} + \sqrt{\frac{2I_b}{\mu C_{ox}\frac{W_b}{L_b}}}\right)^2 \quad (7)$$

$$I_2 = \frac{1}{2}k_2\left(\frac{-v_i}{2} + \sqrt{\frac{2I_b}{\mu C_{ox}\frac{W_b}{L_b}}}\right)^2 \quad (8)$$

The current passing through M_C is equal to the sum of I_1, I_2 and I_b as clarified in equation (9):

$$I_c = I_1 + I_2 + I_b = I_b + \frac{1}{2}k_1\left(\frac{v_i^2}{2} + \frac{4I_b}{\mu C_{ox}\frac{W_b}{L_b}}\right) \quad (9)$$

As seen in (9), the current of M_C is related in quadratic relation with the input differential voltage.

If a copy of the current of M_C is mirrored into the tail current of basic differential pair which is discussed former in section 2.1, equation (10) can be concluded from combination of equations (1) and (9):

$$i_o = \frac{1}{2}kv_i\sqrt{\frac{8}{k}I_b + \frac{16k_1}{kk_b}I_b + \frac{2k_1}{k}v_i^2 - v_i^2} \quad (10)$$

Where $k = \mu C_{ox}\frac{W}{L}$ is the transconductance of basic differential pair, $k_1 = \mu C_{ox}\frac{W_1}{L_1}$ is the transconductance of adaptive biasing differential pair and $k_b = \mu C_{ox}\frac{W_b}{L_b}$ is the transconductance of M_b transistor. If $k_1 = 0.5k$ the transfer characteristic becomes completely linear according to relation (11):

$$i_o = \frac{1}{2}kv_i\sqrt{\frac{8}{k}I_b + \frac{8}{k_b}I_b} \quad (11)$$

C. The novel linear MOS transconductor

We proposed a new MOS transconductor that uses the linearization approach presented above. The proposed circuit consists of 3 main blocks; an adaptive biasing current generator, a high performance current mirror and a main differential pair (fig. 3). M_{C1}- M_{C4} Formed a high performance current mirror. [13] This circuit copy the dynamic current that produced by Adaptive bias current generator circuit which formed by Ma_1, Ma_2, Mb and Mc into the source of the transistors of main differential pair with source degeneration transistor which formed by M_1- M_2.

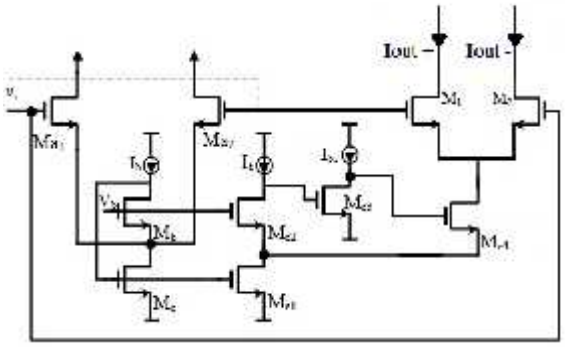


Fig. 3. The novel linear transconductor

M_b , current source I_b and V_b forces the V_{DS} voltage of transistor M_C to a constant value. A replica of this circuit is used to force the V_{DS} voltage of the transistor M_{C1} to be equal to that of transistor M_C.

To have high output impedance, the output cascade transistor M_{C4} is driven by the drain of transistor M_{C2}. As the polarity in the drain of transistor M_{C2} is reversed, an inverting stage is required to drive the gates of transistor M_{C4} .This Inverting stage provides additional gain-boosting, which increases the output impedance. The inverter amplifier has been implemented by means of transistor M_{C3} and biasing current I_{b1}.

The minimum supply voltage is limited by the path formed by I_b, M_b and M_C , so the minimum supply voltage is

$$V_{DD}^{min} = V_{GSC} + 2V_{DSbsat} \qquad (12)$$

where V_{GSC} is gate-source voltage of M_C , V_{DSbsat} is the minimum voltage drop in current source I_b and can be as small as 0.15V in 0.35µm CMOS technology, $V_{th} = 0.65$ V for NMOS ,so

$$V_{DD}^{min} = V_{th} + 3V_{DSsat} = 0.65 + 3 \times 0.15 = 1.1V$$

We have selected V_{DD}=1.5 V in order to have an appreciable voltage swing.

The proposed transconductor was laid out in standard 0.35µm CMOS technology. Post layout simulations from extracted circuit were performed for a single 1.5 V supply using HSPICE and level 49 parameters (BSIM3V3). Fig. 4 shows DC characteristic of proposed transconductance circuit.

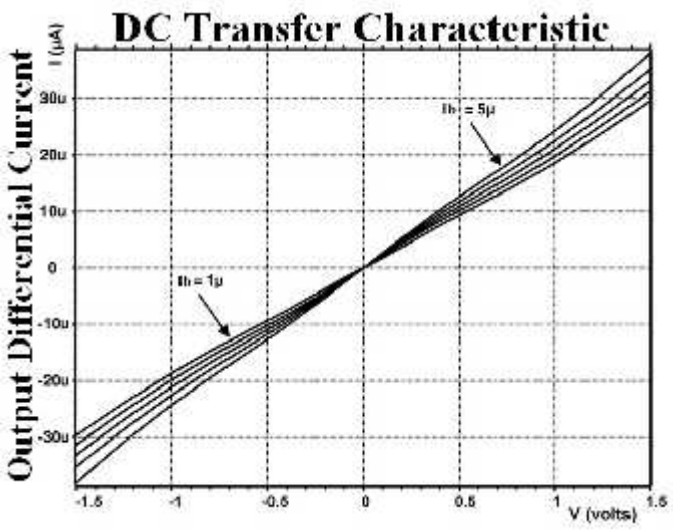
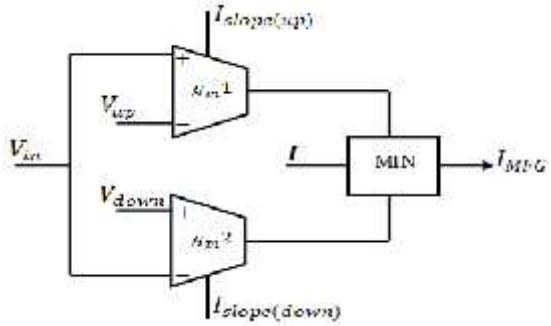


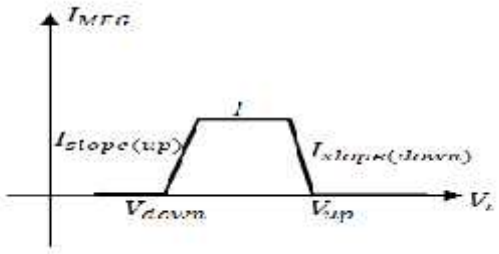
Fig. 4. .Post layout simulated DC transfer characteristic for Ib from 1µA to 5µA by 1µA step

III. Fuzzifier circuit

Using two instances of transconductor in Fig.4 and a minimum current selector circuit, a trapezoidal transconductor characteristic can be generated (Fig.5)



(a)



(b)

Fig.5 (a) MFG block diagram (b) MFG output

This block consists of two transconductors. One creates a positive ramp and the other creates a negative ramp, one defines the V_{up} and the other defines V_{down} , also each transconductor can independently define the slope of the up and down part via bias current I_b , then outputs go through a

minimum current selector circuit which takes the minimum of them to construct a trapezoid output current.

The new low voltage MIN circuit is shown in Fig.6

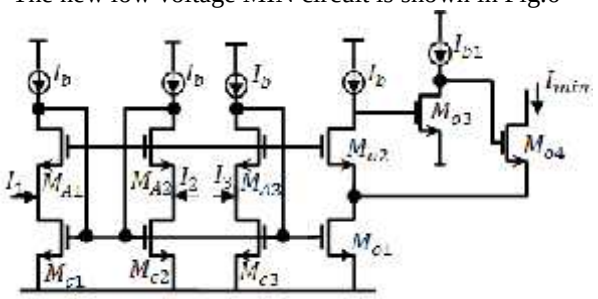


Fig 6. MIN circuit

A proposed circuit has 3 input branches and each branch consists of a current sensing transistor M_{Ci} and a voltage follower M_{Ai} while the gates of transistors M_{Ai} are connected to a common-mode constant voltage V_b .

V_{GS} voltages of all M_{Ci} transistors are equal and proportional to minimum of input currents of I_1, I_2, I_3.this condition drive them to have different V_{DS} voltage. Since they (M_{C1}, M_{C2} and M_{C3}) have different V_{DS} voltage, the voltage follower of all branches (M_{A1}, M_{A2} and M_{A3}) are turned off with the exception of voltage follower in the loosing branch that has the minimum of input currents I_1, I_2 and I_3.

This transistor remains ON and with M_{O1}- M_{O4} formed a high performance current mirror that can copy the minimum current to the output.

This MIN circuit also defines the fuzzy one level for whole MFG circuit. By choosing the value of **I** for the fuzzy one value we also can cut the output signal at the level we want so in other words selecting **I** value, we can use the most linear part of the output signal.

IV. Simulation

The Fuzzifier depicted in fig.6 was laid out in standard 0.35µm CMOS technology. Post layout simulations from extracted circuit were performed for a single 1.5 V power supply voltage using HSPICE and level 49 parameters (BSIM3V3).

Figure 7 and 8 and 9 shows SPICE simulation of the MFG. All the parameters are independently tunable.

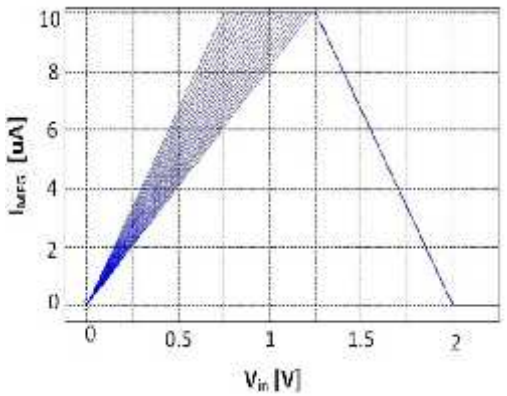


Fig 7. MFG slope tunability

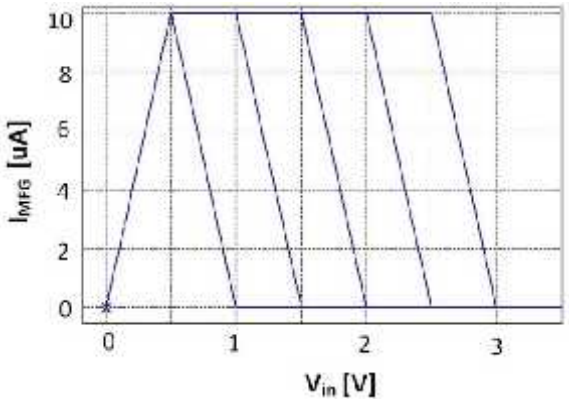


Fig 8. MFG width tunability

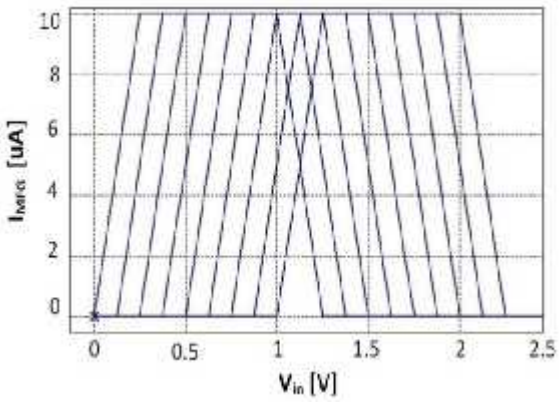


Fig 9. MFG position tunability

V. Conclusion

A novel low-voltage CMOS circuit for the Implementation of trapezoidal transconductance Functions with programmable characteristics have been introduced. The proposed circuit uses the source degeneration linearization method to achieve better linearity. The circuit can be used for the implementation of VLSI analogue neuro-fuzzy systems. The proposed circuit has independently adjustable height, slope, position, and width of the trapezoidal function and has been verified by simulation results.

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