A 1.5 V Minimum Current selector circuit

Behzad Ghanavati, Milad Kaboli, Zohreh Manoochehri

Sama Technical and Vocational Training College, Islamic Azad University, Mahshahr Branch, Mahshahr, Iran
B.ghanavati@mahshahriau.ac.ir

***Abstract*— A low-voltage CMOS current-mode Minimum current selector circuit is designed in 0.35 µm standard CMOS technology.Simulation results using HSPICE that verify the functionality of circuit with 1.5 V supply are presented. The circuit can find application in the implementation of Fuzzy and Neural Network circuits.**

***Keywords*— Analog processing circuit, Minimum Current Selector, LTA, Low-Voltage.**

I. INTRODUCTION

Winner-Take-All (WTA) and Looser-Take-All (LTA) circuits are the analog important and major function building blocks. The function of WTA and LTA circuits identify the largest and the smallest input variable, respectively, and restrains the remaining ones. WTA and LTA are widely used in hardware implementation of fuzzy logic systems, nonlinear filters and self-organizing neural networks, vector quantization, Hamming network, competitive learning, etc.

WTA and LTA can be extensively categorized as the current mode and voltage mode structure. Using current mode analog circuit design has received wide attention due to the supply voltage scaling down and their potential of lower power consumption [1]-[3]. In addition existing voltage mode structures are larger than current mode structures in hardware and area.

In this paper we proposed a novel current mode minimum current selector. There are several structures of current mode MIN circuit proposed on the literature [3]-[6].Our proposed circuit can work under low voltage (1.5 V) power supply that is lower in comparison with previous works. Moreover, it doesn't need any subtraction of current for detecting the minimum current, so precision of the current is preserved.

Section 2 presents the proposed circuit architecture and describes it operation. Simulation results are presented in section 3 and section 4 concludes this paper.

II. CIRCUIT DESCRIPTION

A LTA-Min circuit can be formed as shown in Fig.1. The basic structure of the proposed circuit consists of two branches. Each of these branches consists of a voltage follower transistor (MA_i) and a current sensing transistor (MC_i). The gate of the MA_is is connected to a fixed voltage V_b.

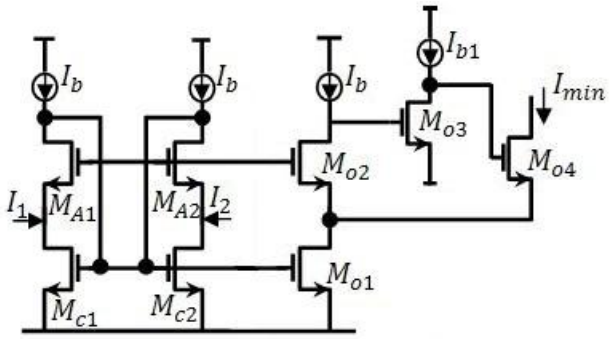

Fig. 1 The prposed Minimum current selector

The gate-to-source voltages of MC_is are equal and proportional to minimum currents I_1 and I_2 so that these transistors have the different drain-to-source voltages. In hence, voltage follower transistors of all of the branches will be turning off, except one, which is in the looser branch. This voltage follower transistor has the minimum current that transmits it to the output by using high quality and appropriate current mirror (MO_1 and MO_4).

Transistor M_{O2}, current source I_b and V_b forces the Drain-to-source voltage of transistor M_{O1} to be a constant value to M_{ci} which is in the looser branch and carry the minimum current.

To have the high output impedance, the output cascade transistor M_{o4} is driven by the drain of

transistor M_{o3}. As the polarity in the drain of transistor M_{o2} is reversed, an inverting stage is required to drive the gates of transistor M_{o4} .This Inverting stage provides additional gain-boosting, which increases the output impedance. The inverter amplifier has been implemented by means of transistor M_{o3} and biasing current I_{b1}.

The minimum supply voltage is limited by the path formed by current source I_b, M_b and M_C, so the minimum supply voltage is expressed as

$$V_{DD}^{\min} = V_{GSb} + V_{DSC,sat} + V_{DSb,sat} \qquad (1)$$

Where V_{GSB} is the gate-to-source voltage of transistor M_b, $V_{DSC,sat}$ is the minimum operating voltage for the current source I_b and $V_{DSC,sat}$ is the minimum drain-to-source voltage of transistor M_c that cause to operate it in saturation region and can be small as 0.15 V in 0.35 µm CMOS technology, V_{tn}=0.6 V. so, the minimum supply voltage is given by

$$V_{DD}^{\min} = V_{tn} + V_{DSsat} = 0.7 + (3 \times 0.115) = 1.15$$

In this paper corresponding to achieved results, we selected V_{DD}=1.5 V in order to have an appreciable voltage swing.

III. Simulation Result

The proposed WTA was laid out in standard 0.35µm CMOS technology. Post layout simulations from extracted circuit were performed for a 1.5 V supply using HSPICE and level 49 parameters (BSIM3V3).

Fig.2 shows the transient simulation result for the proposed Minimum current selector in 500 KHz. Fig. 3 shows the output of the proposed circuit in 50 MHz.

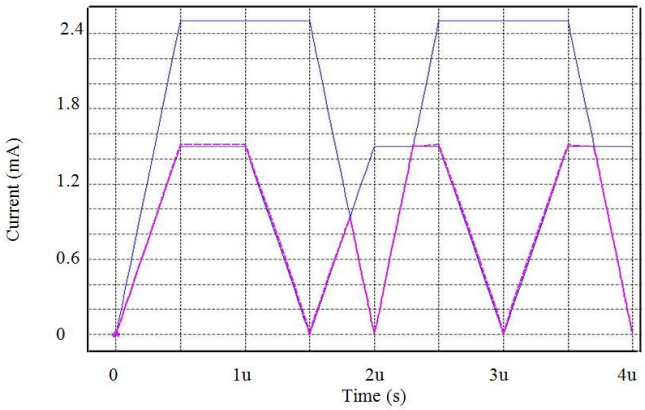

Fig. 2 Min circuit operation in 500 KHz

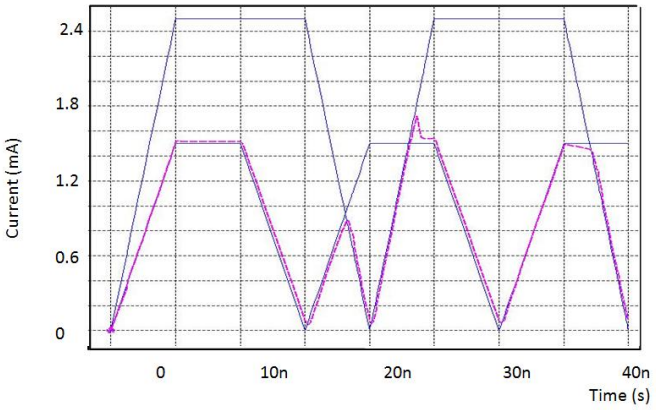

Fig. 3 Min circuit operation in 50 MHz

IV. Conclusions

A new, Low-voltage current mode multi input Minimum current selector circuit is described. The proposed circuit works with a single 1.5V power supply which makes it suitable for low-voltage portable application.

References

[1] [1] A. Fish, V. Milrud, O. Yadid-Pecht, "High-speed and high-precisioncurrent winner-take-all circuit", Circuits and Systems II: Express Briefs, IEEE Transactions on. Vol. 52, No. 3, 2005, pp. 131-135.

[2] [2] J, Ramirez-Angulo, G. Ducoudray-Acevedo, R. G. Carvajal, A.Lopez-Martin, "Low-voltage high-performance voltage-mode andcurrent-mode WTA circuits based on flipped voltage followers",Circuits and Systems II: Express Briefs, IEEE Transactions on. Vol.52 , No. 7, 2005, pp. 420-423 .

[3] Y. Fang, M.A. Cohen, T.G. Kincaid, "Dynamic Analysis of aGeneral Class of Winner-Take-All Competitive Neural Networks",Neural Networks, IEEE Transactions on, Vol. 21, No. 5, 2010, pp.771-783.

[4] Asloni, M., Khoei, A., and Hadidi, K.: 'Design of analog current-modelooser-take-all circuit', IEICE Trans. Electron., 2006, E89-C, (6), pp. 819–822

[5] Huang, C.Y.,Wang, C.J., and Liu, B.D.: 'Modular current-mode multipleinput minimum circuit for fuzzy logic controllers', Electron. Lett., 1996,32, (12), pp. 1067–1069

[6] Dualibe, C., Jespers, P., and Verleysen, M.: 'Embedded fuzzy control forautomatic channel equalization after digital transmissions'. Proc. IEEEInt. Symp. on Circuits and Systems, (ISCAS), Sydney, Australia, 2001,Vol. 3, pp. 173–17