A 1.5 V Current Mode Winner Take All

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***Abstract*— A low-voltage CMOS current-mode WTA (Winner Take All) circuit is designed in 0.35 µm standard CMOS technology.Simulation results using HSPICE that verify the functionality of circuit with 1.5 V supply are presented. The circuit can find application in the implementation of Fuzzy and Neural Network circuits.**

***Keywords*— Analog processing circuit, WTA, Low Voltage.**

I. INTRODUCTION

Winner-Take-All (WTA) and Looser-Take-All (LTA) circuits are the analog important and major function building blocks. The function of WTA and LTA circuits identify the largest and the smallest input variable, respectively, and restrains the remaining ones. WTA and LTA are widely used in hardware implementation of fuzzy logic systems, nonlinear filters and self-organizing neural networks, vector quantization, Hamming network, competitive learning, etc.

WTA and LTA can be extensively categorized as the current mode and voltage mode structure. Using current mode analog circuit design has received wide attention due to the supply voltage scaling down and their potential of lower power consumption [1]-[3]. In addition existing voltage mode structures are larger than current mode structures in hardware and area.

In this paper we proposed a novel current mode WTA. There are several structures of current mode WTA circuit proposed on the literature [4]-[6]. Our proposed circuit can work under low voltage (1.5 V) that is lower in comparison with previous works.

Section II presents the proposed circuit architecture and describes it operation. Simulation results are presented in section III. Conclusion is presented in section IV.

II. CIRCUIT DESCRIPTION

The function of the WTA is to accept input signals, compare their values and produce a high digital output value (logic ‘one’) corresponding to the largest input, while all other digital outputs are set to low output value (logic ‘zero’) [7].

Figure 1 shows the block diagram of the WTA circuit. The circuit includes a 2-input current maximum selector [8] with a voltage inverter.

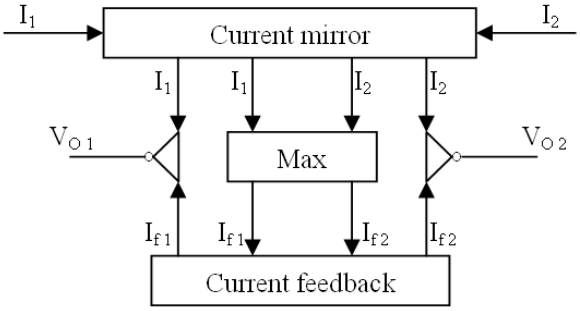

Fig 1. Winner Take All circuit

III. THE CURRENT MAX SELECTOR

The 2-input current maximum selector is shown in Figure 2. The proposed current max selector has 2 input branches and each branch consists of an FVF [14], formed by voltage follower Mai, and current sensing transistor Mci.

Transistor Mai in an FVF performs as an improved voltage follower and the Gate-Source voltage drop of this transistor is constant (neglecting second-order effect) and independent of the load.

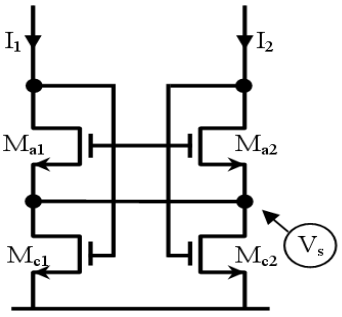

Fig 2. 2-input current max circuit

Transistor Mci operates as a current sensing device. It can sink large current by keeping its Drain voltage approximately

constant. Moreover, the existing impedance at the Source of transistor Mai is very low due to the feedback loop.

The principle of operation of the circuit is as follow. The voltage at node "VS" follows the maximum of input currents I1 , I2, with a DC level shift VGSn where n denotes the maximum current.

In this condition the transistor (Ma1 or Ma2) which carrying the minimum current, have the greater Gate-Source voltage than the value that should have to operate in saturation mode, at this condition this transistor operates in triode mode with Drain-Source voltage value close to zero, thus the current sensing transistor is turning off in this branch and minimum and maximum currents passed through current sensing transistor of winning branch due to properties of FVF cell.

IV. The overall structure of WTA circuit

The circuit of the 2-input WTA is shown in Figure 3. The currents (I1, I2) are the inputs of the circuit.

Each current is mirrored into current max selector, as well as, into the feedback circuit due to PMOS current mirror M12, M22.

Thus the input current of each voltage inverter is:

$$I_{i1} = I_1 - I_{f1} \quad (1)$$

$$I_{i2} = I_2 - I_{f2} \quad (2)$$

We assume at the steady state, the current I1 is the largest input current I1=max (I1, I2)

So

$$I_{f1} = I_1 + I_2 \quad (3)$$

$$I_{f2} = 0 \quad (4)$$

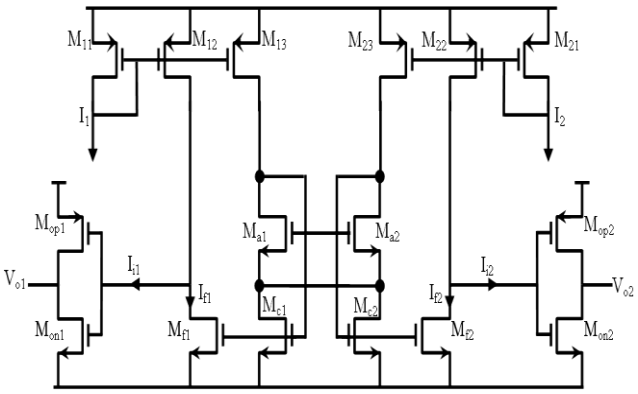

Fig 3. 2-input WTA circuit

From the "Eq. (1)" - "Eq. (4)" the input current of each voltage inverter is:

$$I_{i1} = I_1 - (I_1 + I_2) = -I_2 \quad (5)$$

$$I_{i2} = I_2 - 0 = I_2 \quad (6)$$

This means that only one input current of the voltage inverter corresponding to minimum current is positive and all the other currents are negative. Thus the digital voltage outputs of the circuit will be at logic.

$$\begin{cases} V_{o1} = \text{'one'} \\ V_{o2} = \text{'zero'} \end{cases} \quad (7)$$

V. Simulation Result

The proposed WTA was laid out in standard 0.35µm CMOS technology (Fig.4). Post layout simulations from extracted circuit were performed for a 1.5 V supply using HSPICE and level 49 parameters (BSIM3V3). The total power consumption of circuit is less than 60 µw.

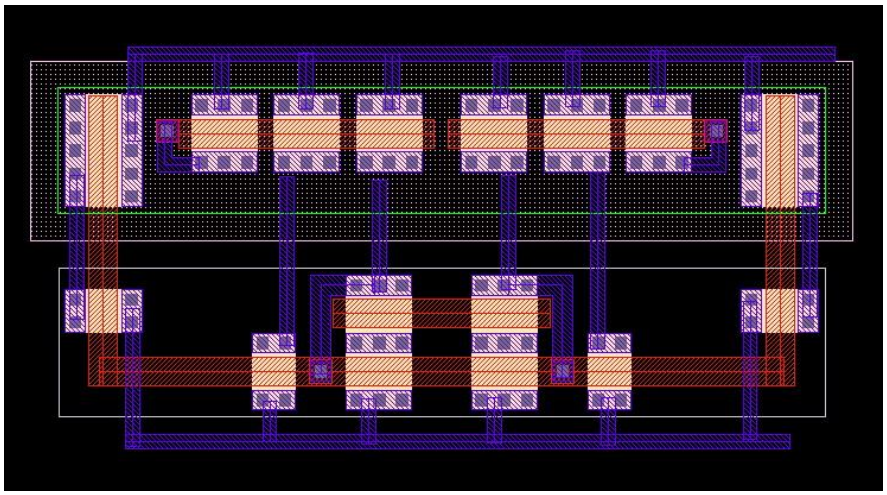

Fig. 4 Layout of the proposed WTA

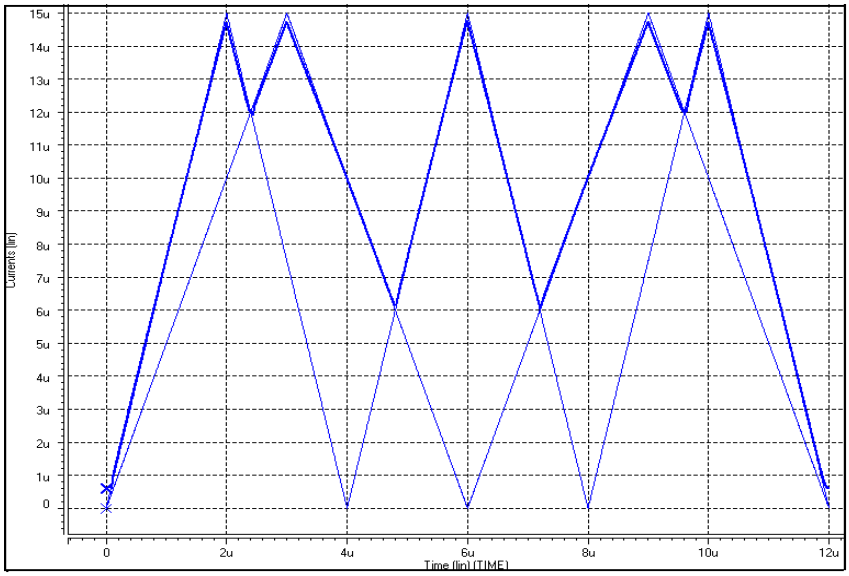

Fig .5 Transient simulation result for the proposed MAX circuit

Transient simulation result for the proposed MAX circuit is shown in Fig.5 where the output is indicated with solid lines.

Fig.6 shows the output transient response of the WTA circuit for two different currents.

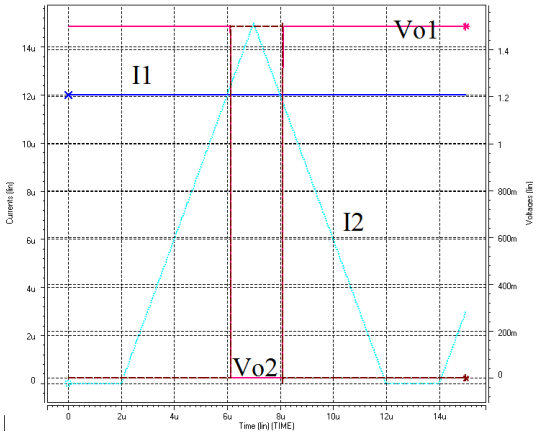

Fig. 6 Transient simulation result for the proposed WTA circuit

VI. Conclusions

A new, Low-voltage current mode multi input WTA circuit is described. The proposed circuit works with a single 1.5V power supply which makes it suitable for low-voltage portable application.

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References

[1] A. Fish, V. Milrud, O. Yadid-Pecht, "High-speed and high-precisioncurrent winner-take-all circuit", Circuits and Systems II: Express Briefs, IEEE Transactions on. Vol. 52, No. 3, 2005, pp. 131-135.

[2] J, Ramirez-Angulo, G. Ducoudray-Acevedo, R. G. Carvajal, A.Lopez-Martin, "Low-voltage high-performance voltage-mode andcurrent-mode WTA circuits based on flipped voltage followers",Circuits and Systems II: Express Briefs, IEEE Transactions on. Vol.52 , No. 7, 2005, pp. 420-423 .

[3] Y. Fang, M.A. Cohen, T.G. Kincaid, "Dynamic Analysis of aGeneral Class of Winner-Take-All Competitive Neural Networks",Neural Networks, IEEE Transactions on, Vol. 21, No. 5, 2010, pp.771-783.

[4] M. Rahman, K.L. Baishnab, F.A. Talukdar, "A high speed and highresolution VLSI Winner-take-all circuit for neural networks andfuzzy systems", Signals, Circuits and Systems, ISSCS. InternationalSymposium on. 2009, pp. 1-4 .

[5] S. Kazemi Nia, A. Khoei, Kh. Hadidi," High Speed High PrecisionVoltage-Mode MAX and MIN Circuits*," Journal of circuits, systemsand computer (JCSC)*, Vol. 16, No. 2, PP. 233-244, April 2007.

[6] R.G. Carvajal, A. Ramirez Angulo, J. Martinez Heredia," High-SpeedHigh-Precision Min/Max Circuits in CMOS Technology," *IEE Electron.Lett*. Vol. 36, NO. 8, PP. 697-699, April 2000.

[7] S. Vlassis and S. Siskos, High speed and high resolution WTA circuit, *Proc. 1999 IEEE Int. Symp. Circuits and Systems, ICAS'99,* Vol. 2, pp. 224–227.

[8] J. Ramirez-Angulo, G. Ducodray-Acevedo, R. G. Carjaval and A. Lopez-Martin, Low-voltage high-performance voltage-mode and current-mode WTA circuit based on flipped voltage followers, *IEEE Trans. Circuits Syst. II*, Vol. 52, July 2005.

[9] R. G. Carvajal, J. Ram´ırez-Angulo, A. L´opez-Martin, A. Torralba, J. Gal´an, A. Carlosena and F. Mu˜noz, The flipped voltage follower: A useful cell for low-voltage lowpower circuit design, *IEEE Trans. Circuits Syst. I*, Vol. 52, July 2005. roman