Reconfigurable Architecture of FPGA Based Image Compression Using DWT

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Abstract— A VLSI architecture designed to perform real-time image compression using wavelets is described. The efficient FPGA implementation of the 'Set Partitioning in Hierarchical Trees' (SPIHT) algorithm for compression of images. The SPIHT uses inherent redundancy among wavelet coefficients . In FPGA implementation the modified basic SPIHT in two ways, one by using static mapping which represent significant information and the other by interchanging the sorting and refinement passes. In this paper, a Modified SPIHT method suitable for image compression is used and hardware implementation is proposed. MSPIHT saves memory space and avoids dynamic dynamic management. The goal of this work is to obtain a lossless image compression by using DWT along with SPIHT algorithm . A hardware realization is done in a Xilinx XC3S200 device. The SPIHT algorithm can be applied to both grey-scale and colored images.

Keywords— Lossless compression, SPIHT algorithm, Wavelet transform, FPGA, Microblaze, soft-core, VHDL

I. Introduction

One of the major challenges in enabling mobile multimedia data services will be the need to process and wirelessly transmit a very large volume of data. One approach to mitigate to this problem is to reduce the volume of multimedia data transmitted over the wireless channel via data compression techniques. The grayscale images that are used in radiology applications. These images may be very large in size and number compression offers a means to reduce the cost of storage and increase the speed of transmission. Low bit rate image compression is essential for the storage of digital images. Today a lot of hospitals handle their medical image data with computers. The use of computers and a network makes it possible to distribute the image data among saff efficiently used.As the health care is computerized new techniques and applications are developed, among them the MRI and CT techniques.MRI and CT produce sequences of images (image stacks) each a cross-section of an object. The amount of data produced by these techniques is vast and this m ight be a problem when sending the data over a network. To overcome this the image data can be compressed. Low bit rate image compression is essential for the transmission and storage of digital images.

Existing Discrete Cosine Transform(DCT)-based compression algorithms such as uses JPEG standard where the need of memory usage much and occurs a problem of artifacts. But in Proposed system uses Wavelet transform with cutting edge technology provides good resolution of images. SPIHT is well for its simplicity but the memory requirement is large. The Modified SPIHT becomes a low memory resolution to SPIHT algorithm. MSPIHT also uses two strategies: firstly the number of error bit is proposed and used to merge the sorting and refinement passes, the error bits indicate the number of bits to be omitted finally, secondly an array is used to store the maximum value of coefficient of very zero sets.

The rest of the paper is organized as follows. In Section 2 explains proposed system using wavelet transform. Section 3,discuss the modified SPIHT algorithm are outlined. Section 4 explains simulation results. Section 5 discuss the Hardware Implementation, Section 6 discuss the Microblaze soft core processor, Section 7 discuss the design Flow and Section 8 discuss the conclusion.

II. Proposed System

DWT can be used to reduce the image size without losing much of the resolutions computed and values less than a pre-specified threshold are discarded. Thus it reduces the amount of memory required to represent given image wavelet Transform has become an important method for image compression. Wavelet based coding provides substantial improvement in picture quality at high compression ratios mainly due to better energy compaction property of wavelet

transforms. The digitized input image is characterised by its intensity values is given to DWT, where the conversion of bit coefficients occurs. The next step is quantization which converts a sequence of floating numbers into sequence of integers .Using physcovisual table the values are quantized to mear values. The next step is encoding where sequence of integers converted into shorter sequence. The goal of wavelet transform is advantage of taking redundancy in the transformed image and obtain good reconstruction in the decompression stage. The reverse process occurs in decoding stage. The output of decoding stage is given to IDWT, where the shorter sequence converted into bit coefficients and atlast the original image is reconstructed as the output image. The 1-D wavelet transform can be extended to a two-dimensional (2-D) wavelet transform using separable wavelet filters. With separable filters the 2-D transform can be computed by applying a 1-D transform to all the rows of the input, and then repeating on all of the columns shown in Fig.1

LL1	HL1
LH1	HH1

Fig.1 Subband Labeling scheme for a one level, 2-d wavelet transform

The 2-D subband decomposition is just an extension of 1-D subband decomposition. The entire process is carried out by executing 1-D subband decomposition twice, first in one direction (horizontal), then in the orthogonal (vertical) direction. For example, the low-pass subbands (Li) resulting from the horizontal direction is further decomposed in the vertical direction, leading to LLi and LHi subbands.

Similarly, the high pass subband (Hi) is further decomposed into HLi and HHi. After one level of transform, the image can be further decomposed by applying the 2-D subband decomposition to the existing LLi subband. This iterative process results in multiple "transform levels". In the first level of transform results in LH1, HL1, and HH1, in addition to LL1, which is further decomposed into LH2, HL2, HH2, LL2 at the second level, and the information of LL2 is used for the third level transform. The subband LLi is a low-resolution subband and high-pass subbands LHi, HLi, HHi are horizontal, vertical, and diagonal subband respectively.

To obtain a two-dimensional wavelet transform, the one-dimensional transform is applied first along the rows and then along the columns to produce four subbands: low-resolution, horizontal, vertical, and diagonal. (The vertical subband is created by applying a horizontal high-pass, which yields vertical edges.) At each level, the wavelet transform can be reapplied to the low-resolution subband to further decorrelated.

III. Modified SPIHT Algorithm

The powerful wavelet-based image compression method called Set Partitioning in Hierarchical Trees (SPIHT).The SPIHT uses partitioning of trees in a manner that tends to keep insignificant coefficients together in larger subsets.It has become the benchmark state-of-the-art algorithm for image compression. The SPIHT method is not a simple extension of traditional methods for image compression, and represents an important advance in the field.

The most important image energy is concentrated in low frequency components and the coefficients are expected to be better magnitude ordered one. A tree structure called Spatial Orientation Tree, naturally defines the spatial relationship of hierarchial pyramid. Each node of a tree corresponds to a pixel and is defind by the pixel coordinate.

The trees are again partitioned into four types of sets, which are set of coordinates of the coefficients:

O(i,j) This is set of coordinates of the off spring of the wavelet coefficients at location (i,j).

D(i,j) This is set of all descendants of the coefficient at location (i.j)

H This is the set of all root nodes.

L(i,j) This is the set of coordinates of all the descendants of of the coefficient at location(i,j).

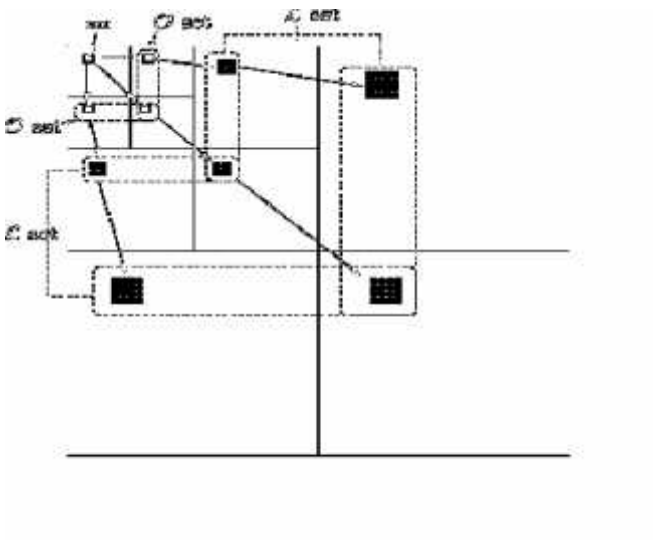

Fig.2 Spatial Orientation Tree

	Fishingboat.tif Original Size-257508 bytes			
Coefficients	Compressed size	Compression ratio	PSNR	MSE
1000	151952	1.69478	22.37	376.26
5000	195165	1.31944	25.52	182.23
15000	210591	1.22279	28.83	85.021
20000	213006	1.20892	29.95	65.738
25000	215930	1.19255	31.77	43.174

The algorithm make use of three lists:

LIP: The list of insignificant pixels.

LIS: The list of insignificant sets.

	Fishingboat.tif Original Size-257508 bytes			
Decomposition Level	Compressed size	Compression ratio	PSNR	MSE
3	48441	5.32	30.72	55.07
4	75970	3.39	33.54	28.78
5	83003	3.10	34.06	25.54
6	84513	3.05	34.19	24.80
7	84889	3.03	34.22	24.62

LSP: The list of significant pixels.

IV. Simulation Results

The proposed algorithm is implemented using MATLAB 7.0 .The visual quality and compression ratios are better when considered with DCT.The modified SPIHT algorithm is greatly enhance the algorithm iteration's efficiency. Hardware is modeled using VHDL under Xilinx ISE 9.1i,XST is used to compile VHDL code code and generate the net list. xilinx ISE 9.1 is used to place and route the design on XC3S200.

TABLE I

Performance Evaluation of DWT-SPIHT Algorithm

TABLE II
Performance Evaluation of DCT

V. Hardware Implementation

The FIELD-PROGRAMMABLE GATE ARRAYS (FPGA's) are flexible and reusable high-density circuits that can be easily re-configured by the designer, enabling the VLSIdesign / validation /simulation cycle to be performed more quickly and less expensive. Increasing device densities have prompted FPGA manufacturers, such as Xilinx and Altera, to incorporate larger embedded components, including multipliers, DSP blocks and even embedded processors. One of the recent architectural enhancements in the Xilinx Spartan, Virtex family architectures is the introduction of the MicroBlaze (Soft IP) and PowerPC405 hard-core embeddedprocessor (1l].The MicroBlaze processor is a 32-bit Harvard Reduced Instruction Set Computer (RISC) architecture optimized for implementation in Xilinx FPGAs with separate 32-bit instruction and data buses running at full speed to execute programs and access data from both on-chip and external memory at the same time.

VI. Microblaze Soft Core Processor

The cluster based multiprocessor system on chip architecture can be designed using cores provided by the microblaze controller and Spartan 3e kit. Micro blaze is a 32 bit soft core IP for a Xilinx based FPGA system design. It is highly configurable depends on the architecture being used. Microblaze has an orthogonal instruction set architecture. It has thirty-two 32-bit general purpose registers and up to eighteen 32-bit special purpose registers, depending on configured options . An interrupt controller is available for use with the Xilinx Embedded Development Kit (EDK) software tools. The processor will only react to interrupts if the Interrupt Enable (IE) bit in the Machine Status Register (MSR) is set to 1. On an interrupt the instruction in the execution stage will complete, while the instruction in the decode stage is replaced by a branch to the interrupt vector (address Ox 10). The interrupt return address (the PC associated with the instruction in the decode stage at the time of the interrupt) is automatically loaded into general-purpose register.

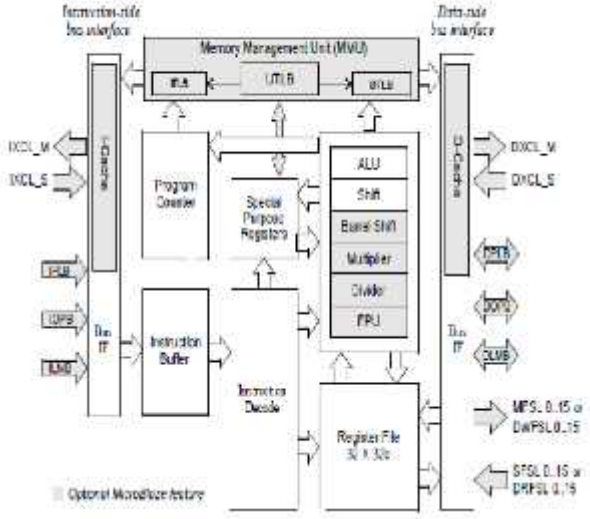

Fig 3. Microblaze Architecture Block diagram

VII. Design Flow

The Xilinx Company provides the suite of tool called EDK as well as IP that enables us to design a complete embedded processor system for implementation in a Xilinx FPGA device. This tool is used to create the hardware system using the Microblaze soft core processor along with require features depends upon the application of the hardware. EDK includes a variety of tools and applications to assist the designer to develop an embedded system right from the hardware creation to final implementation of the system on an FPGA. System design consists of the creation of the hardware and software components of the embedded processor system and the creation of a verification component is optional. A typical embedded system design project involves: hardware platform creation, hardware platform verification (simulation), software platform creation, software application creation, and software verification. SDK is built on the Eclipse open source framework, complimentary to XPS that is used for C/C++ embedded software application creation and verification.The software application can be written in a "C or C++" then the complete embedded processor system for user application will be completed, else debug & download the bit file into FPGA. Then FPGA behaves like processor implemented on it in a Xilinx Field Programmable Gate Array (FPGA) device.

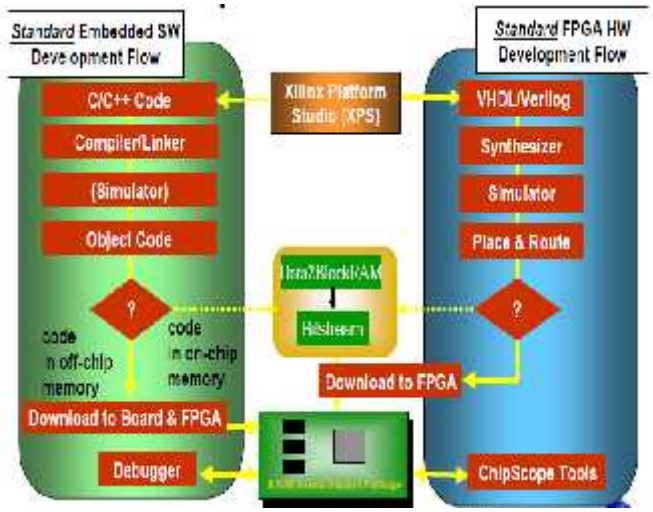

Fig 4. Design Flow

VIII. Conclusion

In this paper, a DWT-based reconfigurable system is designed using the EDK tool. Hardware architectures of two dimensional (2-D) DWT have been implemented as a coprocessor in an embedded system. A new algorithm to image compression is considered. The model involved modification for incorporating the parallism technique to basic SPIHT algorithm. The memory utilization is minimized and throughput is increased. Here some parameters compared such as PSNR, MSE, Compression ratio along with the existing system DCT.

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