VHDL Implementation of Viterbi Decoder by Butterfly Module

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Abstract: **Viterbi Decoder is widely used as decoder of convolution encoder which is used for error correcting communication. Main drawback of Viterbi decoder is its complexity which is increase exponentially with $2^{(K-1)}$. For Viterbi Decoder each time $2^{(K-1)}$ Branch Metrics are required to calculate. But if symmetric property of Viterbi decoder is used than computation can be reduced by factor 4 for one module. To use this symmetric structure, Viterbi decoder is required to implement by Butterfly Module which is given in this paper.**

Keywords: **convolution encoder; trellis diagram, viterbi decoder; butterfly module.**

I. INTRODUCTION

In communication system, data receive at receiver side must be error free. For error free communication two types of techniques are used. One is error detection technique in that extra redundant bits are transmitted. Receiver checks the redundant bits and receives data. If it found data is not correct than it give acknowledgement to transmitter and transmitter send the same data again. This technique is useful in low noise channel. But this technique is consuming more bandwidth in noisy channel as it requires re-transmitting of data frequently. Second method is error correction in which redundant bits are use for correcting data at receiver. In this technique all time redundant bits are transmitted so this is not effective at low noise area. But it is very effective in high noise area. For error correcting code convolution encoder is widely used as it can also correct burst errors. And to decode convolution encoder Viterbi decoder is used at receiver side which gives error correcting output. This paper contains introduction of convolution encoder and Viterbi decoder as well as implementation of both using VHDL.

II. CONVOLUTION ENCODER

Convolution Encoder is used at transmitter side for error free communication and as error correcting code. Convolution encoder output is depending on present input as well as past input given to the encoder. As it is depend on past input memory elements are required to implement it. Output is generated by EX-OR of related input. Main parameters of convolution encoder are number of input (k), number of output (n), and constraint length (K). In this paper parameters of convolution encoder are k=1, n=3, K=5. Data rate of convolution encoder is k/n (1/3). Design of convolution encoder is given in figure-1.

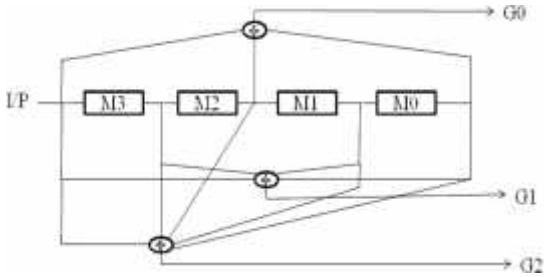

Fig 1 Convolution Encoder

III. TRELLIS DIAGRAM

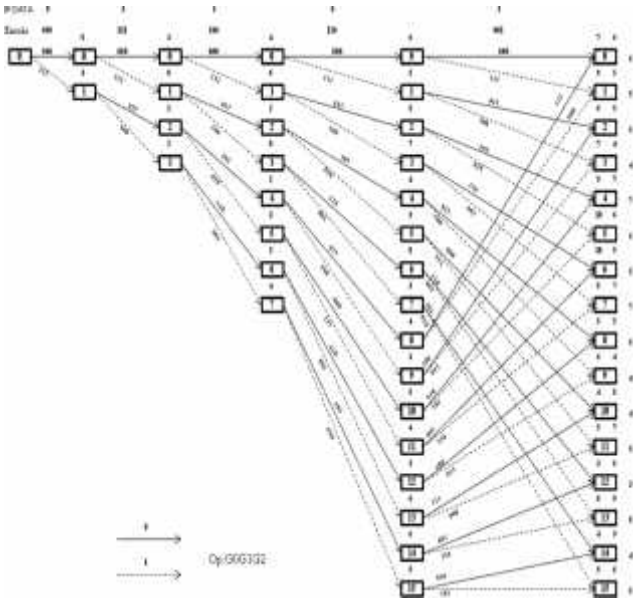

Fig 2 Trellis Diagram

As shown in figure-2 trellis diagram is used to represent convolution encoder each state with input. It represent present state, input and after that next state when applied that particular input. Trellis diagram is used for Viterbi decoder in which optimum path is finding out. After that using that optimum path decoded output means error correcting original data is received. Trellis diagram contain $2^{(K-1)}$ different states. Here value of K=5 so total no of states are 16 as shown in figure. In this way as constraint length (K) increase, complexity of trellis diagram increase exponentially.

IV. BLOCK DIAGRAM OF VITERBI DECODER

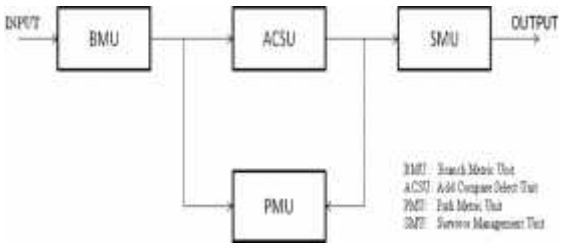

Fig 3 Block Diagram

Branch Metric Unit (BMU):
BMU unit is the first block of Viterbi decoder. In this block received data symbol is compare to the ideal output of the encoder from the transmitter and branch metric is calculated. Hamming distance and Euclian distance can be useful to calculate Branch Metric computation. Due to easy use of hamming distance it is more use for calculation of BM.

Path Metric Unit (PMU):
PMU is useful to calculate Path metric of a stage by adding the Branch Metric to associate path metric from the previous stage of trellis.

Add Compare & Select Unit (ACSU):
ACSU unit is used to compare input from Path metric unit and select optimum path metric for each state. And that Path metric is used for calculation of next stage path metric.

Survivor Memory Management Unit (SMU):
SMU is final unit of Viterbi decoder. It is used to decode the input data. This unit can be implemented by two techniques 1) TB method 2) RE method.

1. Trace Back (TB) Method:
In the TB method, the storage can be implemented as RAM and is call the path memory. Each stage survivor path is stored in RAM. After L branches have been proceeding, the trellis connections are recalled in reverse order and the path is trace back through the trellis diagram. TB method extract the decoded bits, beginning from the state with minimum PM, Beginning at this state and tracing backward in time by following survivor path, which originally contributed to the current PM. A unique path is identified. While tracing back through the trellis, the decoded output sequence, corresponding to the traced branches is generated in reverse order. The trace back method limits the speed of decoding.

2. Register Exchange Method:
In register exchange method, a register assigned to each state contain information bits for the survivor path from the initial state to the current state. In fact register keeps the partially decoded output sequence along the path. In this register exchange method is faster than trace back method. In this paper Viterbi decoder is implemented by register exchange method.

V. BUTTERFLY MODULE

Trellis diagram has symmetric property means that two states have same next states for different input. And branch metrics of both states are also same. One branch metric is complement of other one. So using this property computation of branch metric can be reduced by factor 4. For that all states are required to group into symmetric states. One example of butterfly module is shown in figure-4. As shown in figure for S0 and S8 state, if input is 0 than next state is S0 and if input is 0 than next state is S1. And only branch metric for "000" is required to calculate.

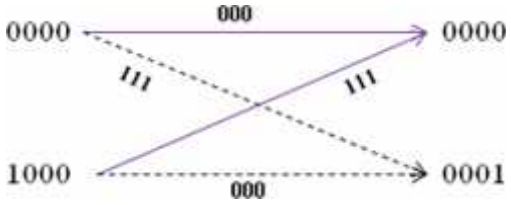

Fig 4 Sample Butterfly Module

VI. RESULT

1. Convolution Encoder Module:
As shown in figure-5 first cycle is used for reset the encoder. At that time all flip flop and other variable reset to the initiate value. After that in next 8 cycle input sequence is "01101010" according to that convolution output is generated. In first state instead of output "000",encoder give output "001" to show noise effect.

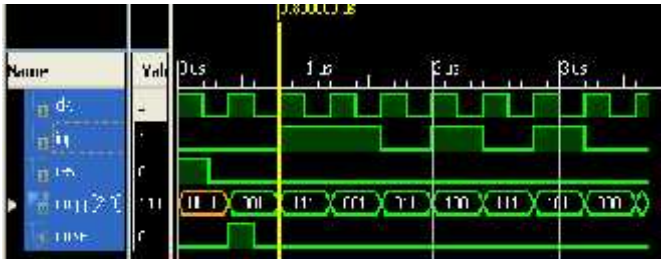

Fig 5 Convolution Encoder

2.Butterfly Module-0:

In figure-5, previous path metric(IMETU) and path metric after calculation(OMETU) is given.In this way all butterfly module output can be calculated.

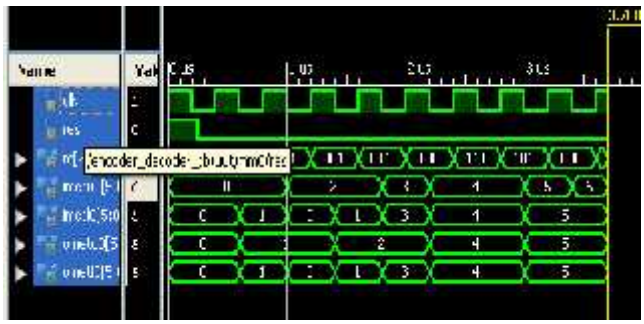

Fig 6 Butterfly Module

3.Viterbi Decoder Output:

In figure-6 Viterbi decoder output is given. Output under highlighted circle "01101010" is decoded output sequence which is matched with input sequence.

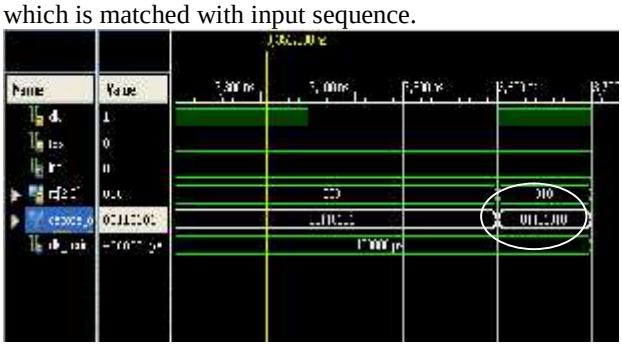

Fig 7 Viterbi Decoder Output

VII. CONCLUSION

From this implementation of Viterbi decoder using butterfly module, it is concluded that computation complexity if Viterbi decoder can be reduced by using butterfly module. Total 24 computations for branch metric are not required in butterfly module. And it is also clear that Viterbi decoder can correct error as shown in results. So convolution encoder and Viterbi decoder can be useful for error correcting.

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