Designing of A new Low Voltage Low Power Tunable Fuzzy Logic Controler Chip

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Abstract— In this paper we design a new Fuzzy Logic controller (FLC) chip with mixed-signal input and analog output. The analog fuzzy engine is based on a novel current-mode CMOS circuit used for the implementation of fuzzy partition membership functions. These membership functions are simply tunable by setting some voltages and currents on IC pins. Input has three membership functions and output is five singleton membership functions.. The controller is tested for two inputs, one output, and nine tunable fuzzy rules. The proposed circuit was laid out standard 0.18 μm CMOS technology. Post layout simulation from extracted circuit were performed for a 1v single power supply voltage using HSPICE software. Power consumption of circuit is 7.2mv.

Index Terms— CMOS FLC chip, Fuzzifier , Min operator, Nonlinear systems, Current mode circuits

1. INTRODUCTION:

In fuzzy systems there are three main steps: (1) fuzzification (membership function generation), (2) fuzzy inference or fuzzy rule evaluation, and (3) defuzzification. Excellent tutorial overviews on a utility of a fuzzy system and its application have been reported in many articles. A Gaussian or triangular function is normally used in the fuzzification process. The second step, fuzzy rule evaluation or fuzzy inference, uses a technique called min-max inference to calculate numerical values representing the truth for certain consequent action based on a set of rules bearing the consequent. The defuzzification step is a process of combining all fuzzy outputs in a specific, crisp result that can be applied to each system output.

For this reason many analog hardware implementations of fuzzy engines are reported in the many literatures. The current-mode fuzzy engine proposed in [1] implements the normalization condition using a feedback loop, which forces the input membership functions to realize a partition. In [2] some Membership Function Circuits (MFCs), with a piecewiselinear characteristic, are proposed. Similarly, [3] proposes a triangular/trapezoidal MFC. However the main lack of those approaches is that the output of the fuzzy system is non-smooth. A tunable voltage-driven MFC has been proposed in [4], implemented using a source-degenerated differential pair, and in [5] a similar MFC is coupled with a custom inference engine. Likewise, [6] presents some fuzzy engines with differential-pair based MFCs, adopting the min-max inference method, with either normalization based or division based defuzzyfication.

The mixed-signal implementation of a fuzzy controller, presented in this paper for general application. The architecture of the analog fuzzy engine uses fuzzy partition membership functions. This kind of membership functions needs to respect the orthogonality condition, that is implemented by analog circuits. This condition leads to a strong simplification of the architecture of the complete fuzzy engine. The solution adopted in this work for the implementation of the membership functions is based on current-mode CMOS circuits. The architecture has been designed and implemented in a 0.18µm CMOS technology with a 1v supply voltage. The paper is organized as follows. Section II reports the current-mode proposed flc chip. This section introduces block diagram of proposed chip and proposed fuzzifier circuit and also explains minimum circuit, current mirror system and eventually describes current-voltage divider. Section III shows the system simulation with MATLAB. Finally, Section 5 describes the architecture of the mixed signal programmable fuzzy controller and contains a description of other analog circuits of the chip.

2. PROPOSED FLC CHIP

2.A. Main Block Diagram of Controller

Considering to Figure. 1 and according to the Fig. 2.a and Fig. 2.b all blocks of proposed system are shown which consist of two inputs (each input has three membership functions) and one output with 5 singletons (NN, N, Z, P, PP) using COA for defuzzifying, Min circuit for combining antecedent of each rule, product-sum inference method for performing system deduction with current mode divider to produce analog outputs.

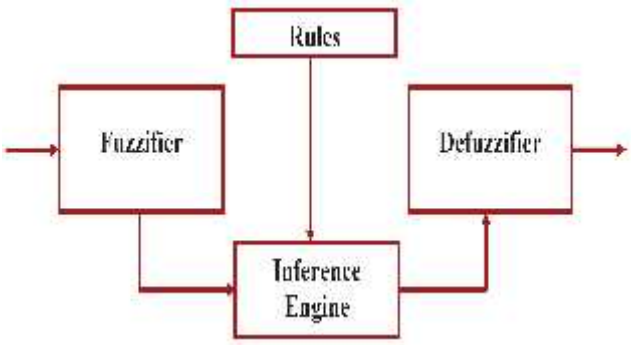
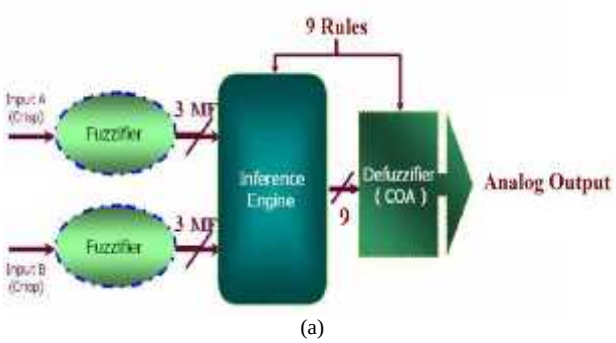
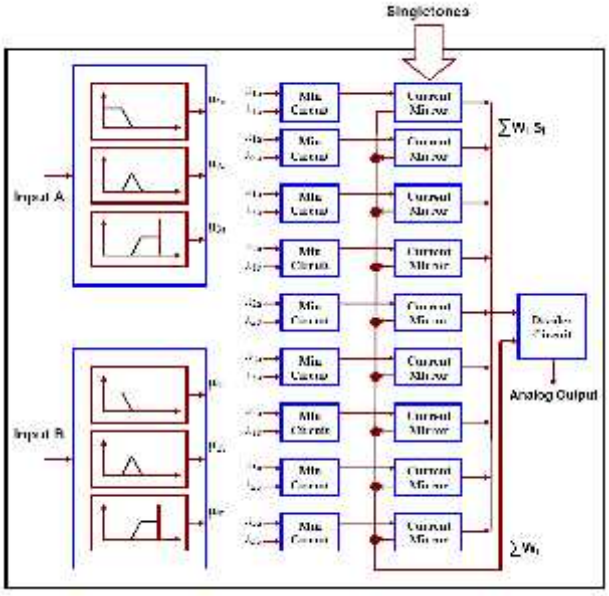


Figure 1. Main block diagram of a controller



(a)



(b)

Figure 2. a)Block diagram of proposed controller b)Design of propose chip

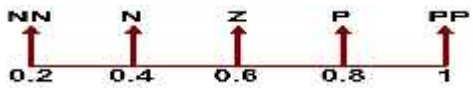


Figure 3. Defenition Singletons(v)

2.B. Fuzzifier (Circuit Design)

The main new integrated circuit to implement Fuzzifier block is shown in Fig. 4. It's clear on the figure of circuit that $I_{b2}=I_{m2a}$ and according to that I_b is fixed so V_{GSm2a} must remain constant and any chandes of V_{in} are passed to sourse terminal.

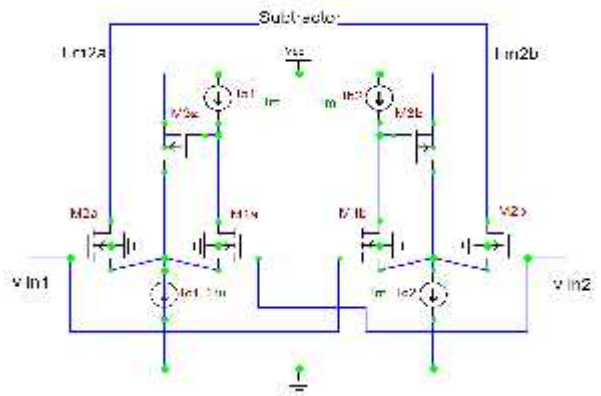


Figure 4. Proposed Fuzzifier circuit

So we have following relations :

$$I_{b2} = K_n (V_{in1} - V_{Sourse} - V_{th})^2 \quad (1)$$

$$V_{Sourse} = V_{in1} - V_{th} - \sqrt{I_b / K_n} \quad (2)$$

$$I_{m2a} = K_n (V_{in2} - V_{Sourse} - V_{th})^2 \quad (3)$$

$$I_{m2a} = K_n (V_{in2} - V_{in1} + \sqrt{I_b / K})^2 \quad (4)$$

And likewise :

$$I_{m2b} = K_n (V_{in1} - V_{in2} + \sqrt{I_b / K})^2 \quad (5)$$

$$I_{out} = I_{m2a} - I_{m2b} \quad (6)$$

$$I_{out} = 4\,k \sqrt{I_b / K_n} \; (V_{in2} - V_{in1}) \quad (7)$$

Fig. 5 shows I_{out} proportional with $V_{in1.}$ In Fig. 4 V_{in2} and I_b (W/L) are tunable voltage and current for start point and slope of curve.

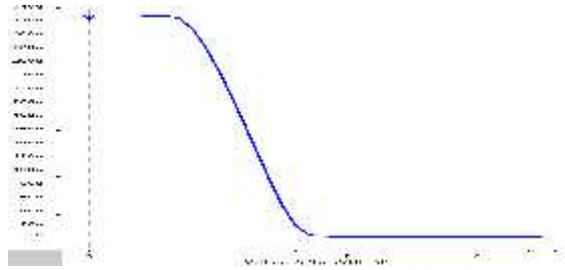
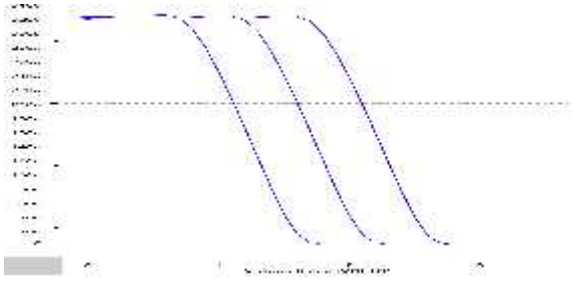
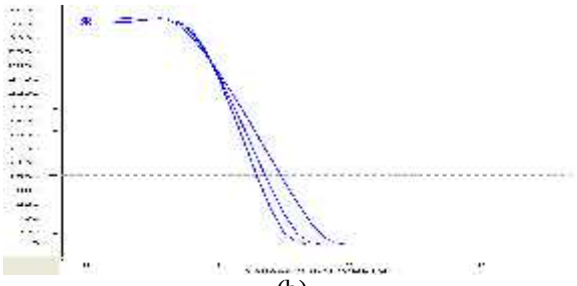


Figure 5. First membership function of fuzzifier



(a)



(b)

Figure 6. a)Tuning of membership function with Vin2 b) Tuning of membership function with Ib or w/l

For product triangle or trapezoidal membership function we need a minimum circuit. It is introduced in next chapter. Before it must adjust V_{in2} and I_b appropriately.

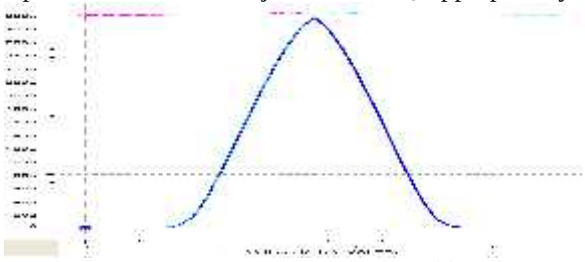


Figure 7. Triangle membership function of fuzzifier

Finally total membership function shows in Figure. 8.

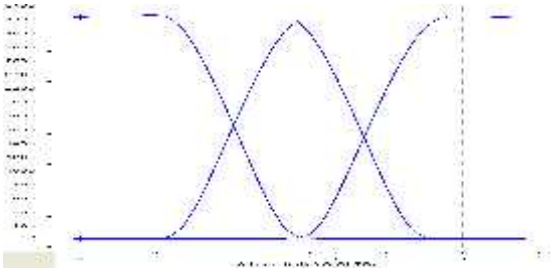
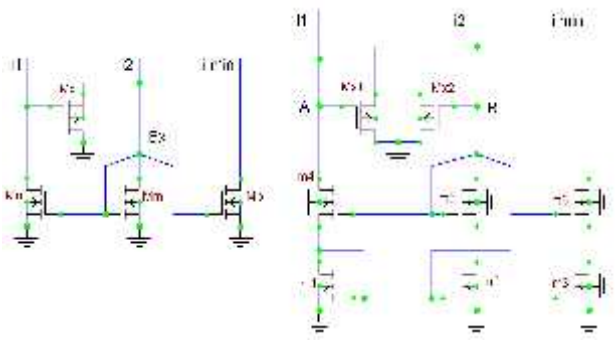


Figure 8. Total membership functions of propose fuzzifier

2.C. Minimum Circuit

Our used connective for compounding antecedents are "AND" operator which is implemented with Min circuit. Fig 9.a shows foundation of circuit behavior that using simple current mirror, there is an individual way for I_1 to pass through, which is the transistor M_1. Moreover, there is an individual way for I_2 to pass through, which is the transistor M_2. Transistor M_3 takes extra current of (I_2-I_1) when I_2>I_1. The drawback of this circuit is the unsymmetrical reflection in output when I_1>I_2. To complete this idea and conquer the problem, we came up with idea which includes using Wilson current mirror and two PMOS transistors as shown in Fig 3b. If I_1>I_2, the voltage of node A and B will be high and low respectively. It causes that M_{x1} turn on and M_{x2} goes to the cut off region. Therefore the extra current of (I_1-I_2) goes through M_{x1} which results the reflected current in output as minimum current (I_{min}=I_2). In another way of I_2>I_1, we have the like mentioned results except that M_{x2} turn on and M_{x1} enter to the cut off region. Even though the mentioned proposed Min circuit is simple, it has high DC current rang, high accuracy and low devices in comparison before works [7], [8], and [9].



(a) (b)

Figure 9. a) Main idea of min circuit b) Structure of proposed min circuit

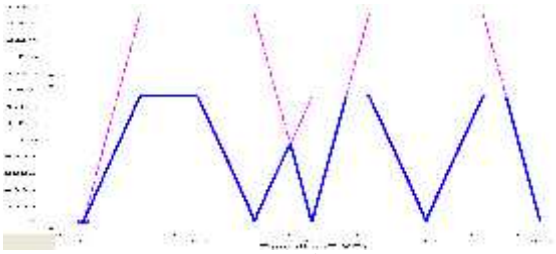


Figure 10. Simulation of minimum circuit

2.D. Current Mirror Circuit

In this chapter introduce a current mirror circuit. Because defuzzifier block is required to product relation $\frac{\sum W_i * S_i}{\sum W_i}$ so numerator of this relation ($\sum W_i * S_i$) is required to a circuit for multiply S_i and W_i. To achieve this, a current mirror circuit can be used accordance with the following circuit :

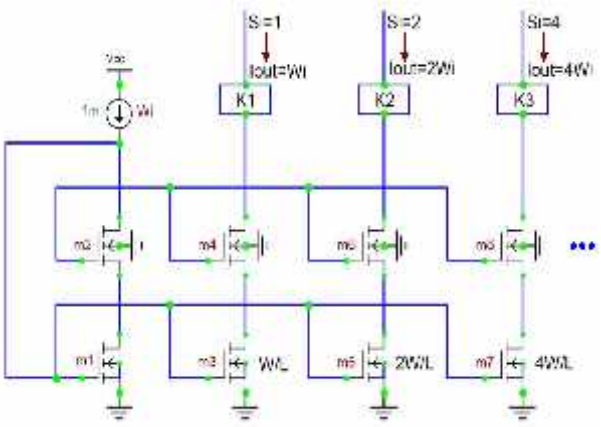


Figure 11. Circuit of Current Mirror

In this figure K_1, K_2, K_3 and … are switch of open/short contact, Also increase W/L in m3, m5, m7, ... causes the I_{out} proportional W/L be multiplied**.**

$$I_{out} = W_i \; S_i = n \; W/L \; W_i \qquad (8)$$

In Figure 12 W_i is 0.2ma and I_{out} for W/L, 2W/L, 3W/L, 4W/L and 5W/L is calculated.

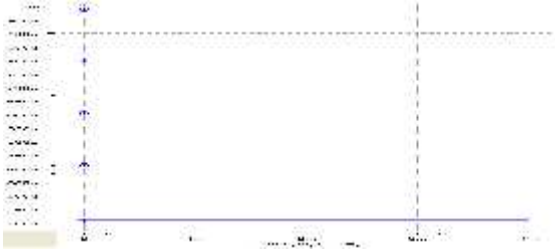


Figure 12. Calculated of Current Mirror Circuit

2.E. Divider Circuit

In this section for division $\sum W_i * S_i$ and $\sum W_i$, a divider circuit is introduced.

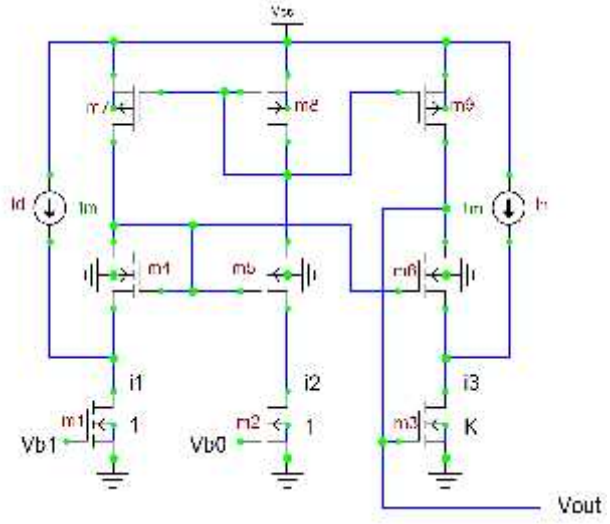


Figure 13. Circuit Of Current-Voltage Divider

In this figure transistors in right column are k times scaled with respect to their homologues at each row, as shown at the bottom of the figure. The division is performed by means of transistors m1, m2, m3 at the bottom layer, all of the being constrained to operate in the triode region. The drain-to-source voltage dropes Vds of those transistors are matched ttanks to (GVO) are identical. This is guaranteed by the upper PMOS mirrors (m7 to m9), which replicate the current I_2 to the left branch and the scaled current $k*I_2$ to the right branch.
While V_{b1} and V_{b0} are fixed bias voltages, the gate voltage V_{out} of transistor m3 is self-adjusted so that the drain current of m6 match the current imposed by m9. In this way, the following relations hold for the drain currents of the triode transistors :

$$I_1 = \beta V_{ds} (V_{b1} - V_{th} - n/2\ V_{ds}) = I_D + I_2 \quad (9)$$

$$I_2 = \beta V_{ds} (V_{b0} - V_{th} - n/2\ V_{ds}) , \quad (10)$$

$$I_3 = k \beta V_{ds} (V_{out} - V_{th} - n/2\ V_{ds}) = I_N + aI_2$$

Where V_{ds} is the common drain-to-source voltage drope for the three bottom transistors while β is the current gain ratio of m1 and m2. Therefore, upon ideal matching conditions, from the latter three equation we can write :

$$(V_{out} - V_{b0}) = \frac{(V_{b1} - V_{b0})}{k} \frac{I_N}{I_D} \quad (11)$$

Thus, if V_{out} is referred to V_{b0}, we obtain a two-quadrant divider. Given the desired current ranges of I_N and I_D, the maximum output voltage swing is defined by the difference $(V_{b1} - V_{b0})$ and the scaling factor k, which must be chosen accordingly.
Whenever a voltage-mode external output interface is required, the performing internally current-mode analog computations. Hence, there is no need for extra interfance converter circuits neither at its inputs nor at the output.
Figure 13 shows V_{out} proportional with I_N.

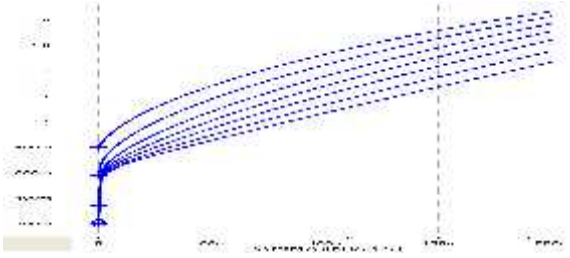


Figure 14. Simulation of Current-Voltage Divider

3. SYSTEM SIMULATION

After extracting the file of circuit layout, all file of blocks were simulated using Hspice software and All of its are shown in relevant sections. In defined model input membership functions, two crisp inputs of A and B in which there are three language terms (Poor, Good, Excellent) are assumed to be as the shapes shown in Fig. 15. It illustrates the obtaining systematic control surface using Matlab software too in Figure 17. Figure 16 shows the 9 rules of inference engine.

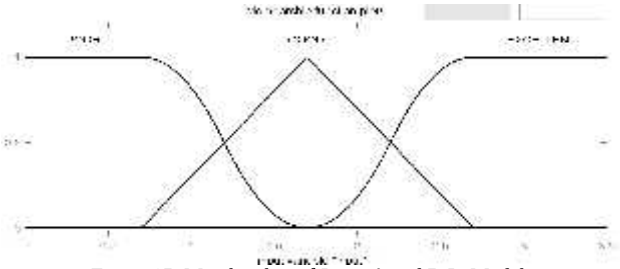


Figure 15. Membership of Input A and B In Matlab

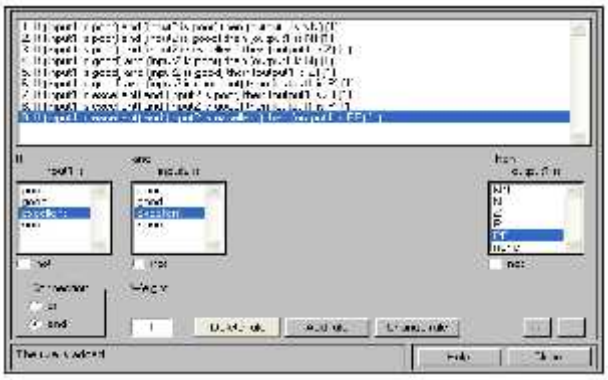


Figure 16. The systematic control surface of controller using Matlab

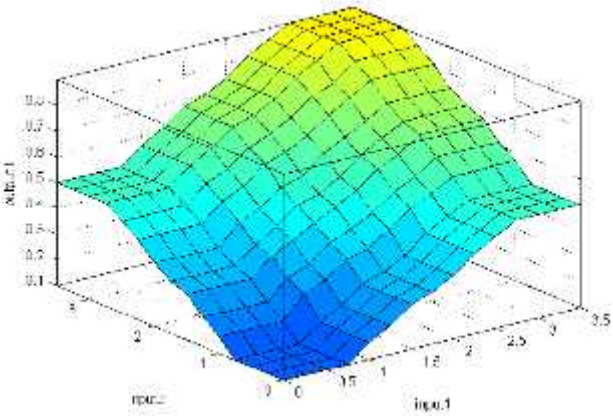


Figure 17. The systematic control surface of controller using Matlab

In Figure 16 NN, N, Z, P and PP are the compact of rules with output linguistic terms as singleton that have 5 terms VS (Very Small), S (Small), M (Medium), L (Large) and VL (Very Large). Tables I to III show a compact of the rules with output linguistic terms as singletons (Fig. 3) that have 5 terms.

Table 1. Fuzzy Rulles (Singletones)

A \ B	Poor	Good	Excellent
Poor	NN	N	Z
Good	N	Z	P
Excellent	Z	P	PP

Table 2. Fuzzy Rulles (Dedicated Numbers)

A B	Poor	Good	Excellent
Poor	0.2	0.4	0.6
Good	0.4	0.6	0.8
Excellent	0.6	0.8	1.0

4. CONCLUSION

Presented in this paper was based on using analog circuit realization in order to increase inference speed and capability of employing more accurate inference and defuzzifying methods with the least circuit complexity.
This controller including new and improved integrated CMOS circuit of Fuzzifier, Min operators, Current mirror and current mode Divider with voltage output can be implemented in 0.18µm CMOS standard technology with 1v supply voltage. The distinctive features of proposed mixed-signal input and analoge output controller are summarized as fallow:

1. Proposed fuzzifier circuit provides maximum controllability, simple circuitry and having different shape types in compare to [9, 10].
2. Higher DC rang and accurate for Min circuit in comparison works [8].
3. Low suplly voltage.
4. Low power consumption.
5. Less number of used transistors in compare to most references.

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