IEEE 802.3 MAC Transmitter Using FSM and VHDL Techniques

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ABSTRACT- **The purpose of this paper is to design and implementation a MAC Transmitter on Field Programmable Gate Arrays (FPGA) that converts 32 bit data in to 4 bit DATA for transmitter. In this paper we design the Ethernet (802.3) connection oriented LAN Medium Access Control Transmitter (MAC). It starts by describing the behavior of MAC circuit using VHISC Hardware Description Language (VHDL).. The MAC layer is works between Logical link layer and physical layer. It starts by describing the behavior and blocks of MAC Transmitter.**

***Keywords*— Local Area Network (LAN), Logical Link Control(LLC), Medium Access Control(MAC), Linear feed Back Register,VHISC Hardware Description Language (VHDL).**

I. INTRODUCTION

General Standard for the Data link layer in the OSI reference model. IEEE 802.3 Standard related to Media Access Control Layer defines the MAC layer for bus networks that use CSMA/CD. This is the basis of the Ethernet standard. The following section goes into greater detail explaining how the CSMA/CD standard functions and how it enables the network to transmit data efficiently and with very few errors. As was explained earlier, CSMA/CD allows machines to send and receive data any time it senses that the network is inactive. If two stations attempt to transmit simultaneously, this causes a collision, which is detected by all participating stations.

After a random time interval, the stations that collided, attempt to transmit again. If another collision occurs, the time intervals from which the random waiting time is selected are increased step by step. This is known as exponential back off.

However effective coding style optimizes FPGA resource allocation for area and speed performance of IEEE 802.3 MAC transmitter can be using linear feedback shift register, one hot finite machine (FSM) state encoding style.

II. MAC INTERNAL ARCHITECTURE

MAC transmitter internal architecture shown in below Fig1.The MAC internal architecture consists of major five blocks.

- DEFER
- BACKOFF
- TRANSMITTER
- FRAME ASSEMBLER
- CRC

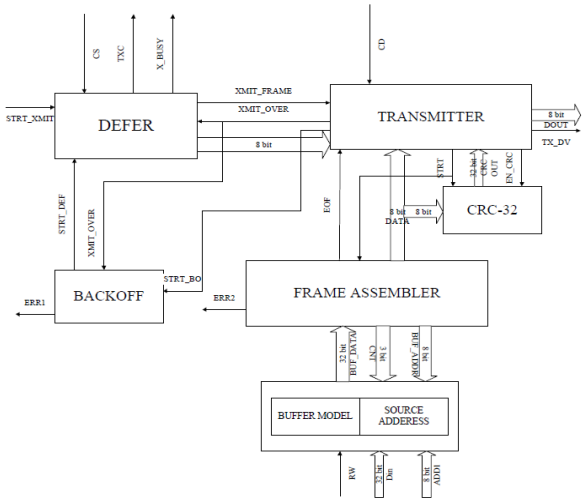


Fig1. Internal Architecture of MAC Transmitter

III. DEFER

The Defer block function providing the inter frame gap period between the two frames. It continuously deferring whenever the physical line is busy. The Defer block continues monitors the carrier sense (CS) signal provided by the physical layer and whenever the medium is busy, it defers the transmission. It provides the inter frame gap period which is 96 bit.

On Receiving the „STRT_XMIT‟from the upper layer (LLC) this block makes the „X_BUSY‟ signal active and starts the process of monitoring the channel for „CARRIER SENSE‟ is provided by the Physical layer. It monitors the channel for inter frame gap period, which is 96 bit period. The Period is split in to two different time slots 60 bit period and 36 bit period. During the 60 bit period if it receive the CARRIER SENSE‟ as active then the timer is restarted. After 60 bit time period is elapsed ,The transmitter does not monitor „CARRIER SENSE‟ for next 3 bit period and gives the signal XMIT_FRAME‟.Once the transmission is started it waits for „XMIT_OVER‟ or „STRT_DEF‟ to be asserted and goes to start of defer when either is asserted.

IV. BACKOFF

When a Transmission attempt has been terminated due to collision, it is retired by the transmitting Data Link until it is successful or attempts 16 (the original attempt plus 15 retries) have been made and all have terminated due to collisions.

The scheduling of the retransmission is determined by a controlled randomization process known as „Truncated Binary Exponential Back Off”. After the end of enforcing a collision (Jamming), the transmitter delays before attempting to retransmit the frame. The delay is an integer multiple of slot time. The number of slot times to delay before the nth retransmission attempts is chosen as a uniformly distributed random integer r in the range

$$0 <= r <= 2^k$$

Where, K=min (n, 10)

If all attempts fail, this event is reported as an error.

V. TRANSMITTER

On Receiving STRT_XMIT active from DEFER block start transmitting 4 bits at a time. At the same time it gives signal TRANSMIT_VALID (TXDV) to the physical layer. First it transmits 7-bytes of PREAMBLE then 1 byte of SFD (Start Frame Delimiter) is transmitted and it also gives STRT signal to the Frame Assembler block and CRC block. After that it accepts 8-bit of data from Frame Assembler. Then it transmit 32-bits of CRC and gives the signal TRANSMIT OVER(XMIT_OVER) to Defer block and de-asserts the signals TXDV and STRT.Since CRC block work on bytes, Frame assembler gives 8-bits of data at the output.

Whereas transmitter gives nibble at the output so it reads from FRAME ASSMBLER after two clock cycles. Frame assembler also gives the output on every two clock cycles. The block also monitors the signal Collision detect (CD) provided by the physical layer. If it detects CD during transmitting PREAMBLE (sequence 1010101010) and then it transmits 4 bytes of JAM Sequence (11111111) .It also asserts the signal Strt_BO and de-assert signal STRT.

VI. FRAME ASSEMBLER

The Function of a frame assembler is to assemble a different component of the frame, viz.destination address, source address, length/Type and data, and supply this to the transmitter as well as the CRC block. Hence, the assembler assembles all the fields over which FCS is determined.

The destination address is the MAC address of the machine to which the particular frame is to be delivered. Each NIC (Network Interface Card) has a unique MAC address. It is this address that is part of the destination address field, which is a 6 byte or 48-bit address.

The function of a frame assembler is to construct the 802.3 frame from the following

1. Destination address stored in first 6 bytes of buffer.
2. Source address that is hardwired onto the MAC.
3. Length stored in the lower word of the second location of buffer.
4. Data bytes stored in the subsequent buffer location.

5. Pad bytes if length is less than 46 bytes to make up a total of 46 bytes of data and pad.

Hence the frame Assembler is tested as follows :-

1. The buffer is filled with some destination address and a length. A source address is also stored in its register.
2. The subsequent buffer location are filled with randomly generated data vectors .
3. The frame assembler is activated by the STRT signal.
4. The byte output of the frame assembler is stored into an output file through textio
5. The frame generated is analyzed to isolate its individual components viz. destination Address, Source Address, Length data + Pad. Each field is verified for correct operation.

The total length of the data must match the length specified in the length field for length between 46 and

1500,where as it should be 46 bytes including data and padding for length field or less than 46. if the length specified is greater than 1500 the frame Assembler should generate an error condition and exit. The Frame Assembler is tested for the following length Conditions Length=0, Length<46, Length=46, Length>46,and <1500 Length =1500, Length <1500.

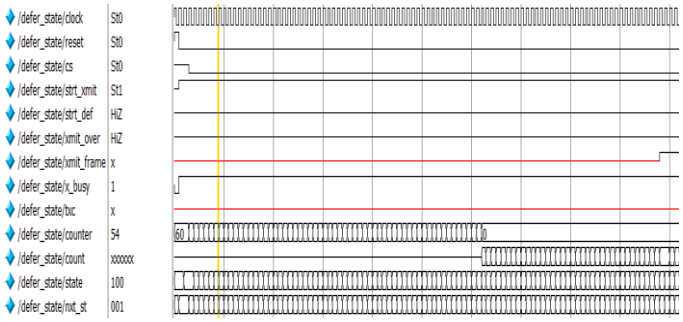
VII. CRC GENERATOR

A Cyclic Redundancy Check (CRC) is used by the transmit and receive algorithms to generate a CRC value for the FCS field. The Frame Check Sequence (FCS) field contains a 4-octet CRC value. This value is computed as a function of the contents of the Source address, Destination Address, Length, LLC Data and PAD. The encoding is defined by the following generate polynomial [1].
G(x)=X32+X26+X23+X22+X16+X12+X11+X10+X8+X7+ X5+X4+X2+X+1 [1]

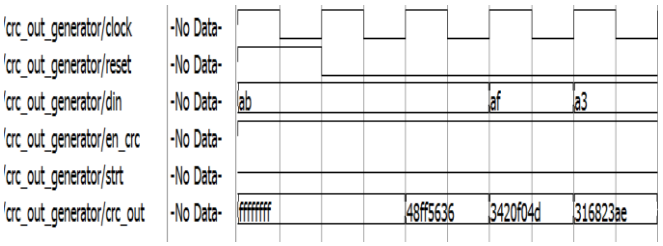
Mathematically, The CRC value corresponding to a given frame is defined by the following procedure.

1. The first 32 bits of the farm are complemented.
2. The n bits of the frame are then considered to be the coefficient of a polynomial M[x] of degree [n-1]. (The first bit of the destination Address field corresponds to the X (n-1). term and last bit of data field corresponds to the X term)
3. M (x) is multiplied by X32 and divided by G (x) , producing a remainder R(x) of degree < 31 .
4. The coefficients of R (x)are considered to be a32-bit sequence.
5. The bit sequence is completed and the results the CRC.

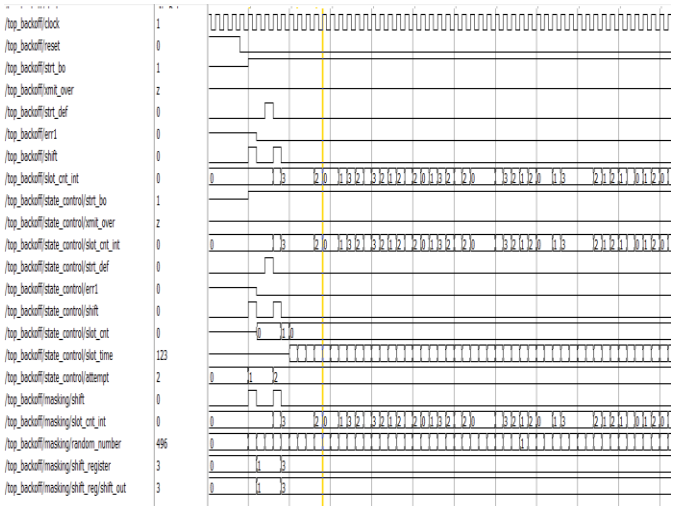
VIII. SIMULATION AND SYNTHESIS RESULTS



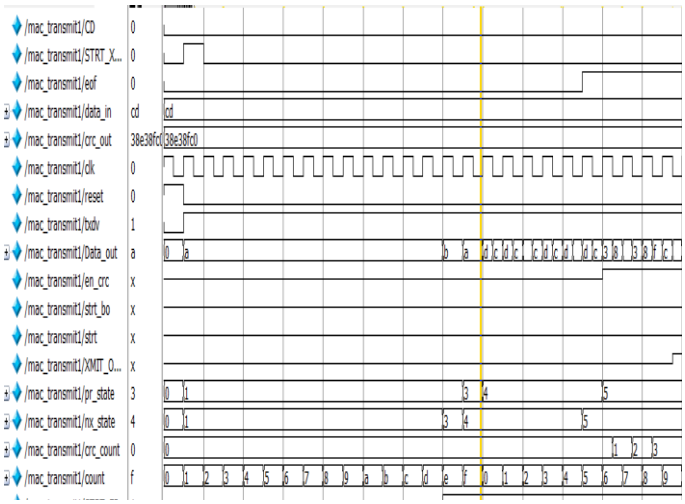
Simulation result of Defer



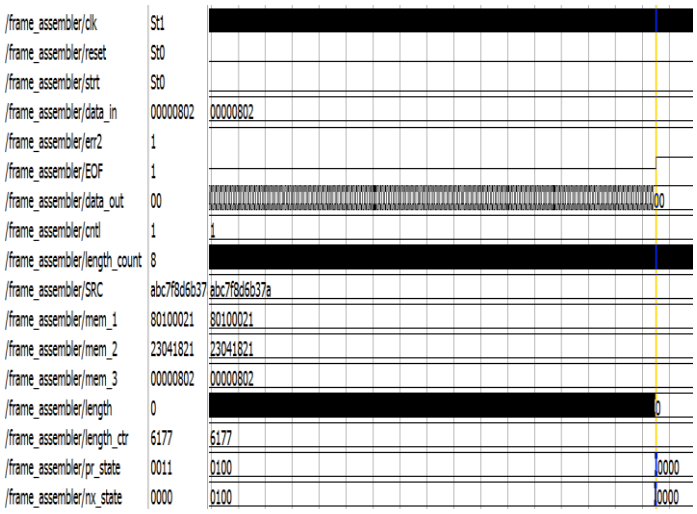
Simulation result of CRC



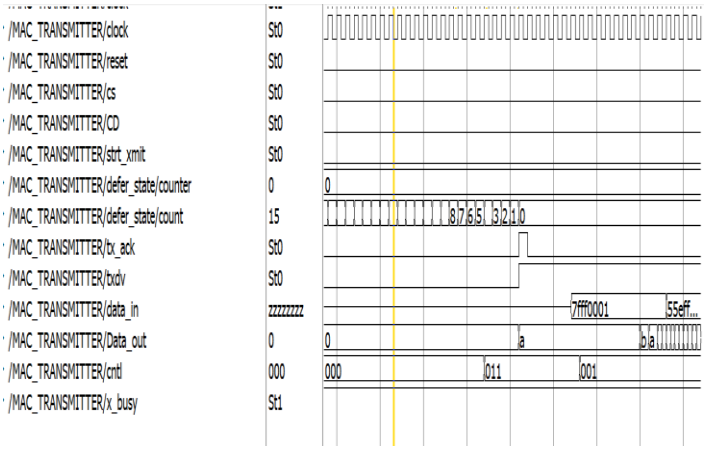
Simulation Result of Top Backoff



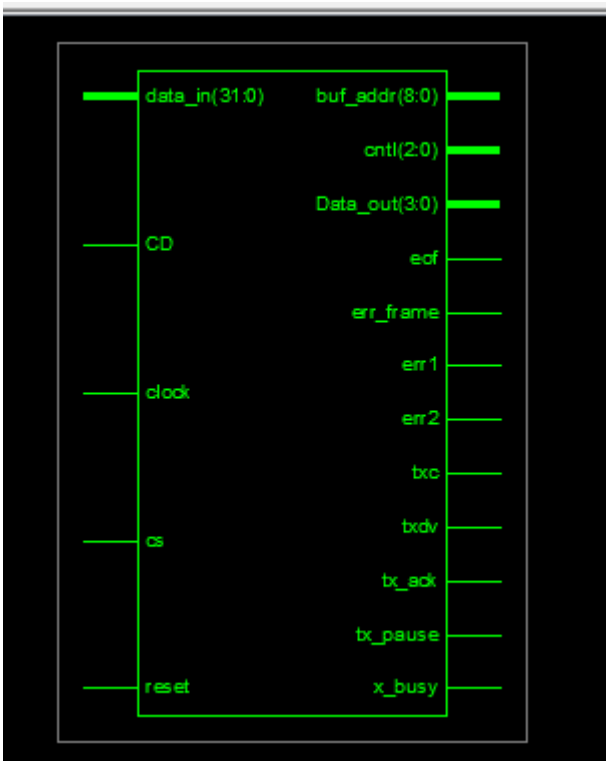
Simulation Result of Transmitter



Simulation result of Frame assembler



Simulation result of the MAC Transmitter Top module



Top level synthesis module

IX. CONCLUSION

The VHDL Implementation of MAC gives the improved digital design process, especially for FPGA design. A hardware description language allows a digital system to be designed and debugged at a higher level before conversion to the gate and flip-flop level. One of the most popular hardware description languages is VHISC hardware description language (VHDL) .It is used to describe and simulate the operation of variety IEEE 802.3 systems.

This paper has covered and discussed a software design, and implementation of a basic IEEE 802.3 (MAC Transmitter) system. The speed of data transmission is very high & it gives proper CRC bit for receiving correct data. The simulated waveforms give the reliability of the VHDL implementation to describe the characteristics and the architecture of the designed MAC with embedded BIST.

The simulated waveforms also have shown the observer how long the test result can be achieved by using the Built-In-Self-Test technique (BIST) is completed at 39.2ms using 25 MHz clock speed transmitting at 100 Mbps. Even though it seems not to be as fast as it should be when BIST is implemented (the receiver needs to wait the signal from the transmitter), the MAC Transmitter module still takes advantage of the 100% fault coverage. This is the most important thing that should not be left out by any designer to

ensure the reliability of their design. The next target for this research is to verify the RTL, implement and download it on Xilinx‟s FPGA chip.

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