8x8 Bit of Low Power Multipliers

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***Abstract*— Multiplier plays significant role in the DSP processors. It is old concept but every time researchers are encouraged to made modification in the multipliers because of its important in today's world. A 8x8 bit multiplier with the modified radix-4 encoding Multiplier plays significant role in the DSP processors. It is old concept but every time researchers are encouraged to made modification in the multipliers because of its important in today's world. A 4x4bit multiplier with the modified radix-4 encoding technique serves a better approach rather than existing other multipliers. The 4x4bit radix-4 multiplier implemented in 45nm CMOS technology. Simulated with the TANNER EDA tool and compared with the Low-cost low power bypassing based multiplier and radix-4 multiplier in terms of the delay, number of transistor count and power dissipation. Every aspect of the technological parameter serves better performance technique serves a better approach rather than existing other multipliers. Array Multiplier is also implemented with the improved full and half adder for low power dissipation. The 4x4bit radix-4 multiplier and Array multiplier implemented in 45nm CMOS technology. Simulated with the TANNER EDA tool and compared with the previously work done. Comparisons is made in terms of the delay, number of transistor count and power dissipation. Every aspect of the technological parameter serves better performance**

***Keywords*—** Array Multiplier, Radix-4, Modified booth encoding, CMOS, 45nm, TANNER

I. INTRODUCTION

In today's world the speed and power consumption are the most fundamental things that could be necessary to achieve. As electronics engineer it should be the first criteria. Multiplier gives the significant important in the power dissipation and speed. Multipliers are merely very useful in the DSP processors, math processors, and arithmetic processors. In the DSP processors it is necessary to do convolution, fast Fourier transform and correlation. Multiplier will make these things comparatively faster.

Here the new kind of multiplier is designed for the low power dissipation and for the less delay and for the less area (number of transistors). There are so many techniques available for design of multiplier. Here we have used the radix-4 technique and adding and shifting for array multiplier.. Even in the modified booth recoding there are various techniques are available like radix-2, radix-4, radix-8, radix-16, and radix-32. Among these the radix-4 serves the better area and power consumption and better speed compare to radix-2[5]. Going to further, In the multiplier the booth decoder has been designed. Even also it can be design various way and we have implemented it with our own method. The CLA (carry look ahead adder) is used for the faster multiplication. Basic multiplication can be realized by the shift add algorithm by generating partial products and adding successive properly shifted partial product. Thus multiplication is proportional to number of partial products to be added. So the ultimate thing is that if we reduced the partial product then automatically we get the lesser delay and power dissipation. [4]. the array multiplier has the AND gates and adders for the operation. Each of the partial products will be generated when multiplier is multiplying with multiplicand.

Various kind of technologies are available for implementation like BJT, pass transistors, transmission gates and etc. but we have chosen to do this in CMOS because CMOS is widely used now a days and it also gives better response compared to previous technologies in terms of power dissipation, delay. The simulation is done in the TANNER EDA V.15

II. ARCHITECTURE

A. RADIX-4 MBE MULTIPLIER

Architecture of 8x8 bit radix-4 multiplier for low power, less delay and low area is shown in figure. Here the booth encoder gets the multiplier value and the booth decoder will get the multiplicand value. The booth decoder has a HA (half adder) in front of it for the 2's complement case. It will generate the partial product (PPG). This partial product will give to the sign extension for the shifting of the bits and then it will give to the CLA (carry look ahead adder). Finally we get the 8 bit output.

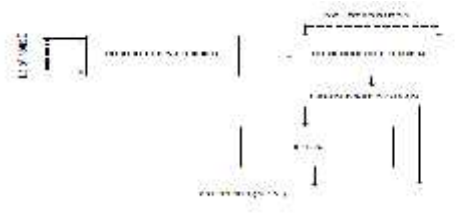

Figure 1: Architecture of proposed radix-4 MBE multiplier

Booth Encoder and PPG Module

Booth encoder is the essential part of the multiplier. It consumes much of the area of multiplier. The booth encoder can be designed in various ways. [7] as much as good the booth encoder the number of getting output chances good. Booth encoder is implemented with the help of inverter, XOR and AND gates. It will generate the three control signals which are given to the booth decoder for the generation of the partial product. According to the design of booth encoder we will get the output of three control signals that are shown in table 1.

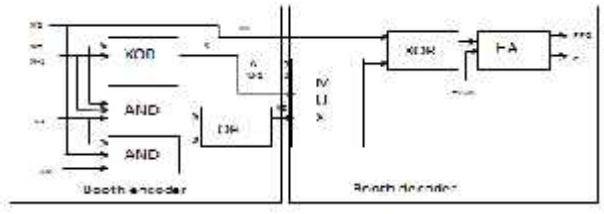

Figure 2: Booth encoder and PPG module

Table 1: Booth Encoder Truth Table

X1	X0	X-1	MI	X	X2
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	0	0	1
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	1	0
1	1	1	1	0	0

The designed booth encoder and decoder are modified and shown in figure 2. The one bit booth decoder is shown here and in further way designed the 9-bit booth decoder. For the 8x8 bit radix-4 modified booth multiplier.

Sign Extension

This sign bit extension is different from the book and reference value, we apply the highest partial product bit rather than the multiplicand bit. This difference maybe come from we take a different approach to add sign bit. The book and reference paper all take the same way to put sign bit add at adder part. We finish this target at the generation partial product.

Carry Look Ahead Adder

Adder is widely used in the generic computer because it is very important for adding data in the processor. The simplest binary adder is ripple carry adder. It is easy to be understood and implemented. A more complex binary adder is carry look ahead adder (abbreviated as CLA) .It uses the same carry look ahead circuits to construct the higher-bit CLA recursively. It is widely used due to its superior performance over ripple carry adder. The speed of execution is the most important factor that needs to be considered for appraising the quality of an adder. Traditional CLA is constructed by XOR, AND, and OR gates. The proposed circuit uses NAND gates to replace the AND and NOT gates in CLA, it can decrease the cost of CLA and increase the speed of CLA. The method of speeding up the addition process is based on the two additional functions of full adder, called carry generated and carry propagate functions. CLA speed up the process by eliminating the ripple carry delay.

It examines all the input bits simultaneously and also generates the carry-in bits for all the stages simultaneously. The various partial full adder has been designed for the carry outs and they are implemented as given below expressions.

C1=CG+CP0.Cin
C2=CG1+CP1.CG0+CP1.CP0.Cin
C3=CG2+CP2.CG1+CP2.CP1.CG0+CP2.CP1.CP0.Cin
C4=CG3+CP3.CG2+CP3.CP2.CG1+CP3.CP1.GO+CP3.CP2.CP1.CP0.Cin

Radix-4

Booth encoding algorithm is a method that reduces the number of partial products in the process of multiplying the multiplicand and the multiplier. Here add –a and send a carry of 1 into the nextradix4digitofthemultiplier. If Radix-4 multiplication performed with the recoded multiplier, only the multipliers of ±a and ±2a will be required, all of which are easily obtained by shifting and/or complementation. In four bit Radix-4 multiplier, 2 partial products will be produced. Partial products are reduced to half as compared to the shift and add method. [3] It is then simulated and then finally compared with other multipliers. Booth recoding is fully parallel and carry free. The main advantage of the modified Booth algorithm is that it reduces the partial Products to n/2. The following gives the algorithm for performing sign and unsigned multiplication operations by using radix-4 Booth recoding. Radix-4 Booth algorithm which scan strings of three bits with the algorithm given below: (1) Extend the sign bit 1 position if necessary to ensure that n is even. (2) Append a 0 to the right of the LSB of the multiplier. (3) According to the value of each vector, each Partial Product will be 0, +y, –y, +2y or –2y. The negative values of y are made by taking the 2's complement.

a	**0110**	
x	**1010**	
z	**-1 -2**	**Radix-4 recoded version of x**
$P^{(0)}$	000000	
+Z0a	110100	
$4P^{(1)}$	110100	
$P^{(1)}$	11110100	
+Z1a	111010	
$4P^{(2)}$	11011100	

$P^{(2)}$ 11011100

B. Array Multiplier

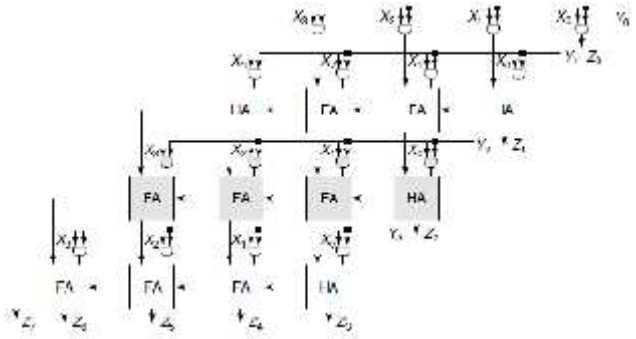

Figure 3: Array multiplier[10]

In array multiplier the figure 2 shows the architecture. In array multiplier, consider two binary numbers A and B, of m and n bits. There are mn summands that are produced in parallel by a set of mn AND gates. n x n multiplier requires n (n-2) full adders, n half-adders and n2 AND gates. Also, in array multiplier worst case delay would be (2n+1) td. The delay for this multiplier is larger. It also requires larger number of gates because of which area is also increased; due to this array multiplier is less economical.

This is the unique architecture for the array multipliers but the important thing is the design of FA (full adder) and HA (half adder). Array has generally the long delay but though it is useful because of its ease of implementation to avoid complexity and low cost. Here we tried with help of designing these adders as much efficient is possible. For the design of the full adders we have to use XOR gate and that can be implement with the 6 transistors only instead of conventional 12 transistors. Full adder can be implemented in various ways like using two XNOR, using 14 transistors, 28 transistors, using GDI and transmission gate etc. among that our full adder has 30 transistors but the output is much glitches free compared to other full adders when using 45nm technology.

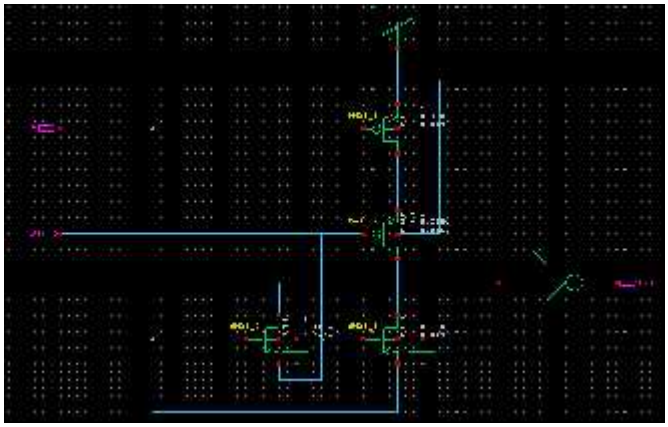

Figure 4: XOR gate

III. SIMULATION

The simulation of the 8x8 bit modified radix-4 multiplier and array multiplier is done in the TANNER tool. In this simulation we have consider the 45nm parameter and the given VDD is 1v. Below (Figs.5~7) shows the complete schematic view of the multiplier and (Figs.6~8) shows the simulated result of multiplier. With the help of simulation the different parameters like power dissipation, delay and number of transistors are easily find and they are compared with the other existing multipliers. Simulation gives the output of array and radix-4 with the appropriate input. For the multiplication we have consider 11111111 bits for multiplicand and 11111111 bits for multiplier and the final output is 1111111000000001.

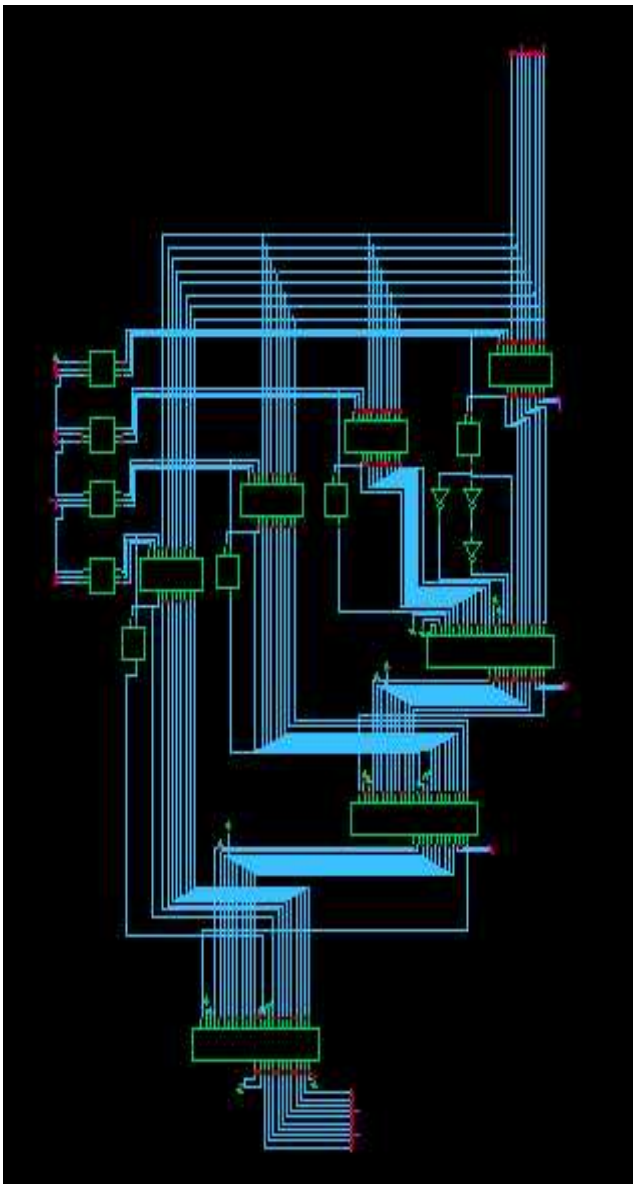

Fig 5: Proposed radix-4 8x8 bit MBE multiplier

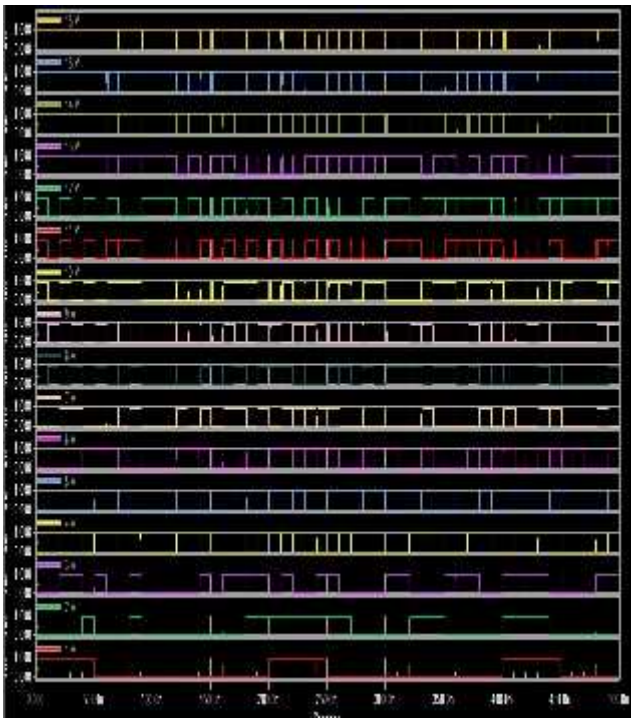

Fig 6: simulation of radix-4 MBE multiplier

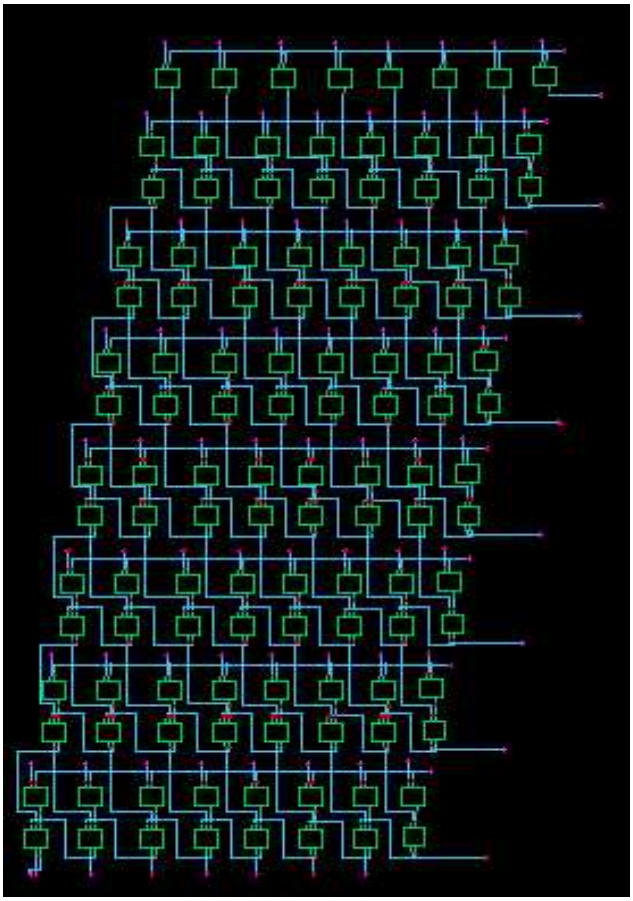

Fig 7: Proposed 8x8 bit Array multiplier

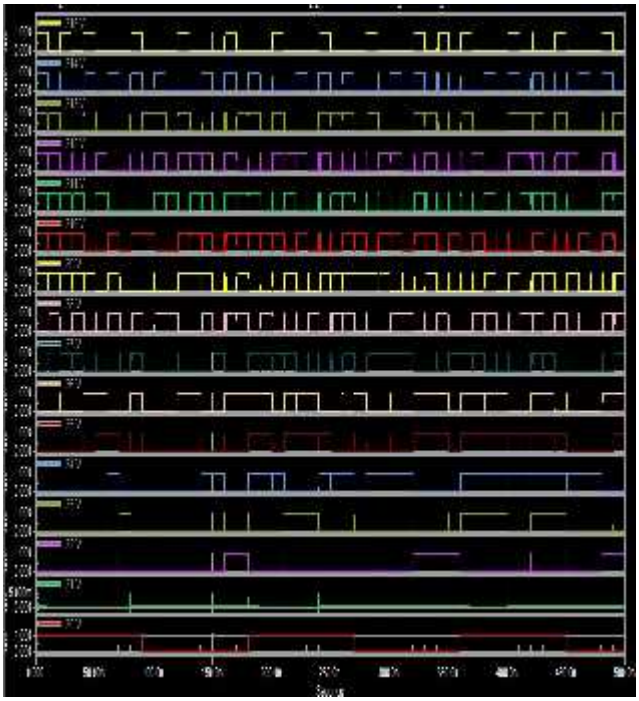

Fig 8: simulation of array multiplier

Table 2: Comparisons of 8x8 bit multipliers

Param-eter	Proposed Radix-4	Proposed Array	[2]	[3]	[9]	[8]
VDD	1V	1V	3.5V	3.5V	-	-
Delay	447.14228 (ps)	1.27200 (ns)	1.2124 (ns)	187 (ps)	3.02 (ps)	3.81 (ps)
PD(mW)	1.0268861	0.261890	8.081	0.623	5.16	489
nm	45	45	350	350	-	-

IV. CONCLUSION

The radix-4 modified booth multiplier is designed with the new technology and proposed architecture become successful for the delay, power dissipation and area means number of transistors. The proposed multiplier is lacking in terms of delay with the same as the array multiplier has the advantage in terms of power dissipation. The other parameters are improves as shown in table 2. This multipliers can be used in various applications like DSP processors and math processors.

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