Implementation and Performance Analysis of 4-bit GDI Adders

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ABSTRACT :
Adders plays an important role in the DSP processors,microprocessors, digital signal processors and data processing application-specific integrated circuit (ASIC) is its data path,word length. It is not a new concept but every time researchers are encouraged to made modification in the adders because of its important in today's world.Several logic families have been proposed and used to improve circuit performance beyond that of conventional static CMOS family The 4 bit adders implemented in 45nm GDI technology. Simulated with the TANNER EDA tool and compared different adders in terms of the delay, number of transistor count and power dissipation. Every aspect of the technological parameter serves better performance.

KEY WORDS: ***Full Adder,Ripple Carry Adder, Carry look Ahead Adder Carry Select Adder,Carry Skip Adder, 45nm, TANNER.***

1. INTRODUCTION

With the advances in Very Large Scale Integration (VLSI) technology, arithmetic operations are penetrating into more and more applications. At the heart of data-path and addressing units in turn are arithmetic units, such as comparators, adders, and multipliers. Finally, the basic operation found in most arithmetic components is the binary addition.Computations needs to be performed using low-power, area-efficient circuits operating at greater speed. Addition is the most basic arithmetic operation;and adder is the most fundamental arithmetic component of the processor.

Designers of VLSI have several options to reduce the power dissipation in the various design stages. Much of the research efforts of the past years in the area of digital electronics have been directed towards increasing the speed of digital systems. Recently, the requirement of portability and the moderate improvement in battery performance indicate that the power dissipation is one of the most critical design parameters.The three most widely accepted metrics to measure the quality of a circuit or to compare various circuit styles are area, delay and power still demands high computational speeds. Hence, in recent VLSI systems the power-delay product becomes the most essential metric of performance.

I. ADDERS

The saying goes that "if you can count, you can control". Addition is a fundamental operation for any digital system, digital signal processing or control system. A fast and accurate operation of a digital system is greatly influenced by the performance of the resident adders because of their extensive use in other basic digital operations such as subtraction, multiplication and division.

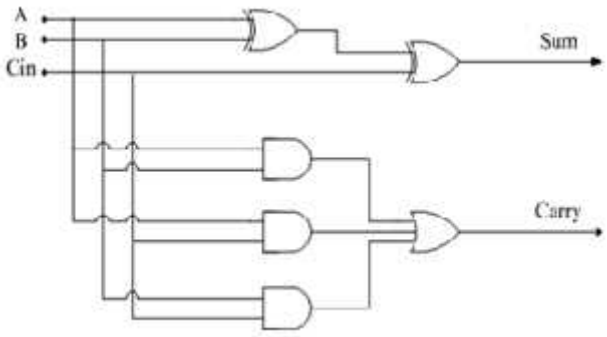


Figure 1:Gate level full adder circuit

Hence, improving performance of the digital adder would greatly advance the execution of binary operations inside a circuit compromised of such blocks. All these operations are realized by complex systems of transistors. Most of these systems have the adder in their critical path. The critical path consists of transistors that produce the maximal time-delay in the output signal. The behavior of the transistors in the critical path essentially determines performance of the entire system. Performance of the adders can be considered as extremely significant for VLSI systems.It is also a very critical one if implemented in hardware because it involves an expensive carry-propagation step, the evaluation time of which is dependent on the operand word length.

As transistor process technology approaches the nanometer scale, process variation significantly affects the design and optimization of high performance microprocessors. Prior studies have shown that chip operating frequency and leakage

power can have large variations due to fluctuations in transistor gate length and subthreshold voltage.

2. GDI Logic

A new low power design technique that solves most of the problems known as Gate-Diffusion-Input (GDI) is proposed. This technique allows reducing power consumption, propagation delay, and area of digital circuits. A basic GDI cell contains four terminals – G (common gate input of nMOS and pMOS transistors), P (the outer diffusion node of pMOS transistor), N (the outer diffusion node of nMOS transistor), and D (common diffusion node of both transistors).

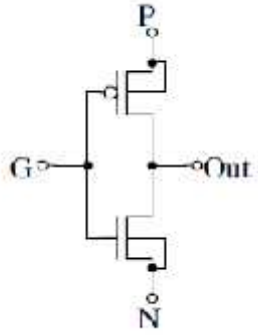


Figure 2: Basic GDI cell

GDI method is based on the use of a simple cell as shown in figure 2. At the first look the design is seems to be like an inverter, but the main differences are 1) GDI consist of three inputs- G (gate input to NMOS/PMOS), P (input to source of PMOS) and N (input to source of NMOS). (2) Bulks of both NMOS and PMOS are connected to N or P (respectively), so it can be arbitrarily biased at contrast with CMOS inverter.

Table 1:GDI logic functions

N	P	G	Out	Function
'0'	B	A	$\bar{A}B$	F1
B	'1'	A	$\bar{A}+B$	F2
'1'	B	A	$A+B$	OR
B	'0'	A	AB	AND
C	B	A	$\bar{A}B+AC$	MUX
'0'	'1'	A	$\bar{A}$	NOT

Table 1 shows how a simple change of the input configuration of the simple GDI cell corresponds to very different Boolean functions. Most of these functions are complex (6–12 transistors) in CMOS, as well as in standard PTL implementations, but very simple (only two transistors per function) in the GDI design method.

This design can implement a wide variety of logic functions using only two transistors. This method is suitable for design of fast, low-power circuits, using a reduced number of transistors ,while improving logic level swing and static power characteristics and allowing simple top-down design by using small cell library.

3. Ripple Carry Adder

In the parallel adders,the carry out of each stage is connected to the carry-in of the next stage.The sum and carry-out bits of any stage cannot be produced,until some time after the the carry-in of that stage occurs.This is due to the propagation delays in the logic circuitry,which lead to a time delay in the addition process.The carry propogation delay for each full-adder is the time between the application of the carry-in and the occurrence of the carry-out.

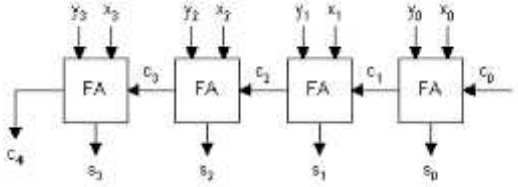


Figure 3: 4-bit Ripple Carry Adder

Referring to the 4-bit parallel adder,the sum (s0) and the carry-out (cout) bits given by FA0 are not valid until after the propogation delay of FA0.Similiarly,S1 is not valid until after the cumulative propogation delay of two full adders (FA0 and FA1),and so on.At each stage ,the sum bit is not valid until after the carry bits in all preceding stages are valid.In effect,carry bits must propogate or ripple through all stages before the most significant bit is valid.Thus,the total sum (the parallel output) is not valid until after the cumulative delay of all adders.

The Parallel adder in which the carry-out of each adder is the carry-in to the next most significant adder is called a ripple carry adder.The greater the number of bits that a ripple carry must add,the greater the time to required for it to perform a valid addition.

4. Carry Look Ahead Adder

In the case of the parallel adder,the speed with which an addition can be performed is governed by the time required for the carries to propagate or ripple through all of the stages of the adder.The carry look ahead adder speeds up the the process by eliminating this ripple carry delay.It examines the all the input bits simultaneously and also generates the carry-in bits for all the stages simultaneously.

The method of speeding up the addition process is based on the two additional functions of the full adder,called the carry generate and carry propagate functions.

$Pi = Ai \oplus Bi$ Carry propagate

$Gi = Ai.Bi$ Carry generate

Note that both propagate and generate signals depend only on the input bits and thus will be valid after one gate delay. The output sum and the carryout are given by:

$Ci+1 = Gi + PiCi$

$Si = Pi \oplus Ci-1$

These equations show that a carry signal will be generated in two cases:
1) if both bits Ai and Bi are 1
2) if either Ai or Bi is 1 and the carry-in Ci is 1.
Figure 6 shows the carry generator needed to add four bits numbers.

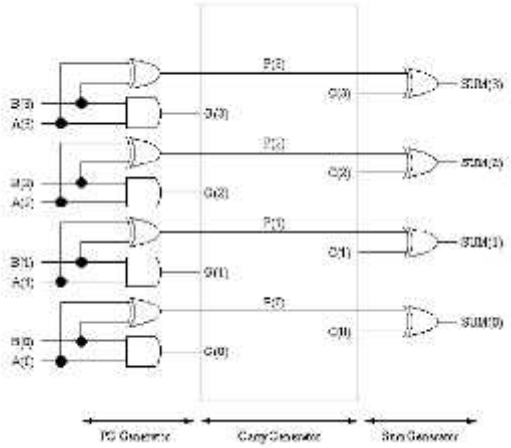


Figure 4:4-bit Carry Look Ahead Adder

5. Carry Skip Adder

A carry-skip adder consists of a simple ripple carry-adder with a speed up carry chain called a **skip chain**. This chain defines the distribution of ripple carry blocks.

5.1 Carry Skip Mechanics

The addition of two binary digits at stage i, where i≠ 0, of the ripple carry adder depends on the carry in, *Ci* , which in reality is the carry out, *Ci-1*, of the previous stage. Therefore, in order to calculate the sum and the carry out, *Ci+1*, of stage i, it is imperative that the carry in, *Ci*, be known in advance. Note that in some cases *Ci+1* can be calculated without knowledge of *Ci*.

Pi = Ai ⊕ Bi (1)--carry propagate of ith stage
Si = Pi ⊕ Ci (2)--sum of ith stage
Ci+1 = AiBi + PiCi (3)--carry out of ith stage
Supposing that *Ai = Bi*, then *Pi* in equation 1 would become zero. This would make *Ci+1* to depend only on the inputs *Ai* and *Bi*, without needing to know the be equivalent to the carry in. Hence we can simply propagate the carry to the next stage without having to wait for the sum to be calculated.

5.2 Carry Skip Chain

The carry skip chain mechanism (Figure 5) works as follows: Two strings of binary numbers to be added are divided into blocks of equal length. In each cell within a block both bits are compared for un-equivalence. This is done by Exclusive ORing each individual cell producing a comparison string. Next the comparison string is ANDed within itself in a domino fashion.

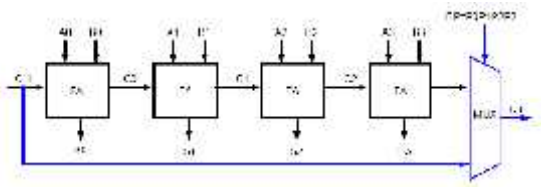


Figure 5:Carry Skip Adder

This process ensures that the comparison of each and all cells was indeed unequal and we can therefore proceed to propagate the carry to the next block. A MUX is responsible for selecting a generated carry or a propagated carry with its selection line being the output of the comparison circuit just described.

6. Carry-Select Adder

The concept of the carry-select adder is to compute alternative results in parallel and subsequently selecting the correct result with single or multiple stage hierarchical techniques. In order to enhance its speed performance, the carry-select adder increases its area requirements. In carry-select adders both sum and carry bits are calculated for the two alternatives: input carries “0” and “1”. Once the carry-in is delivered, the correct computation is chosen (using a MUX) to produce the desired output. Therefore instead of waiting for the carry-in to calculate the sum, the sum is correctly output as soon as the carry-in gets there. The time taken to compute the sum is then avoided which results in a good improvement in speed. Carry-select adders can be divided into equal or unequal sections. Figure 8 shows the implementation of carry select adder.

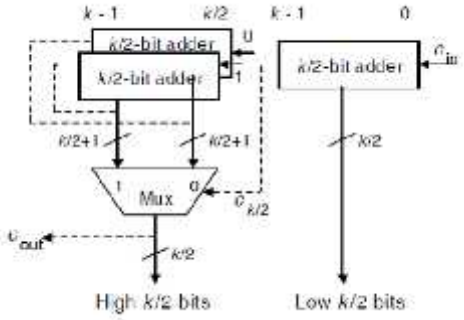


Figure 6:Carry Select Adder

Carry select adders use multiple narrow adders to create fast wide adders. Consider the addition of two n bit numbers with a = an-1…..a0, and b = bn-1…..b0. At the bit level the adder delay increases from the least significant 0th position upward, with the (n-1)th requiring the most complex logic. A carry select adder breaks the addition problem into smaller groups. A carry-select adder provides two separate adders for the upper words, one for each possibility. A multiplexer (MUX) is then used to select the valid result. The figure 8 shows the block diagram of CSA. As a concrete example, consider an 8-bit adder that is split into two 4-bit groups. The

lower order bits a3 a2 a1 a0 and b3 b2 b1 b0 are fed into the 4-bit adder to produce the sum bits S3 S2 S1S0 and a carry-out bit C4 as shown.

7. SIMULATION

The simulation of the GDI adders is done in the TANNER tool. In this simulation we have consider the 45nm parameter and the given VDD is 1v. Below figure shows the complete schematic view of the various adders and the simulated result of various adders. With the help of simulation the different parameters like power dissipation, delay and number of transistors are easily find and they are compared with the other adders. Simulation gives the output with the appropriate input.

7.1 Implementation of 2-input GDI XOR gate

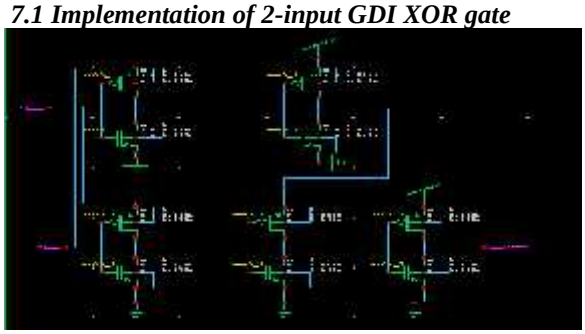


Figure 7:Implementation of 2-input GDI XOR gate

7.2 Implementation of 2-input GDI AND gate

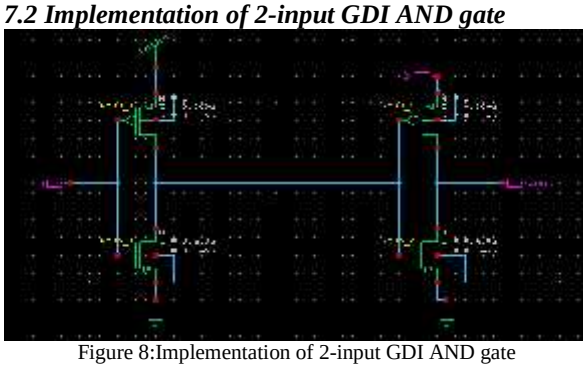


Figure 8:Implementation of 2-input GDI AND gate

7.3 Implementation of 2-input GDI OR gate

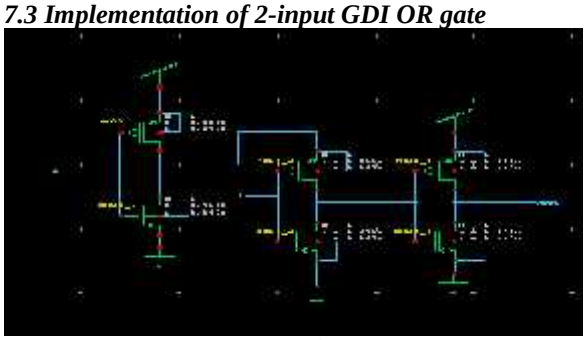


Figure 9:Implementation of 2-input GDI OR gate

7.4 Implementation of 1-bit GDI full adder

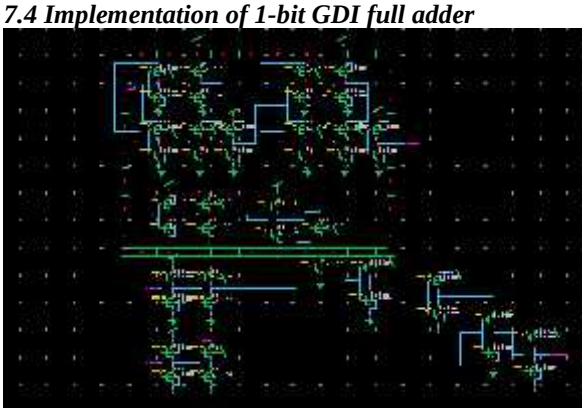


Figure 10:Implementationof 1-bit GDI full adder

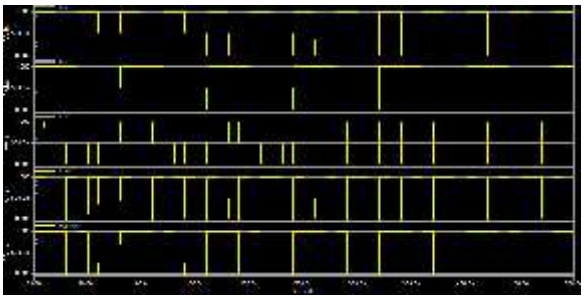


Figure 11: Simulation results of 1-bit GDI full adder

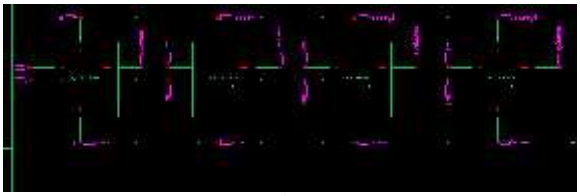


Figure 12:Implementation of 4-bit GDI Ripple Carry Adder

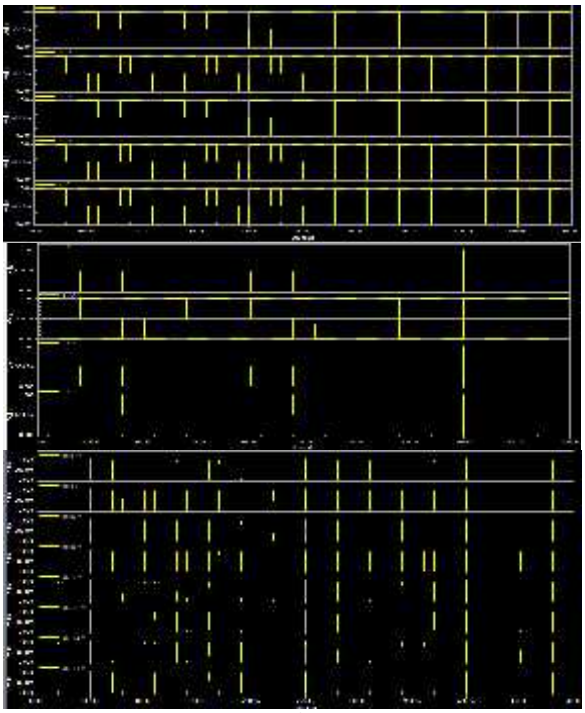


Figure 13:Simulation results of 4-bit GDI ripple carry adder

7.5 Implementation of Carry Look Ahead Adder

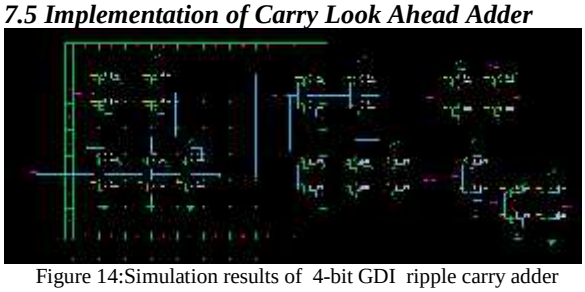


Figure 14:Simulation results of 4-bit GDI ripple carry adder

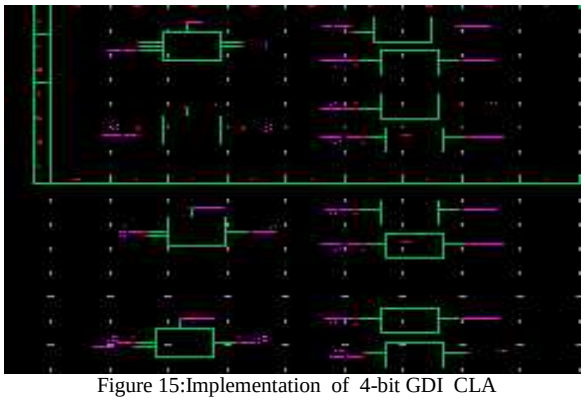


Figure 15:Implementation of 4-bit GDI CLA

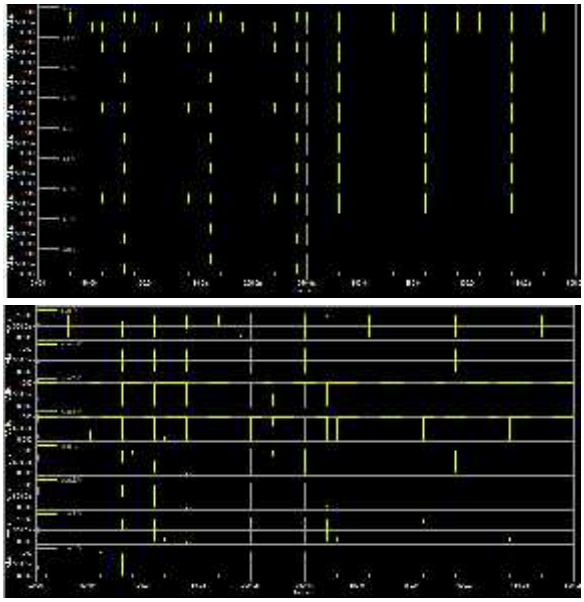
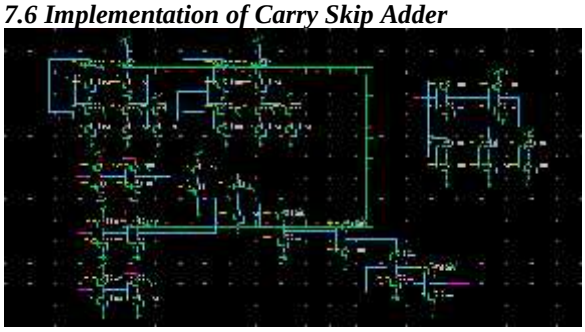


Figure 16:Simulation results of 4-bit GDI CLA

7.6 Implementation of Carry Skip Adder



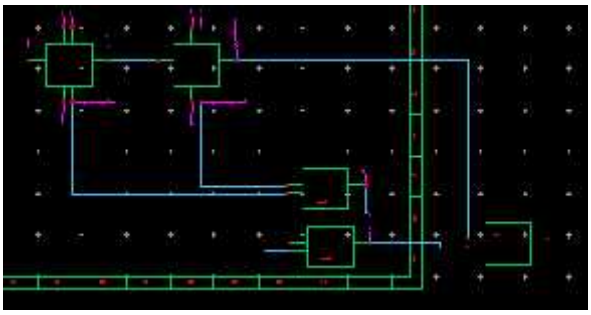


Figure 17:Implementation of 4-bit GDI CSK

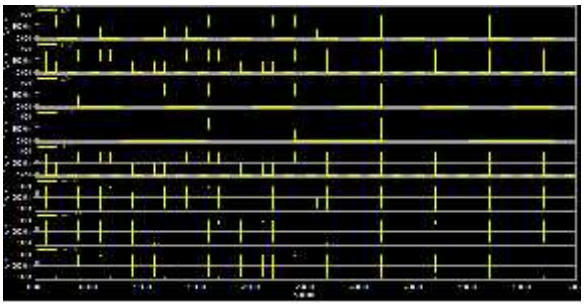


Figure 18:Simulation results of 4-bit GDI CSK

7.7 Implementation of Carry Select Adder

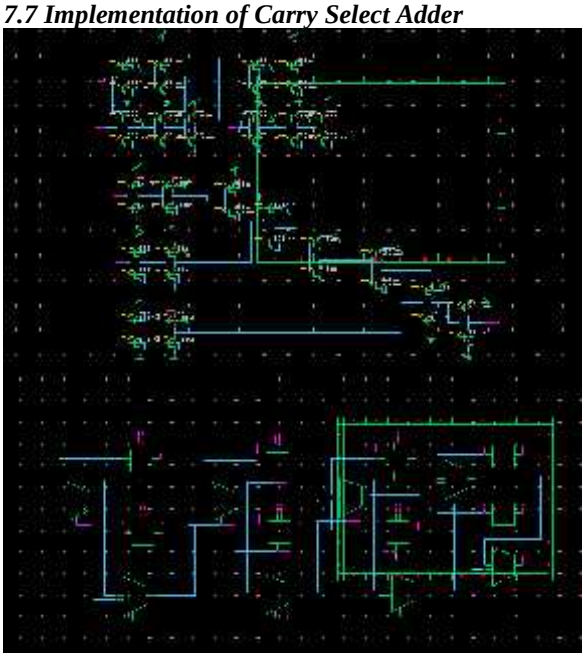


Figure 19:Implementation of 4-bit GDI CSA

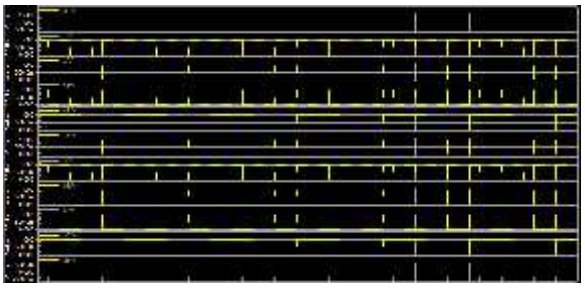


Figure 20:Simulation results of 4-bit GDI CSA

8. COMPARISONS

8.1 Low power

In this paper,comparison of various adders are done on one of the parameter that is power parameter.Here comparison is done on average power dissipation.

8.2 Transient Delay

In this paper,comparison of various adders are done on one of the parameter that is delay parameter.Here comparison is done on average transient delay.

Table 1: Comparative analysis of adders

Parameters	Ripple Carry Adder	Carry Look Ahead Adder	Carry Skip Adder	Carry Select Adder
Technology (nanometer)	45	45	45	45
Vdd	1v	1v	1v	1v
Transient Delay(ns)	0.28	0.20	0.52	0.52
Average Power dissipation(mW)	0.045	0.035	0.096	0.124
Transistor Count	176	160	264	248

9. CONCLUSION

GDI 4-bit various adders are designed with 45 nm technology with 1v vdd.Carry look ahead adder has comparatively low transient delay and low power dissipation.so this adder can be used in various applications like DSP processor and math processor.

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