A High Throughput Low Complex VLSI Architecture for MIMO

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***Abstract*—Multiple Input Multiple Output (MIMO) transmission has become more popular for mobile communication systems. MIMO detection is a big issue. In this paper a low complex and high throughput VLSI implementation is proposed .The major issue of concern is to keep the computational complexity of the decoding algorithm within a limited bound. The K-Best detectors are attractive for VLSI implementations as it gives less computational complexity. The K-Best detector guarantees an SNR-independent fixed-throughput detection which gives a performance close to that of ML. Here instead of exhaustively searching all the nodes, the intermediate nodes of the search tree on demand is expanded /visited. This architecture is well suitable for pipelined parallel implementation. The proposed algorithm is used to fabricate a 4x4, 256QAM complex multiple-input-multiple-output detector.**

***Keywords*—MIMO, K-Best, VLSI**

I. INTRODUCTION

Radio transmissions traditionally use one antenna at the transmitter and one antenna at the receiver is termed Single Input Single Output (SISO). The transmitter and the receiver both have one RF chain (that's coder and modulator). SISO is simple and cheap to implement and it has been used age long since the birth of radio technology. Mainly it is used in radio and TV broadcast and our personal wireless technologies (e.g. Wi-Fi and Bluetooth). To improve the performance of the system, a multiple antenna technique has been considered. A system which uses a single antenna at the transmitter and multiple antennas at the receiver are named Single Input Multiple Output (SIMO).A system which uses multiple antennas at the transmitter. Into the traditional frequency-time domain a third dimension, space, is introduced. This is done by transmitting multiple streams of data at the same frequency on multiple antenna, to increase throughput. Normally, multiple receiver antennas are used as this configuration achieves high data rates. This type of transmission is called Multiple Input Multiple Output (MIMO)single antenna at the receiver is named as Multiple Input Single Output (MISO). Multiple-input multiple-output (MIMO) systems are widely recognized as the enabling technology for future wireless communication systems. In particular the use of spatial multiplexing allows channel to achieve a linear increase in capacity with the minimum of the number of antennas employed at the transmitter and at the receiver.

The objective of this project is to design a high throughput, low complex VLSI architecture for MIMO. The resulting design is energy efficient. The modified k-best algorithm gives low complexity for the circuit. The MIMO technique gives a high throughput. This method increases capacity and the spectral density.

II. PROJECT DESCRIPTION

The MULTIPLE-INPUT-MULTIPLE-OUTPUT systems have the potential of achieving high spectral efficiency, high data rate, and robust wireless link, with an complexity which is acceptable in wireless systems. The MIMO technology has been already included in many wireless communication standards, such as the long-term evolution project, IEEE 802.16e, and IEEE 802.16 m. The design of low-complexity, low-energy, high-performance, and high-throughput receivers is the key challenge in the design of any MIMO receiver. Several MIMO

detection algorithms have been proposed to address this challenge, which offer various tradeoffs between the performance and the computational complexity. Among the large variety of the MIMO detection techniques ,maximum-likelihood (ML) detection is the optimum detection method and minimizes the bit error rate (BER) performance. But its computational complexity grows exponentially with the number of transmit antennas. On the other hand, linear detection methods such as the zero-forcing or the minimum mean squared error (MMSE) have lower complexity with a poor BER performance.

Finally, as a tradeoff between complexity and performance loss, a large category of the detection algorithms have been proposed, which includes the depth-first and the breadth-first search algorithms. The well-known depth-first strategy is the sphere decoder (SD) which guarantees the optimal performance in the case of unlimited execution time . But the intrinsic variable throughput results in extra overhead in the hardware and significantly lower data rates in the lower signal-to-noise ratio (SNR) regimes. Among the breadth-first search methods, the most commonly used approach is the K-Best algorithm (a.k.a M-algorithm) . The K-Best detector guarantees an SNR-independent fixed-throughput detection scheme with a performance close to that of ML. Although K-Best detectors are attractive for VLSI implementations, there are still some challenges, such as an efficient sorting and expansion scheme, in order to pave the way to achieve high throughputs.

III.MIMO SYSTEM MODEL

MIMO system having NT antennas at the transmit and NR receive has the channel matrix H(M×N) as

$$Y=Hs+n \quad (1)$$

Where n is Guassian noise vector, the transmitted symbol is s with the received signal which is represented by (y)

The main objective of the MIMO detection is to find the closest ŝ for a given signal received which is represented by (y)

$$\hat{s} = \arg \min_{s \epsilon \mathcal{O} \mathrm{N}\, T} \| y - Hs \|^2 \quad (2)$$

A. Proposed K-Best Algorithm

The QR decomposition of channel matrix H=QR in which Q is a unitary matrix of NR×NT matrix and R represents an upper triangular matrix of $N_T \times N_T$

$$T_i(s^{(i)})=T_{i+1}(s^{(i+1)})+e_i|(s^{(i)})|^2 \quad (3)$$

$$L_i(s^{(i)})=L_i(s^{(i)})^{-1}\times r_{ii} \quad (4)$$

Step I. Level NT

1) Calculate the FC which is the NT the entry of the z matrix.

2) Find all of the Level-2 nodes that at the same location as row of the constellation with the FC.

3) Calculate the PED of the FC and all the Level-2 nodes and save all these √M nodes and their PED values in a register bank (i.e., L).

Step II. Level (NT − 1)…Level 2

1) For i = 1 : K

a) Calculate the value of Li s(i) for the incoming node, which is the i th parent of the current level.

b) Find the FC.

c) Find RSE_Num Level-2 nodes, which are the nearest nodes to the FC using the row SE enumeration (RSE) technique.

d) Calculate the PED values for the above RSE_NumLevel-2 nodes and the FC, and then save all these nodes in the corresponding register bank (L) result-ing in |L|= RSE_Num + 1forthe i th parent of the current level.

Step III. First Level

1) For k = 1 : K

a) Calculate the value of L_k S(k) for the incoming node, which is the kth parent of the current level.

b) Find the FC and the corresponding PED.

End

2) Find the sorted list of the K first children of the parents in the order of non-decreasing PED.

3) Find the node with the minimum PED from the sorted list of the first children and announce it with all of its parents up to the level NT as the hard decision outputs of the detector.

IV. IMPLEMENTATION

The VLSI implementation of the proposed architecture consists mainly of the elements for the selection of best noes. The $z_i$and r_{ij} along with some of the control signals are given through it. At each of the states the best node is chosen and for that node the best child is visited and the siblings are considered by the column enumeration. Then a list of these nodes are updated in the list L. The sorter performs a sorting based on the PED values of the elements present in this list. The element node with a lowest PED value is taken and is announced as the child node. In the next stage this node is taken and is expanded for the next child node. Here too the siblings are taken and are visited. In the last charted the best leaf node is obtained. This way enables the expansion of limited node thus reducing the complexity of computation.

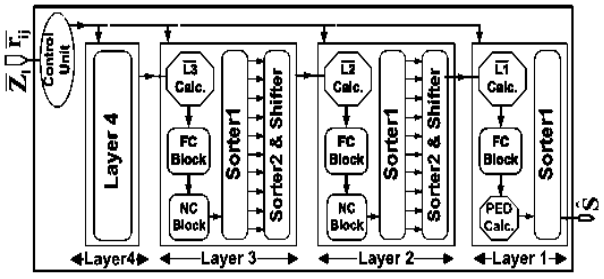

Fig.1Proposed VLSI architecture of a 4 × 4, 64-QAM MIMO detector

A. Layer NT

The layer NT implements Step I of the proposed algorithm. The detailed VLSI architecture of the layer NT is shown in Fig. 1, gets input as z4 and r44 as and generates K parents of layer NT − 1asthe outputs.

B. Layer (NT –1)... Layer 2

In the layer NT − 1 through Layer 2, the centries of z and R, some control signals and the K parents of the previous layer are taken as inputs and the K parents of the next layer is given as the output. In fact, these layers of the proposed architecture perform Step II of the proposed algorithm.

C. Layer 1

Finally, Layer 1 of the architecture performs Step III of the proposed algorithm and announces the child with the lowest PED with all its parents up to Layer NT as the output ˆs of the detector.

D. Li Calculation (Li Calc.)

In order to find the FC the value of s[0] l = Ll s(l) should be calculated and this value is used to calculate Ll s(l) for the PED calculation. As the different numbers of zi and rij are used to calculate L1, L2, and L3 a customized fully pipelined architecture is proposed.

E. NC block

This block is used in all layers except the first and the last layer. A fully pipelined VLSI architecture is proposed for the NC block. The NC block implements the step II and the step II.1 using adders, subtractors, and norm calculation blocks.

F. FC block

The proposed architecture for the FC block performs the step I.1 and step II.1.b of the proposed algorithm. This is done by using two mapper blocks and two limiter blocks. The FC block gives the best node as the FC node. This node is the one with low PED.

V. SIMULATION RESULTS

The simulation result shows the received signals by the K-Best algorithm.Selecting the signals which are transmitted by multiple antennas.

Fig 2 Received signals

VI. CONCLUSION

Multiple-input multiple-output (MIMO) systems are widely recognized as the enabling technology for future wireless communication systems .The algorithms which were used for this MIMO are very complex to implement .By using the K-Best algorithm reduced complexity architecture can be formed .The main purpose of MIMO is to achieve a high data rate with a increase in capacity .The performance degradation is very little. The less power consumption and the improved performance are due to the reduced complexity in the algorithm. A high throughput can be achieved using this algorithm. The size of the chip is also reduced.

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