Design a novel Low-Noise ,High Gain and High Bandwith Amplifire for 5GHz Wireless Recivers

Farhad Amiri, Milad kaboli
Amiri_f611@yahoo.com, kaboli.m@iauo.ac.ir
Islamic Azad University of Bushehr Branch, Islamic Azad University of omidieh Branch

Abstract*__Broadband systems (WB), a new wireless technology that can transmit data at a range of frequency bands with very low power and high data rate requirements. MOS technology, mainly due to low cost, low power consumption, high efficiency, low noise and high bandwidth circuits frequently WB, is used. Low-noise amplifier (LNA) is one of the most important components in a wireless sensor is available. The first piece of the whole system because it determines the sensitivity of the signals received from the antenna is amplified. Having a low noise LNA with good input match and gain sufficient brown field in the frequency range of the operation is required. Recently, a new architectural style with a broadband LNA is presented in the literature. The aim of this work is to design an optimal orbital characteristic.In this thesis, a low noise amplifier with high gain and low power in the 6-2 GHz band for use in wireless receiver design using 0.18µm CMOS technology with software ADS (Advance Design System) and simulated the results are compared with similar tasks.

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Index Term: LNA , WB , WLAN,ADS(Advance Design System)

I. INTRODUCTION

Communication technology is moving toward a major milestone. The explosive growth of the wireless industry, global access to the internet, and the ever increasing demand for high speed data communication are spurring us toward rapid developments in communication technology. Cellular phones, pagers, wireless local area networks (WLAN), global positioning system (GPS) handhelds, and short-range data communication devices employing Bluetooth and ultra wideband (UWB) technologies are all examples of portable wireless communication devices [1]-[4]**.** An irreplaceable component of any RF receiver is the front-end low-noise amplifier (LNA). As the first active building block in the receiver front-end, the LNA should provide considerable gain while minimizing the noise introduced to the system. Fig. 1 depicts the simplified structure of an RF receiver. The received signal is typically filtered, amplified by an LNA and translated to the base-band by mixing with a local-oscillator (LO)**.** After being demodulated, the signal is applied to an analog-to-digital converter (ADC) which digitizes the analog signal. The digital signal is then processed in a digital signal processing unit (DSP)[5]-[9]. As can be seen, the first step of signal amplification is done by the LNA. Therefore, the performance of LNA can greatly affect sensitivity and noise parameters of the overall receiver

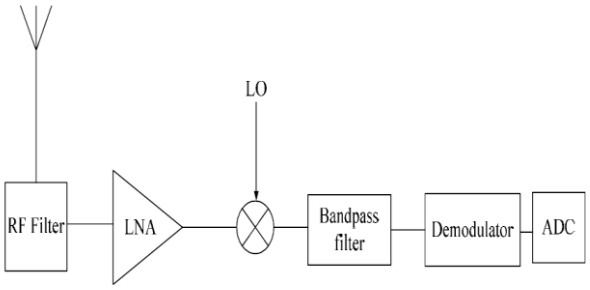

Figure 1.Block diagram of a simplified RF receiver

II. CIRCUIT ANALYSIS

The actual configuration of the common-gate stage (see Fig. 3) is more complex than that shown previously in Fig. 2(d).An inductor,Ls , is placed between the source of the MOS transistor and the ground terminal forming an *LC* resonator with the gate-to-source capacitance Cs in common-gate configuration.The finite output resistance of the transistor also influences the performance of the LNA. It is observed in Fig. 3 that the load impedance of the common-gate stage and the input impedance of the next stage will degrade the matching and noise performance due to the short-channel MOS transistor's relatively low output resistance which is generally around 500 Ω for a 0.18- m CMOS process [10]. The relatively low gain of a common-gate amplifier is another important design consideration, as 15 dB of gain is targeted to amplify the received UWB signal. The small-signal model of the transistor employed in the analysis is given in Fig. 4(a), in which the gate-to-drain parasitic capacitance C_{gd} and the finite output resistance R_0 are both included to observe the influence of the important parasitics on the performance of the proposed LNA

III. INPUT MATCHING

The small-signal equivalent circuit for the impedance calculation is given in Fig. 4(b). Z_L is the impedance of the load Z_{in2} is the input impedance of the next stage and

g_{m1} is the transconductance of the MOS transistor in common-gate configuration.The input impedance can be derived as :

$$Z_{in} = \frac{1}{g_{m1} + \frac{1}{Z_s(\omega)} + \frac{1 - g_{m1}Z_0(\omega)}{R_0 + Z_0(\omega)}} \quad (1)$$

where$Z_s(w)$ and $Z_0(w)$ are given by (3) and (4) below, respectively

$$Z_S(\omega) = j\omega L_S // \frac{1}{j\omega C_{gs}} = \frac{j\omega L_s}{1 - \omega^2 C_{g\delta} L_s} \quad (2)$$

$$Z_0(\omega) = \frac{1}{j\omega C_{gd}} // Z_L // Z_{in2} \quad (3)$$

In fact, the term $(1\text{-}gm1Z_0(w))/(r_0+Z_0(w))$in the denominator of (2) is introduced by the finite output resistance of the MOS transistor due to channel length modulation effect. To obtain more insight on the impact of on the input impedance, we may assume that and are both composed of high- inductors and capacitors and can thus be regarded as purely reactive within the frequency band of interest

$$Z_S(\omega) = jX_S(\omega) \quad (4)$$

$$Z_0(\omega) = jX_0(\omega). \quad (5)$$

Equation (2) can be re-written by substituting (4) and (5) into (2) and we get:

$$Z_{in} = \frac{1}{g_{m1} - j\frac{1}{X_S(\omega)} + \frac{1 - jg_{m1}X_0(\omega)}{R_0 + jX_0(\omega)}}$$

$$= \frac{1}{\left(g_{m1} - \frac{g_{m1}.X_0^2(\omega) - R_0}{R_0^2 + X_0^2(\omega)}\right) - j\left(\frac{1}{X_S(\omega)} + \frac{1 + g_{m1}.R_0}{R_0^2 + X_0^2(\omega)}.X_0(\omega)\right)} \quad (6)$$

The term1/Xs(w) in (6) dominates the imaginary part because $g_{m1}R_0X_0(w) << R_0^2+X_0^2$ (w) throughout the frequency of interest. Since $g_{m1}R_0X_0(w) << R_0^2+X_0^2$ (w), the real part in the denominator will remain relatively constant within the 3.1–10.6-GHz UWB band.

IV. GAIN ANALYSIS

In order to effectively amplify the low PSDUWB signal at the receiver, a relatively high gain is desired for the LNA. For example,the LNA proposed in [11] provides a gain of 15 dB over the UWB bandwidth, and even higher gain is targeted in the design stage so as to compensate for the possible implementation loss due to process variations. Meanwhile, as the development of the other blocks in the UWB receiver front-end is still on the way, a variable gain mechanism is desired in the LNA so that it can be incorporated into different UWB receivers with different link budgets without significant modifications. In general, a resistor is employed as the load of a wide-band amplifier with a series inductor. This combination boosts the load impedance at high frequency. However, such a load is not applicable for a common-gate LNA because the resistor substantially degrades the noise performance of the circuit. Thus, a single inductor serves as the load for our design. It resonates with the total capacitance at the output of the common-gate stage, but limits the bandwidth of the amplifier. A new technique is introduced here to broaden the bandwidth while enhancing the gain of the amplifier. Two common-source stages with inductive loads are added after the common-gate stage to increase the gain of the amplifier. The three inductive loads are selected so that they resonate with the total capacitance at the output node of each stage at three different frequencies within the 3.1- to 10.6-GHz band. Consequently, with proper tuning of the three frequency points, the bandwidth and the gain of the amplifier are both enhanced.Fig. 2 illustrates the proposed bandwidth and the gain enhancement technique, and shows the simulation result for the power gain. The graph indicates that a relatively high while flat gain of 15.4–18.7 dB is achieved on the 3.1- to 10.6-GHz UWB band justifying our enhancement technique. However,
more have to be done to compensate for the implementation losses. As can be found in many wide-band amplifier design works, the measured gain is less than the simulated gain, which is probably due to the EM radiation loss

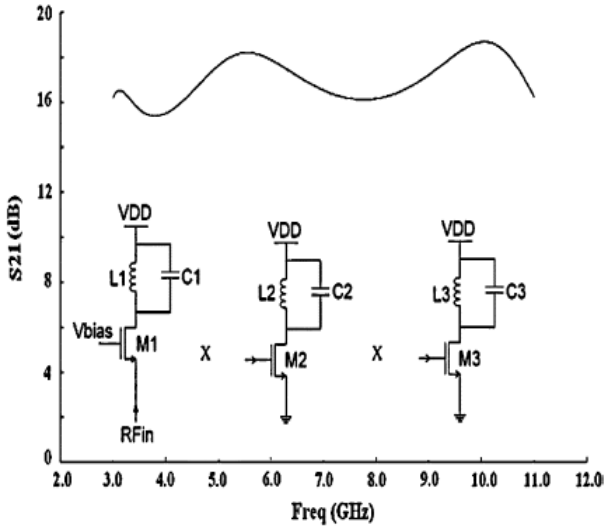

Fig. 2. Illustration of the gain and bandwidth enhancement method with simulation result.

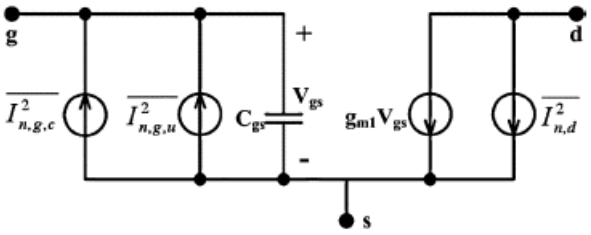

Fig.3. MOS transistor noise model including the induced gate noise.

and the substrate loss of the silicon process. Furthermore, such loss increases with frequency. Therefore, the loss at the high-end of the frequency band is assumed to be 3 dB higher than that at the low-end around the nominal gain of 15 dB, and this assumption is verified in Section V by the post-layout simulation, in which the substrate loss has been taken into consideration

V. Noise Analysis

Extra attention should be given to the noise characteristics of the proposed LNA as it employs a common-gate stage to achieve wide-band input matching, which is generally noisier than the narrow-band matching techniques such as inductive
source degeneration. In order to optimize the noise performance, the MOS transistor noise model with the induced gate noise and the channel thermal noise is employed for the analysis (see Fig. 3) [12]. In Fig. 3, is the PSD of the channel thermal noise which is given as:

$$\frac{\overline{i_{n,d}^2}}{\Delta f} = 4kT\gamma g_{do} \quad (7)$$

where is the Boltzmann constant, is the absolute temperature in Kelvin, is the zero-bias drain conductance, and is the bandwidth over which the noise figure is measured [12]-[14]. The PSD of the induced gate noise is given by:

$$\frac{\overline{i_{n,g}^2}}{\Delta f} = 4kT\delta g_g \quad (8)$$

where is the coefficient of the induced gate noise and is the equivalent shunt gate conductance, which is given by increases in short-channel devices :

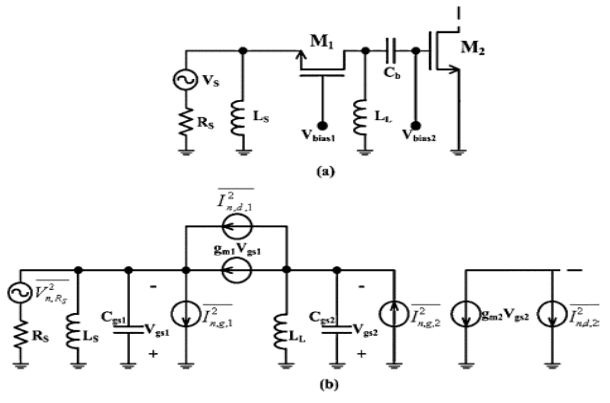

Fig. 4. Noise calculation of the common-gate stage cascaded by a commonsourcestage. (a) Basic schematic. (b) Equivalent small-signal circuit.

The induced gate noise is partially correlated with the channel thermal noise, with a correlation coefficient c, given by:

$$c = \frac{\overline{i_g\, i_d^*}}{\sqrt{\overline{i_g^2}\,\overline{i_d^2}}} \quad (9)$$

Theoretically, for long-channel devices with the noise current direction defined in Fig. 3, and its magnitude decreases as the channel gets shorter [12]-[14]. Thus, the induced gate noise can be divided into two parts as shown in Fig. 3: The firstpart is fully correlated with the channel thermal noise with a PSD given by:

$$\overline{i_{n,g,c}^2}/\Delta f = 4kT\delta g_g |c|^2 \quad (10)$$

and the second part is fully uncorrelated with the channel thermal noise with a PSD given by:

$$\overline{i_{n,g,u}^2}/\Delta f = 4kT\delta \cdot g_g \cdot (1 - |c|^2) \quad (11)$$

.Due to the low gain of the common-gate stage, the noise contribution of the subsequent stages cannot be simply neglected. We perform the noise figure calculation at the output of the second common-source stage so as get a more accurate approximation of the noise performance of the whole amplifier. Based on the schematic of the circuit for noise analysis and its smallsignal equivalent circuit given in Fig. 8, the output noise PSD contributed by the source resistor is given as:

$$S_{n,R_s} = \frac{4kTR_s g_{m1}^2 g_{m2}^2 |Z_0(\omega)|^2}{(1 + g_{m1}R_s)^2 + \frac{R_S^2}{|Z_S(\omega)|^2}} \quad (12)$$

The noise contributed by the part of the induced gate noise in that is fully uncorrelated with the drain noise is given by:

$$S_{n,g,u,1} = \frac{4kT\alpha\delta.(1-|c|^2).\omega^2 C_{gs1}^2 R_s^2 g_{m1} g_{m2}^2 |Z_0(\omega)|^2}{5.\left[(1 + g_{m1}R_s)^2 + \frac{R_S^2}{|Z_S(\omega)|^2}\right]} = \frac{\alpha\delta.(1-|c|^2).\omega^2 C_{gs1}^2 R_s}{5.g_{m1}}.S_{n,R_S}. \quad (13)$$

VI. SIMULATION AND RESULT

The circuit simulations of the proposed design are performed in ADS (Advance Design System) that show in figure5.TableIII summarizes the performance of the proposed CMOS UWB LNA and makes a comparison of the circuit with the recently reported designs. All the wide-band LNA works compared here are based on the conventional transistor-amplifier architecture.The design of the proposed CMOS UWB LNA is based on the Chartered Semiconductor Manufacturing (CHRT) 0.18-µm 1.8-V standard RFCMOS technology.For high frequency performance and minimum parasitic capacitances, a minimum channel length of 0.18 m is chosen for all the transistors employed in the proposed circuit.

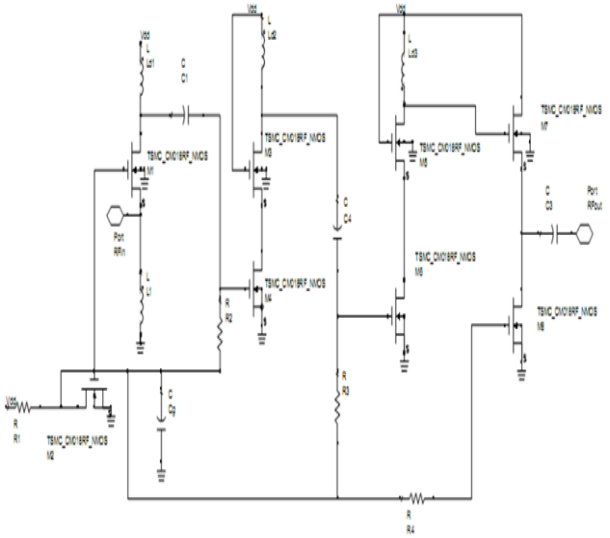

Fig.5. Schematic of the proposed CMOS UWB LNA (with biasing circuit).

A source-follower has been added as an output buffer for testing purposes. The output impedance is given as:

$$Z_{out}(\omega) = \frac{1 + j\omega Z_3(\omega) C_{gs6}}{g_{m6} + j\omega C_{gs6}} // \gamma_{06} // \gamma_{07} \approx \frac{1 + j\omega Z_3(\omega) C_{gs6}}{g_{m6} + j\omega C_{gs6}}$$

(14)

The -factor of the inductors in modern CMOS technology generally vary significantly with frequency,thus a feedback resistor is introduced between the drain of and , to damp the -factor of for better gain flatness. The circuit is biased by means of current mirrors. To minimize the power consumption, the common-gate stage shares the same current mirror that biases the source-follower, while the two cascode stages shares another. The resistors are added for signal choking, while ensures good reverse isolation by forming a low pass filter with . By adjusting the resistance of , we can determine the biasing current and the transconductance of both cascode stages to adjust the overall gain of the LNA.

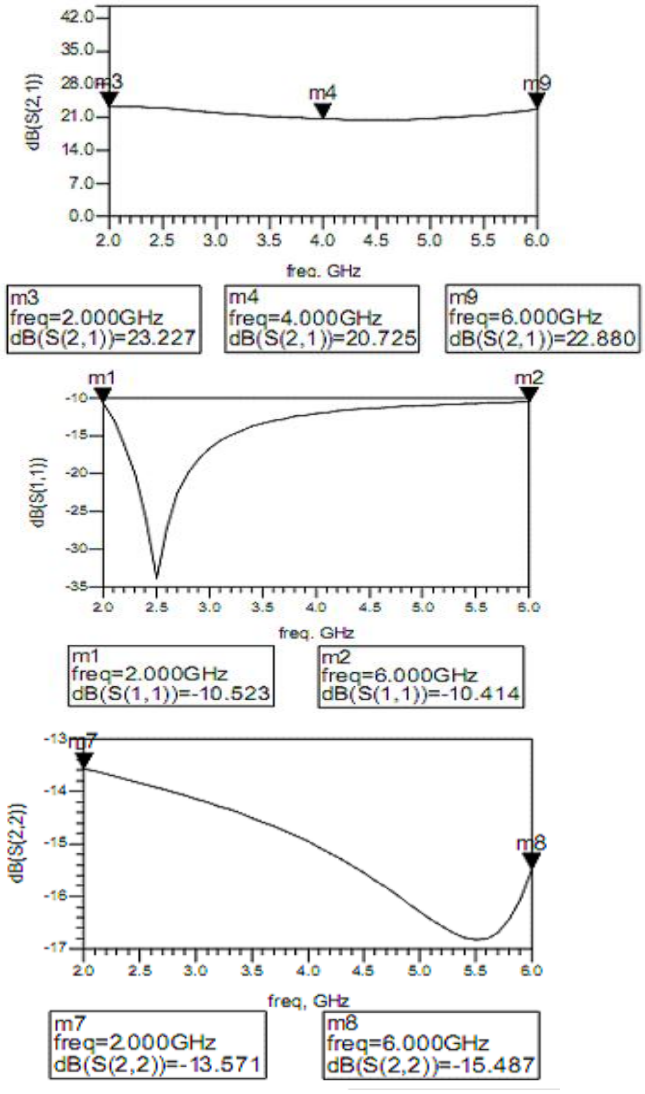

Fig.6. Output matching and reverse isolation.

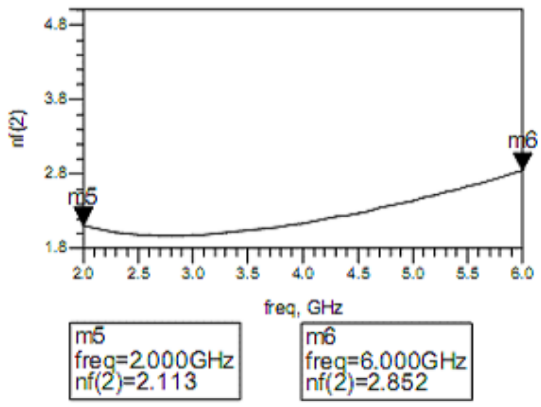

Fig.7. Noise figure.

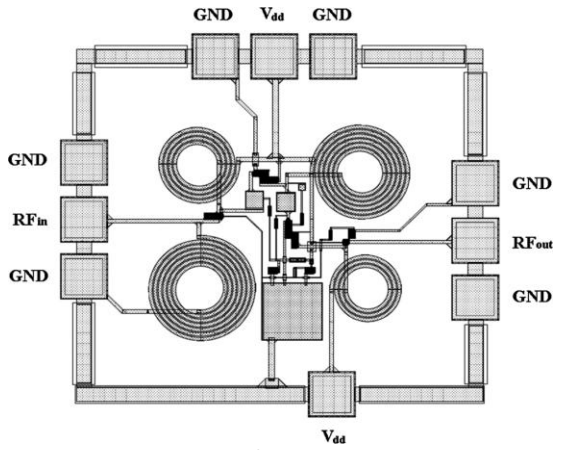

Fig.8. Layout of the proposed circuit.

In Fig. 8, the layout design of the proposed CMOS UWB LNA is shown. The die size is 0.50 mm (0.74 mm 0.67 mm), including the pads and the guard ring.

VII. CONCLUSION

The simulation results show that the proposed LNA gives a low noise and loss power to other devise .Table.1 summarizes the performance of the proposed CMOS UWB LNA and makes a comparison of the circuit with the recently reported designs. All the wide-band LNA works compared here are based on the conventional transistor-amplifier architecture. You can see this circuit .in general ,active elements used in the circuit can be implemented with appropriate filters at the input and output of this circuit is transformed into a UWB.Also, this circuit can use in IEEE 802.11.a and IEEE 802.11.b standard's of WLAN.

Ref	Tech	S_{11}[db]	S_{22}[db]	G_{max}[db]	B[GHz]	NF_{avg}[db]	Sup.voltage	P_{diss}[mW]
This work	0.18µm CMOS	< -10.14	< -13.5	21.62	2 - 6	2.53	1.8	13.05
[1]	0.18µm CMOS	< -8	< -10.5	17.0	3.1-4.8	3.9	1.8	21
[5]	0.6µm CMOS	< -7	< -9	7.4	0.5-4	5.5	3	83.4
[6]	018µm CMOS	< -9	< -12	16.5	2.0-5.2	4.7	1.8	38
[7]	0.25µm CMOS	< -8	< -13	13.7	2 - 4.6	1.9	2	35
[13]	0.18µm CMOS	< -6	< -11	7	1.5-7.5	8.7	1.8	21.6
[18]	0.18µm CMOS	< -7.2	< -9	13.1	1-7	3.3	1.8	75
[21]	0.18µm CMOS	< -5.3	< -14	13.2	5 - 5.96	2.59	1.8	22.2

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