# New Design Of A 0.18µm CMOS Low Power High Frequency Four Quadrant Multiplier

Milad Kaboli
Sama technical vocational training college, islamic azad university, mahshahr branch, mahshahr, iran
Kaboli.m@iauo.ac.ir

## ABSTRACT

A new CMOS low voltage current-mode four-quadrant analog multiplier based on squarer circuit with voltage output is presented. The proposed circuit is composed of a pair of current subtractors, a pair differential-input V-I converters and a pair of voltage squarers. The circuit was simulated using HSPICE simulator in standard 0.18 µm CMOS level 49 MOSIS (BSIM3 V3.2 SPICE-based). Simulation results show the performance of the proposed circuit and experimental results are given to confirm the operation. This topology of multiplier results in a high frequency capability with low power consumption.
The multiplier operates for a power supply ±1.2V. The simulation results of analog multiplier demonstrate a THD of 0.96% in 10MHz, a −3dB bandwidth of 2GHz and a maximum power consumption of 5.6mW.

## INTRODUCTION

At present, battery-power system requires circuits which operate on low voltage supply and low power consumption. Thus, demands for analog circuits that can operate at low voltage supply are very high. The analog multiplier circuit is one of the important building blocks in VLSI communication systems, which can be applied to frequency mixers, variable gain amplifiers, adaptive filters, phase-locked loops and much other signal processing circuit. Several low-voltage CMOS multipliers have been presented using CMOS transistors operated in the triode region [1-2] and saturation region [3-6], the saturation region design will have the batter frequency response, so this paper proposes the saturation region design.
The four-quadrant multiplier is a very important building block of analog signal processing system. It has many applications in automatic gain controlling, phase-locked loops, modulation, detection, frequency translation, square rooting of signals and neural networks. To implement the multipliers in IC technologies, the Gilbert cell is a popular structure in bipolar IC technologies due to its wide dynamic range and high frequency performance [12].
However, the characteristics of MOS devices and bipolar devices are different, thus the MOS version of Gilbert cell [13-15] requires extra linearization circuits which degrade the circuit performance. These have either high voltage (and/or power) supply requirements [14], poor linearity or low output (current) signal levels [15]. Recently, some four-quadrant multipliers suitable for low voltage operation have been developed [16-18], but other features of which such as dynamic range and frequency performance are limited. In this paper, we propose a new CMOS four-quadrant analog multiplier based on the squarer-algebraic identity in MOS saturation region. The multiplier performs the product of two continuous signals x and y, yielding an output z = Kxy, where K is a constant with suitable dimension. In this paper, we present a low-power, high-speed four- quadrant analog multiplier circuit in current mode.

## CIRCUIT DESCRIPTION

The principle of the proposed multiplier is based on the square-algebraic identity :

$$(I1 + I2)^2 - (I1 - I2)^2 = K\, I1\, I2 \qquad (1)$$

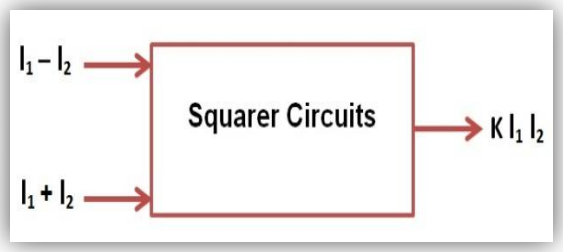



Fig 1. Proposed Circuit Symbol

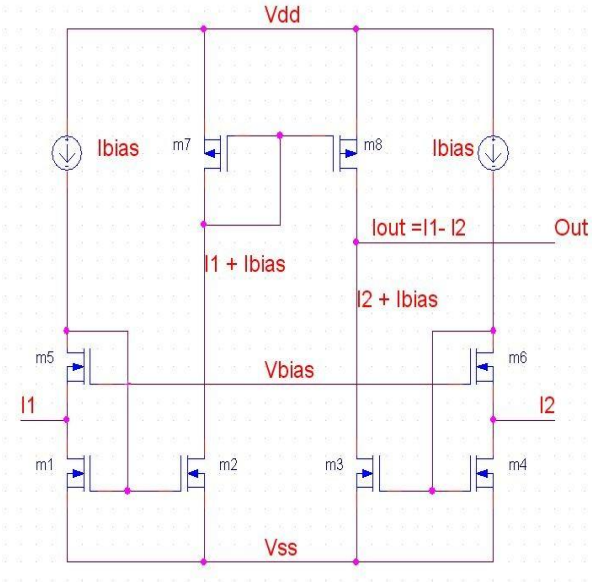
Therefore, the circuit needs two adder-subtractor circuits and two Squarer Circuits.

## CURRENT ADDER-SUBTRACTOR CIRCUIT

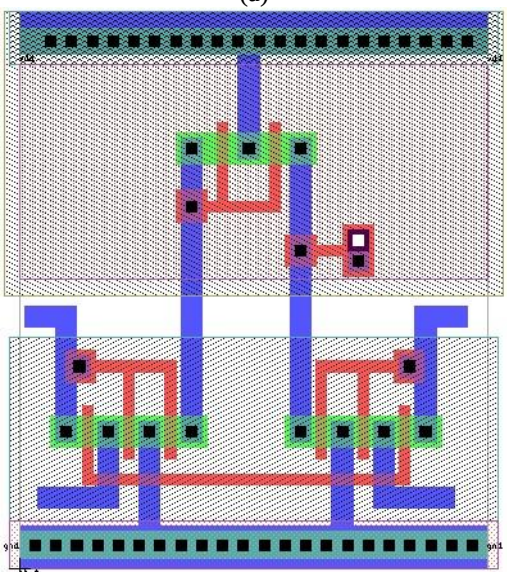
The current adder-subtractor circuit is illustrated in Fig. 2, which consists of the transistors M1 to M8. Current of the terminal-out follows the difference of the currents of terminal-I1 and terminal-I2. Hence, we name terminal-out as current output. The current of the terminal-out can be expressed as follows:

$$Iout = (I1 + Ibias) - (I2 + Ibias) = I1 - I2 \quad (2)$$

By changing the direction of current I2, circuit convert to current adder in terminal-out.
The current source, Ibias forces equal currents of 56 µA in the transistors (M1–M4). Thus, the gate to source voltages of these transistors will be equal, which forces the voltages of the two input terminals to be zero.




(a)



(b)

Fig 2.a. Current Subtractor circuit, Fig.2.b. Layout of the Current Subtractor circuit

**SQUARER CIRCUIT**

Considering the circuit in Fig 3, while M1 and M2 work in saturation region.

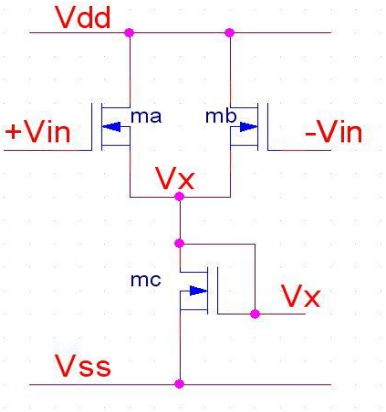



Fig 3. Squarer

The currents through the transistors can be expressed as :

$$IDa = 0.5\,\mu n\,Cox\,W/L\,(VGS1 - VTn)^2 \quad (3)$$

$$IDb = 0.5\,\mu n\,Cox\,W/L\,(VGS2 - VTn)^2 \quad (4)$$

$$K = \mu n\,Cox\,W/L \quad (5)$$

$$VGS > VTn\,, VDS \geq VGS + VTn \quad (6)$$

Where K is the parameter of transistor, µn is the electron mobility, Cox is the gate oxide capacitance per unit area, W/L is the transistor aspect ratio, VGS is the gate-to-source voltage, VDS is the drain-to-source voltage and VTn is threshold voltage of the MOS transistor. Suppose all transistors are identical, then K1=K2=K and VTn1=VTn2=VTn and:

$$IDc = IDa + IDb \quad (7)$$

Where IDc, IDb and IDa is the drain currents of Mc, Mb and Ma.

$$IDc = \frac{K}{2}[(Vin - Vx - VTn)^2 + (-Vin - Vx - VTn)^2\ ] \quad (8)$$

$$IDc = \frac{K\,[(Vin)^4 + 2(Vin)^2(Vss+2VTn)^2 + (Vss+2VTn)^4\,]}{4(Vss+2VTn)^2} \quad (9)$$

For small signal of Vin it can be assumed that $Vin^4 \approx 0$.
Then, the output current can be expressed as the simple input signal squarer as follows:

$$IDc = \frac{K}{2}(Vin)^2 + \frac{K}{4}(Vss + 2VTn)^2 \quad (10)$$

The voltage at Vx can be derived from using small signal model that is :

$$VX = \frac{K}{2}gm(Vin)^2 + \frac{K}{4}gm(Vss + 2VTn)^2 \quad (11)$$

**I to V conventer**

Figure 4 is an I to V converter that consists of 2 same aspect ratio of MOSs and operates in the saturation region.

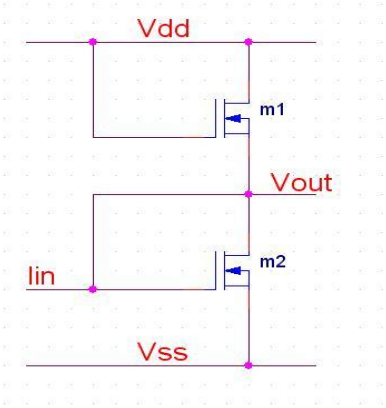



Fig 4. I to V Converter

$$ID1 = 0.5\,K\,(VDD - Vout - VTn)^2 \quad (12)$$

$$ID2 = 0.5\,K\,(Vout - VSS - VTn)^2 \quad (13)$$

$$(VDD - VTn) = -(VSS + VTn) \quad (14)$$

$$Iin = ID2 - ID1 \quad (15)$$

$$Iin = 2\,K\,Vout\,(VDD - VTn) \quad (16)$$

$$Vout = \frac{Iin}{2\,K\,(VDD - VTn)} \quad (17)$$

**INVERTER CIRCUIT**

Figure 5 is an inverter that consists of 2 same aspect ratio of MOSs and operates in saturation region.

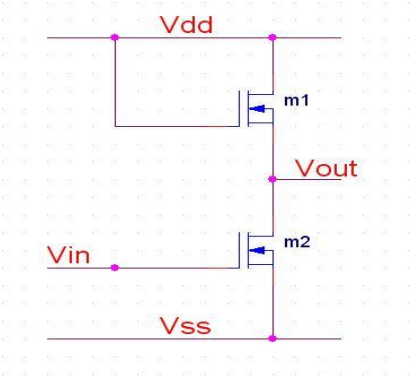



Fig 5. Inverter

$$ID1 = 0.5\,K\,(VDD - Vout - VTn)^2 \quad (18)$$

$$ID2 = 0.5\,K\,(Vout - VSS - VTn)^2 \quad (19)$$

$$VGS1 = VGS2 \quad (20)$$

$$(VDD - Vout) = (Vin - VSS) \quad (21)$$

$$Vout = -Vin \quad (22)$$

Merging the I to V converter and the inverter, as shown in Figure 6 and Figure 7, yields the nodes and V1, V2, V3 and V4 voltages bellow.

$$V1 = \frac{IX + IY}{2\,K\,(VDD - VTn)} \quad (23)$$

$$V2 = \frac{-IX - IY}{2\,K\,(VDD - VTn)} \quad (24)$$

$$V3 = \frac{IX - IY}{2\,K\,(VDD - VTn)} \quad (25)$$

$$V4 = \frac{-IX + IY}{2\,K\,(VDD - VTn)} \quad (26)$$

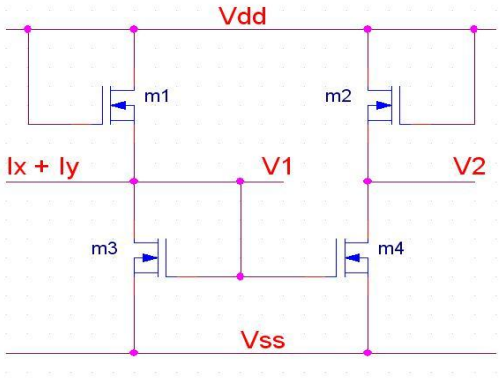



Fig 6. . I to V converter and Inverter with feed input of $I_X + I_Y$

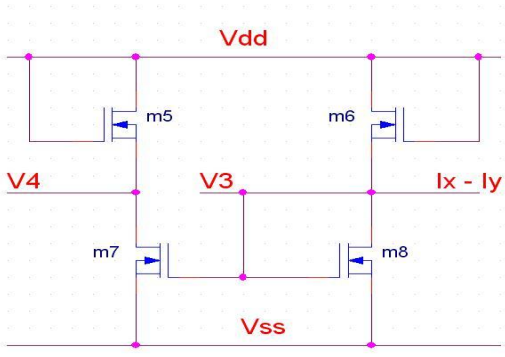



Fig 7. I to V converter and Inverter with feed input of $I_X - I_Y$

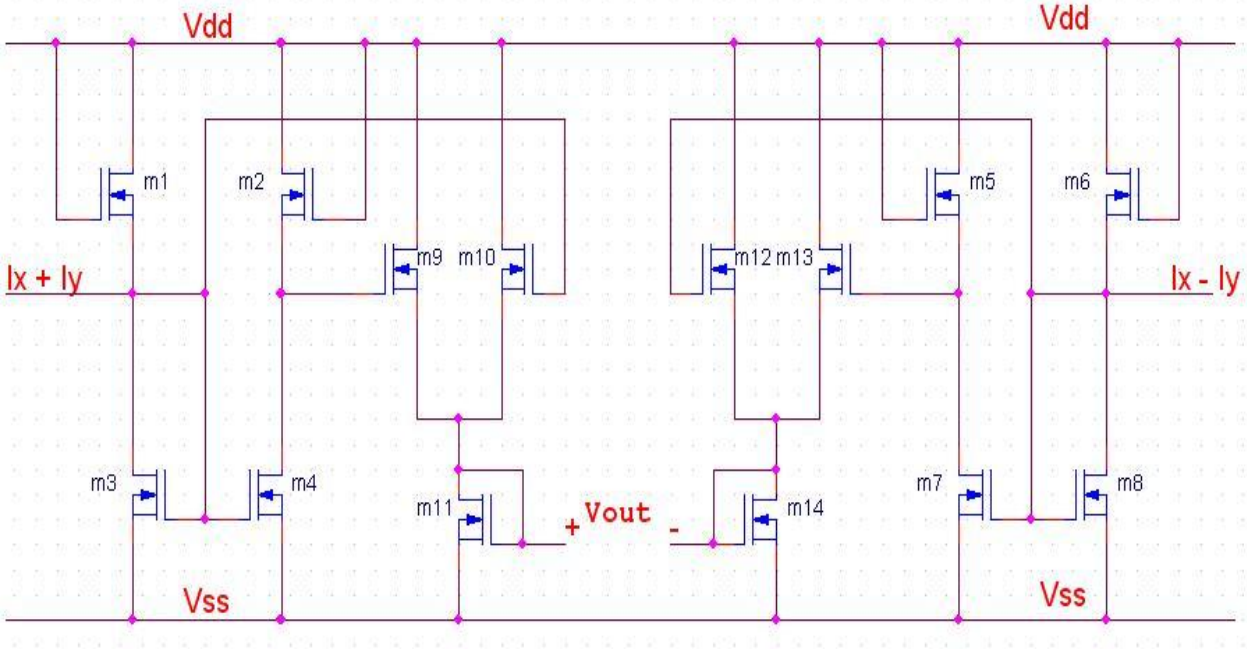
**PROPOSED CIRCUIT**

The proposed square circuit, shown in Fig 8 comprises 14 NMOS transistors.

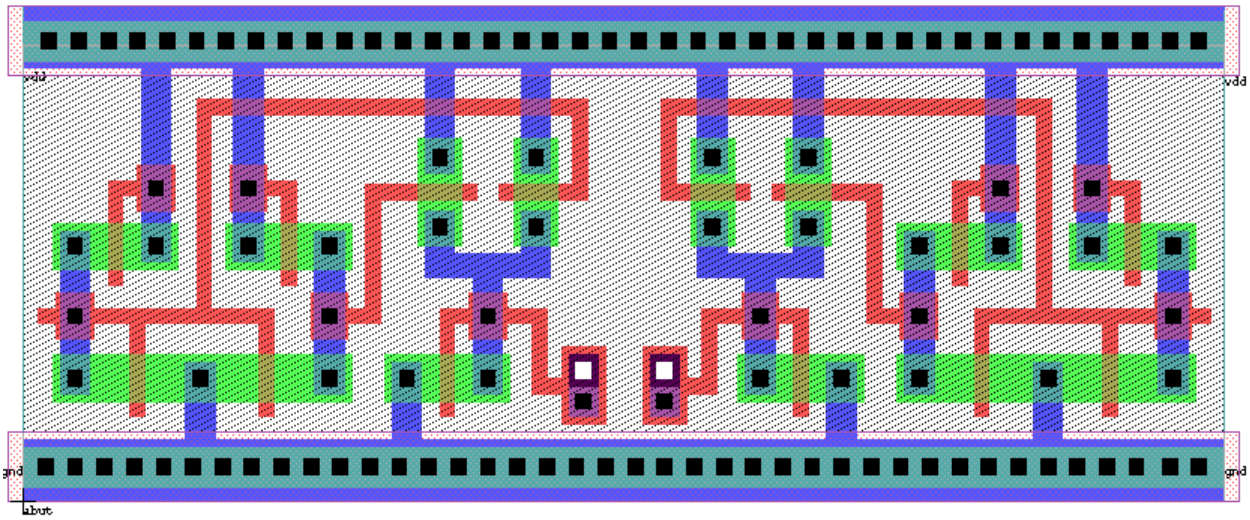
$$\text{Vout} + = \frac{K}{2}\text{gm}(\text{V1} - \text{V2})^2 + \frac{K}{4}\text{gm}(\text{Vss} + 2\text{VTn})^2 \quad (25)$$

$$\text{Vout} - = \frac{K}{2}\text{gm}(\text{V3} - \text{V4})^2 + \frac{K}{4}\text{gm}(\text{Vss} + 2\text{VTn})^2 \quad (26)$$

$$\text{Vout} = (\text{Vout} +) - (\text{Vout} -) \quad (27)$$




(a)



(b)

Fig 8.a Proposed Multiplier , Fig.8.b. Layout of the proposed multiplier circuit

**SIMULATION RESULT**

The complete circuit of the current multiplier is viewed in Figure 8, and the simulation use 0.18µm CMOS and simulate with H-Spice level 49 MOS aspect ratio shown in Table 1.

The simulation result of the DC characteristic can be seen in Figure 9. Input of Ix and Iy current are -100µA to +100µA by Ix increase from -100µA to +100µA and Iy sweep from -100µA to +100µA in 5 (five) steps, as we can see in Figure 9.

Table 1. Aspect ratio of MOS transistor

| MOS Transistor | W/L |
|---|---|
| M9-M14 | 10u/0.5u |
| M1-M8 | 0.5u/0.5u |

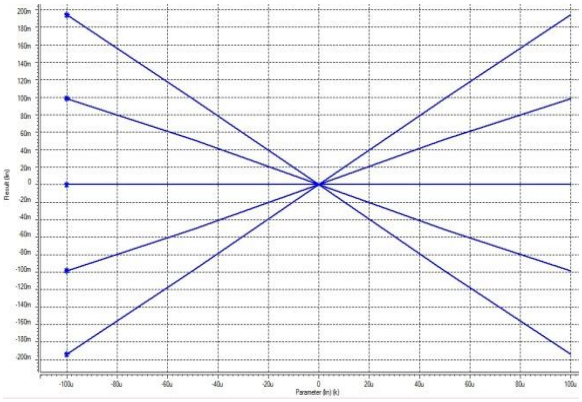


Fig 9. The Transfer Characteristic Curve Of The Multiplier

Figure 10 shows about frequency response. The frequency increases from 100 kHz to 100 GHz. The simulation result measures that -3dB of the frequency is about 2 GHz and offset of current sweep from 5µA to 25µA in 5 (five) steps.

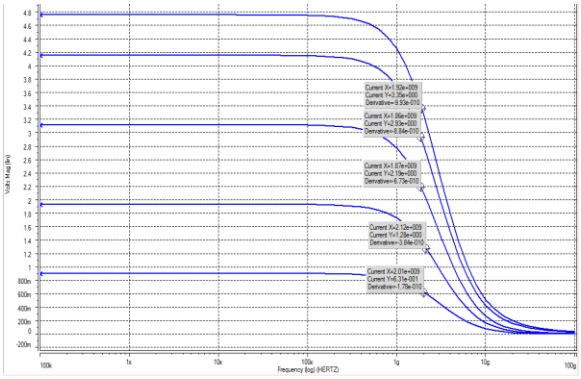


Fig 10. AC Transfer Characteristics Of The Multiplier

Figure 11 shows about the total harmonic distortion (THD). We feed Iy current 1 value that is +10 µA. Ix is sine wave by amplitude 10µA, and the frequency from 1 kHz to 1GHz.
As seen in the THD graph, when Iy is +10µA, THD is approximately 0.96% until the frequency increase to 10 MHz, where THD starts to increase. The maximum THD is 2.91% at 1 GHz.

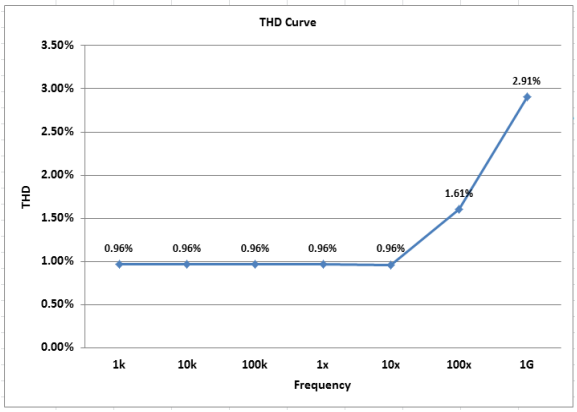



Fig 11. Relation Between THD And Frequency

The next is about the multiplier circuit that is applied in modulator. $I_x$ is 50µA and has frequency 1 MHz, while Iy is a carrier signal, with frequency 10 MHz, and amplitude 50µA as we can see in Figure 12 and Figure 13. The modulated frequency is shown in Figure 14.

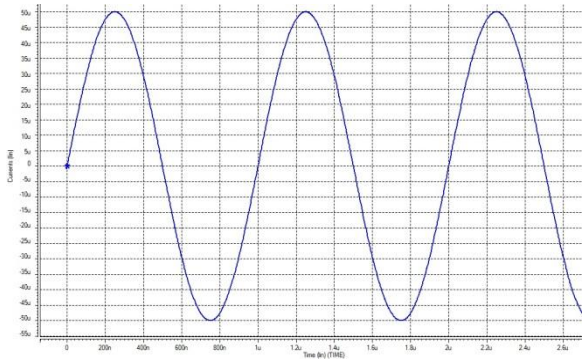


Fig 12. Sinusoidal Input Signal

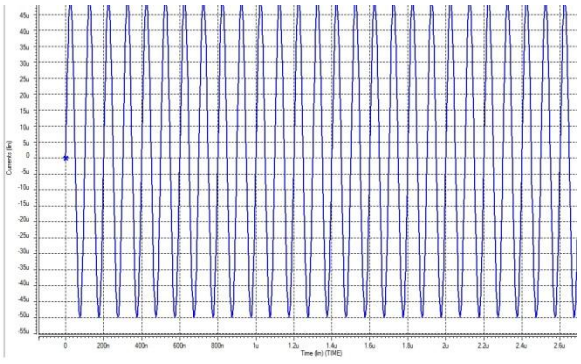


Fig 13. Sinusoidal Input Signal

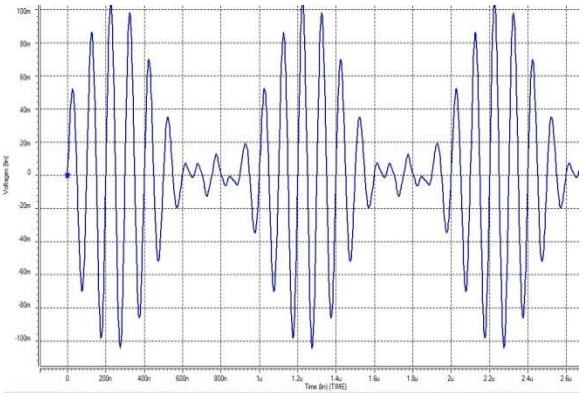


Fig 14. Amplitude Modulation Of The Two Sinusoidal Input Signal

## CONCLUSION

A current multiplier circuit using ±1.2V voltage supply is proposed in this article. Frequency response of the circuit is 2 GHz. Other Value of Simulation is shown in Table 2.

Table 2. Other Value of Simulation and simulation result

| Parameter | Value |
|---|---|
| Technology | 0.18 µm CMOS |
| Supply voltage | ±1.2 |
| CMOS Amount | 14 |
| Bandwidth | 2GHz |
| Power dissipation | 5.6mW |
| THD(%) | 0.96% |

## ACKNOWLEDGMENT

This paper was resulted from research proposal entitled "New Design Of A 0.18µm CMOS Low Power High Frequency Four Quadrant Multiplier" which is supported by Sama technical vocational training college, islamic azad university, mahshahr branch, mahshahr, iran.

## REFERENCES

[1] S.-L. Lin. _low Voltage CMOS Four-Quadrant multiplier,_*Electron.Lett.*,vol.30,pp..2125.2126,1994.

[2] J.-H. Tsay, S.-I. Lin, J.-J.Chen and Y.-P. Wu._CMOS four-quadrant multiplier using triode transistors based on regulated cascode structure,_ *Electron,Lett.,* vol.31,no.12, pp. 962-963,1995.

[3] J.S.Pena-Finol and J.A. Connelly, _AMOS fourquadrant analog multiplier using the quarter-square technique,_ *IEEE J.solid-state circuits*, vol.SC-22, pp.1067-1073, Dec.1987.

[4] B. Gilbert, ``A precision four-quadrant multiplier with nanosecond response.'' IEEE Journals of Solid State Circuits SC- 3(6), pp. 353±365, 1968.

[5] Journals of N. Babanezhad and G. C. Temes, ``A 20V fourquadrant CMOS analog multiplier.'' IEEE Journals of Solid State Circuits SC-20(6), pp. 1158±1168, 1985.

[6] B. S. Bong, ``CMOS RF circuits for data communication applications.'' IEEE Journals of Solid State Circuits SC-21, pp. 310±317, 1986.

[7] S. C. Quin and R. L. Geiger, ``A +5V CMOS analog multiplier.'' IEEE Journals of Solid State Circuits SC-22, pp. 1143±1146, 1987.

[8] A. L. Coban and P. E. Allen, ``Low-voltage four-quadrant analog multiplier.'' Electronic Letters pp. 1044±1045, 1994.

[9] Journals of H. Tsay, S. I. Liu, and Y. P. Wu, ``CMOS fourquadrant multiplier using triode transistors based on regulated cascade structure.'' Electronic Letters, pp. 962±963, 1995.