Designing Of A New 0.18um CMOS Voltage Mode Squar Root Analog Multiplier

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ABSTRACT

A new CMOS low voltage current-mode four-quadrant analog multiplier based on squarer circuit with voltage output is presented. The proposed circuit is composed of a pair of current subtractors, a pair differential-input V-I converters and a pair of voltage squarers. The circuit was simulated using HSPICE simulator in standard 0.18 µm CMOS level 49 MOSIS (BSIM3 V3.2 SPICE-based). Simulation results show the performance of the proposed circuit and experimental results are given to confirm the operation. This topology of multiplier results in a high frequency capability with low power consumption.
The multiplier operates for a power supply ±1.2V. The simulation results of analog multiplier demonstrate a THD of 0.65% in 10MHz, a −3dB bandwidth of 1.39GHz and a maximum power consumption of 7.1mW.

INTRODUCTION

At present, battery-power system requires circuits which operate on low voltage supply and low power consumption. Thus, demands for analog circuits that can operate at low voltage supply are very high. The analog multiplier circuit is one of the important building blocks in VLSI communication systems, which can be applied to frequency mixers, variable gain amplifiers, adaptive filters, phase-locked loops and much other signal processing circuit. Several low-voltage CMOS multipliers have been presented using CMOS transistors operated in the triode region [1-3] and saturation region [2], the saturation region design will have the batter frequency response, so this paper proposes the saturation region design.
A number of circuit techniques for realizing a CMOS analog multiplier had been collected and systematically evaluated by G. Han and E. Sanchez-Sinencio [4]. According to [4], there are several means to realize a four quadrant analog multiplier and it is also suggested by [5] that using saturated MOSFET in strong inversion is more practical than any other means. Recently, based on a square-law relation of saturated MOSFET, various compact multiplier architectures which are constituted by a circuit cell called a "flipped voltage follower: FVF" [6], have been chronologically proposed in [7]-[8]. Most of them feature wide input range, high operating frequency and low power consumption which are resulted from excellent manipulations of the square-law function in high compactness structures. Focusing on the latest version in [8], which is seemed to be the most compact circuit, it is found that the overall multiplier circuit can not be called compact since it requires an extra voltage reference connected between the resistive loads. To generate the extra voltage reference, more power consumption and circuit complexity are unavoidable.
In this paper, we propose a new multiplier circuit which is based on a similar technique to [9] but an arrangement of the circuit in transistor level is improved such that the extra voltage reference becomes redundant and can be eliminated.

BASIC DESCRIPTION

Basic idea of a linearized multiplier using square-root circuit is shown through Fig.1. The output current of a source-couple pair, drain currents of M1 and M2 (Ia and Ib, respectively), are applied to the identical square-root circuits. Injecting the output currents of the input transistors into the square-root blocks, a differential output current of the overall circuit will become a multiplication function of two input signals Vab and Vcd. More detail of mathematical analysis using square-law relation of saturated MOSFET in strong inversion will be shown in the paragraph below.

$$\mathrm{Iout} = \mathrm{Iout1} - \mathrm{Iout2} = \mathrm{K\,Vcd}\,(\sqrt{\mathrm{Ia}} - \sqrt{\mathrm{Ib}}) \quad (1)$$

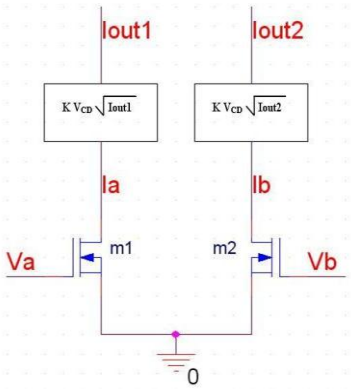


Fig 1. Proposed Circuit Symbol

Assuming the MOSFET M1 and M2 are biased in active region and neglecting channel length modulation effect, the current Ia and Ib can be respectively found as

$$\mathrm{Ia} = \mathrm{Kn}\,(\mathrm{Va} - \mathrm{Vtn})^2 \quad (2)$$

$$\mathrm{Ia} = \mathrm{Kn}\,(\mathrm{Vb} - \mathrm{Vtn})^2 \quad (3)$$

where Kn=0.5 µn Cox (W/L) is a transconductance parameter of each MOSFET and Vtn is the threshold voltage of NMOS transistor.

From (2) and (3), the relationship between the current Ia and Ib and the differential input voltage Vab = Va - Vb can be given by

$$\sqrt{Ia} - \sqrt{Ib} = Vab\sqrt{Kn} \quad (4)$$

The drain currents Ia and Ib are fed into the square root blocks controlled by Vcd, results in

$$Iout = Iout1 - Iout2 = K\,Vcd\,(\sqrt{Ia} - \sqrt{Ib}) \quad (5)$$

where K is the gain of the square root blocks. Substituting (4) into (5), yields

$$Iout = K\,Vcd\,\sqrt{Kn}\,Vab\,Vcd \quad (6)$$

It can be seen that an output current appeared in (6) is in form of a multiplication function between two input signals Vab and Vcd.
Based on this approach, both linear transconductor [9] and four-quadrant analog multiplier [10] have been proposed. Unfortunately, the early works in [9] and [10] require more than 3V for supply voltage which is not sufficiently low for modern analog design. Subsequently, a new square rooting circuit operated under 1.2V single supply was proposed in [11] which can be applied as a compact four quadrant analog multiplier as well [8]. However, the multiplier in [8] is not practical since it requires an ideal voltage reference to create the multiplication function.
In the next section, the improved square root circuit which is more suitable for realizing an analog multiplier will be described.

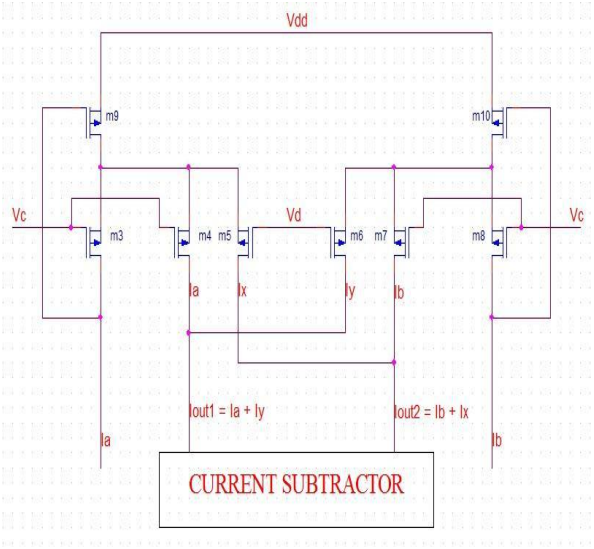


Fig 2. The proposed square rooting circuit.

SQUARE ROOTING CIRCUIT

A proposed square rooting circuit which is improved from [11] is shown in Fig.3. Using square-law relation of saturated MOSFET in strong inversion and setting M3-M8 to be identical, the currents Ix and Iy are found to be

$$Ix = Kp\,(Vcd - \sqrt{\frac{Ia}{Kp}})^2 \quad (7)$$

$$Iy = Kp\,(Vcd - \sqrt{\frac{Ia}{Kp}})^2 \quad (8)$$

where Kp=0.5 μp Cox (W/L) is a transconductance parameter of each PMOS transistor and Vcd = Vc - Vd is a differential control voltage.
Considering (7) and (8) in conjunction with the fact that Ia + Iy = Iout1 and Ib + Ix = Iout2 leading to

$$Iout1 = KpVcd^2 + 2Vcd\,\sqrt{Ia}\,\sqrt{Kp} + Ia + Ib \quad (9)$$

$$Iout1 = KpVcd^2 + 2Vcd\,\sqrt{Ib}\,\sqrt{Kp} + Ia + Ib \quad (10)$$

Subtracting (9) and (10), results in

$$Iout = Iout1 - Iout2 = 2Vcd\sqrt{Kp}(\sqrt{Ia} - \sqrt{Ib}) \quad (11)$$

It is obvious that the output current of the improved square root circuit is a function of a square root of Ia and Ib and its gain can be adjusted by the voltage Vcd and transconductance parameter Kp.

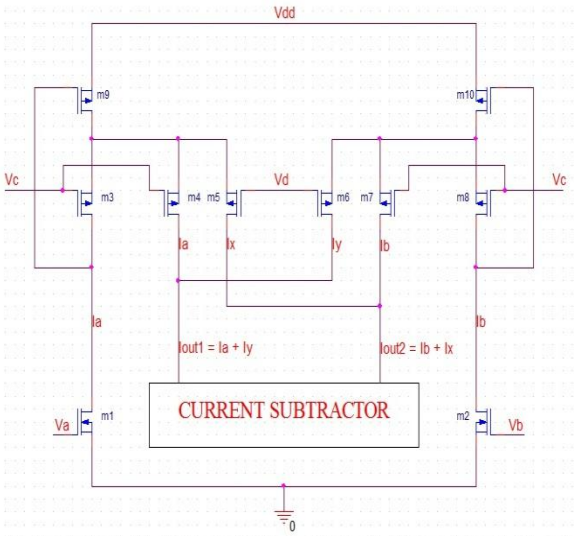


Fig 3. Design of proposed multiplier circuit

I TO V CONVENTER

Figure 4 is an I to V converter that consists of 2 same aspect ratio of MOSs and operates in the saturation region.

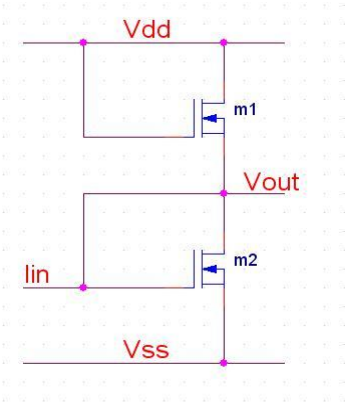


Fig 4. I to V Converter

$$ID1 = 0.5\,K\,(VDD - Vout - VTn)^2 \quad (12)$$

$$ID2 = 0.5\,K\,(Vout - VSS - VTn)^2 \quad (13)$$

$$(VDD - VTn) = -(VSS + VTn) \quad (14)$$

$$Iin = ID2 - ID1 \quad (15)$$

$$Iin = 2\,K\,Vout\,(VDD - VTn) \quad (16)$$

$$Vout = \frac{Iin}{2\,K\,(VDD - VTn)} \quad (17)$$

PROPOSED CIRCUIT

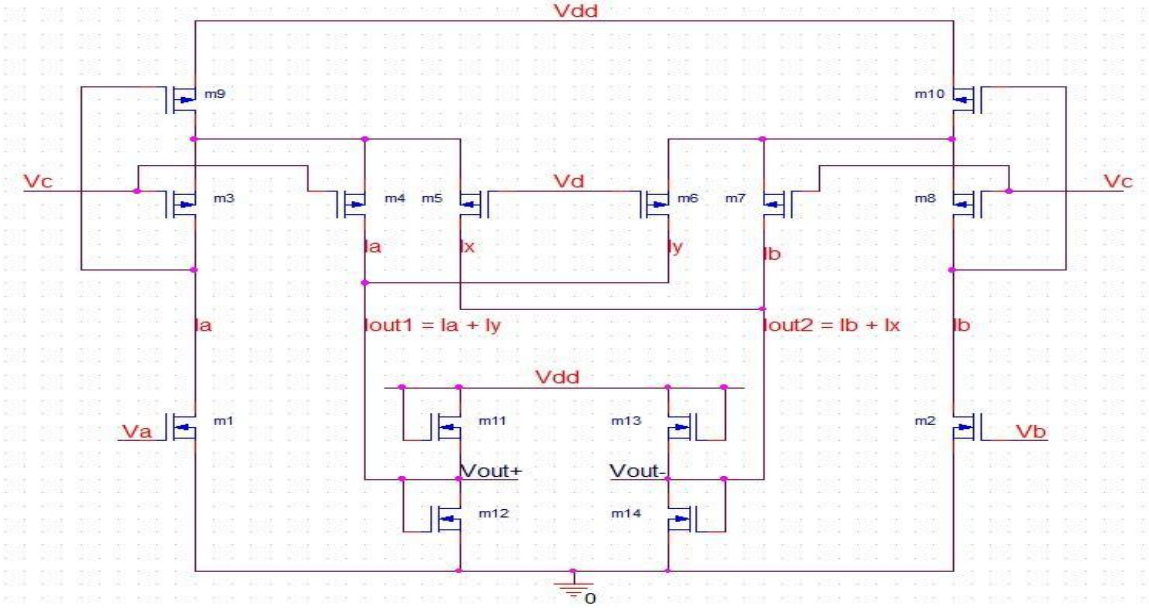
Merging the I to V converter and the square rooting circuit, as shown in Figure 5 comprises 14 NMOS transistors.

The proposed square circuit, shown in Fig 5 comprises 14 NMOS transistors.

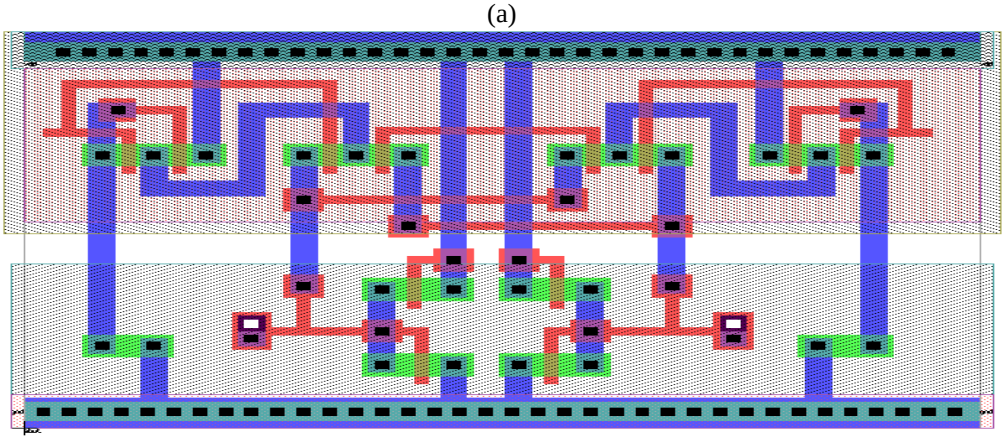
$$Vout+ = \frac{IinKpVcd^2 + 2Vcd\sqrt{Ia}\sqrt{Kp} + Ia + Ib}{2\,K\,(VDD - VTn)} \quad (18)$$

$$Vout- = \frac{IinKpVcd^2 + 2Vcd\sqrt{Ib}\sqrt{Kp} + Ia + Ib}{2\,K\,(VDD - VTn)} \quad (19)$$

$$Vout = (Vout+) - (Vout-) \quad (20)$$



(a)



(b)

Fig 5.a. The proposed multiplier circuit , Fig 5.b. Layout of he proposed multiplier circuit

SIMULATION RESULT

The complete circuit of the current multiplier is viewed in Figure 8, and the simulation use 0.18µm CMOS and simulate with H-Spice level 49 MOS aspect ratio shown in Table 1.

Table 1. Aspect ratio of MOS transistor

MOS Transistor	W/L
M9-M10	10u/0.5u
M1-M8	0.5u/0.5u
M11-M14	1u/0.5u

The simulation result of the DC characteristic can be seen in Figure 6. Input of Vab and Vcd voltage are -100mV to +100 mV by Vab increase from -100 mV to +100 mV and Vcd sweep from -100 mV to +100 mV in 5 (five) steps, as we can see in Figure 6.

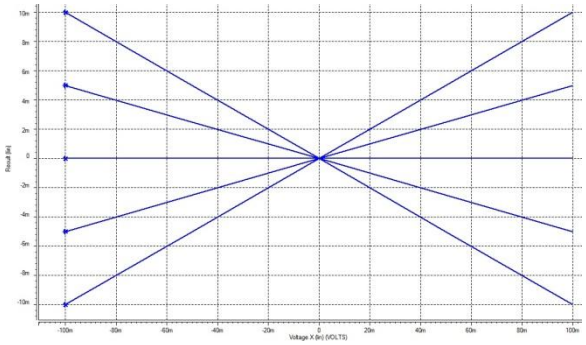


Fig 6. The Transfer Characteristic Curve Of The Multiplier

Figure 7 and figure 8 shows about frequency response. The frequency increases from 1XHz to 100 GHz. The simulation result measures that -3dB of the frequency is about 1.39 GHz and offset of voltage sweep from 0.7V to 1.V in 3 (three) steps for Vab in figure 7 and 0.6V to 1V in 3 (three) steps for Vcd in figure 8 .

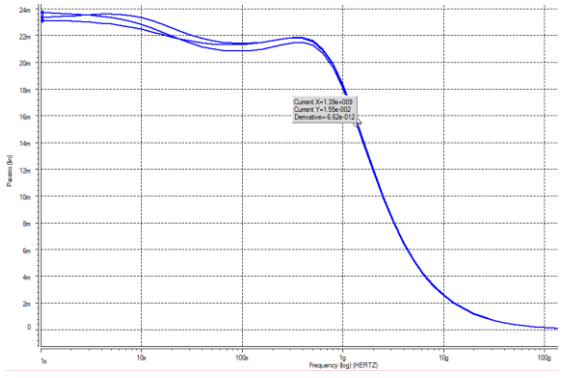


Fig 7. AC Transfer Characteristics Of The Multiplier

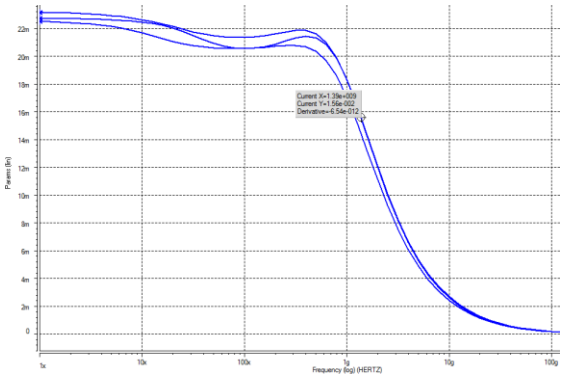


Fig 8. AC Transfer Characteristics Of The Multiplier

Figure 8 shows about the total harmonic distortion (THD). We feed Iy current 1 value that is +10 µA. Ix is sine wave by amplitude 10µA, and the frequency from 1 kHz to 1GHz.
As seen in the THD graph, when Iy is +10µA, THD is approximately 0.65% until the frequency increase to 10 MHz, where THD starts to increase. The maximum THD is 3.90% at 1 GHz.

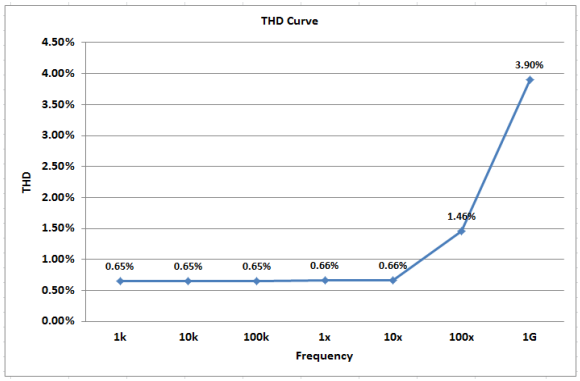


Fig 9. Relation Between THD And Frequency

The next is about the multiplier circuit that is applied in modulator. Ix is 10µA and has frequency 500 MHz, while Iy is a carrier signal, with frequency 5 GHz, and amplitude 5µA as we can see in Figure 10 and Figure 11. The modulated frequency is shown in Figure 12.

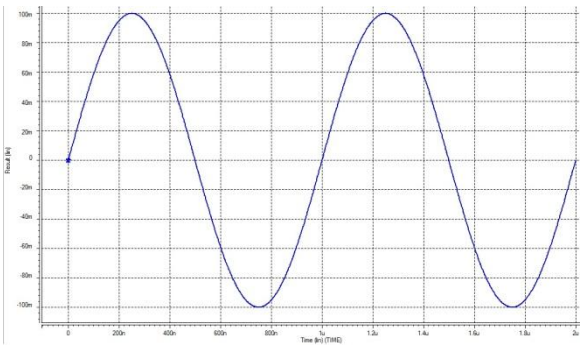


Fig 10. Sinusoidal Input Signal

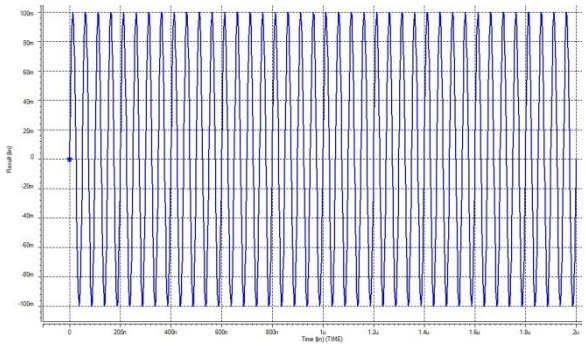


Fig 11. Sinusoidal Input Signal

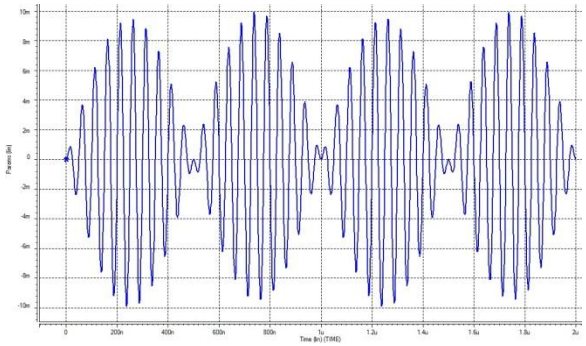


Fig 12. Amplitude Modulation Of The Two Sinusoidal Input Signal

CONCLUSION

A current multiplier circuit using ±1.2V voltage supply is proposed in this article. Frequency response of the circuit is 1.39 GHz. Other Value of Simulation is shown in Table 2.

Table 2. Other Value of Simulation and simulation result

Parameter	Value
Technology	0.18 μm CMOS
Supply voltage	±1.2
CMOS Amount	14
Bandwidth	1.39GHz
Power dissipation	7.1mW
THD(%)	0.65%

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