A Review on Multiple Cell Upset Data Correction using Decimal Matrix Code for Enhanced Memory Reliability

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***Abstract*—The data stored in memory needs to be considered for the reliability for its content stored when the memory is exposed to the radiation environment in case of transient multiple cells upsets (MCUs). In order to protect the data from the radiation and transients there are many advanced packaging techniques are suggested. The particular packaging technique provides safety from a limited variation of radiations. The devices used for the present wireless communication field are subject to the exposed radiations of the surrounding environment. In such conditions of radiations few data protection techniques are preferred to use for authenticating the data before using it for further process. One of the techniques used for this is Error correction code. The encoded data is then stored in memory place by utilizing the protection technique. The redundant bits used for minimizing delay overhead in data correction are to be stored in memory location utilizes in error correction code. A review on memory data error detection and correction code is presented in this paper.**

***Keywords*— Decimal Addition, Error Correction Codes (ECCs), Error Syndrome, Hardware Memory, Multiple Cell Upsets (MCUs).**

I. INTRODUCTION

The factors behind the increasing speed of soft error rate in memory cells, which are fabricated on the down scale of CMOS technology to deep nano-scale and when these cells are exposed to space environment radiations counts for the soft error rate. The data stored in semiconductor memory location is in the form of charge may be affected by the ionizing character of the exposed radiation causes the soft error rate in memory cells. The process of error generation due to radiation that affect the memories which are exposed to the environmental radiations is represented with the help of memory block are shown by fig. 1. In figure it is shown that M0 - M7 is the Memory Data Byte (eg, 10110101) to be send when this memory data is exposed to the Radiation memory data is being affected by the radiation and the send bits gets changed to eg, (10111100). In the process of sending or receiving data to or from the memory location, there may be a single-bit error and in some cases multiple-bit error or multiple cell upset (MCUs) becomes a serious dependability concern about memory reliability. The error correction codes (ECCs) are utilized in order to tolerant the faults in the memory up to the maximum possible extent. A simple block

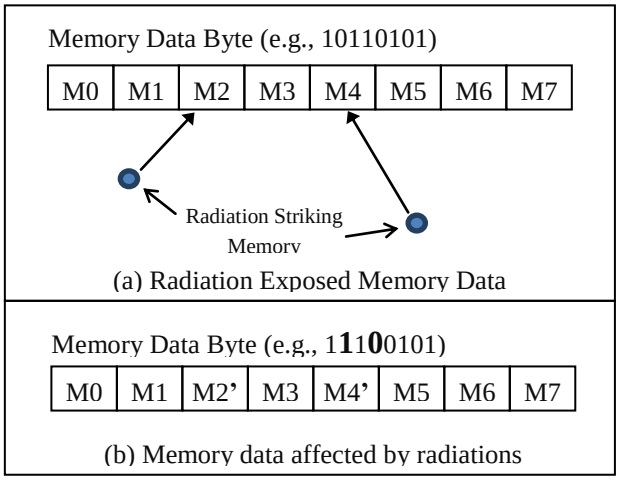

Fig. 1 Soft Error caused in Semiconductor Memory due to exposure to Energy Radiation

Diagram of the fault tolerant memory encoder implementation is shown in fig. 2.

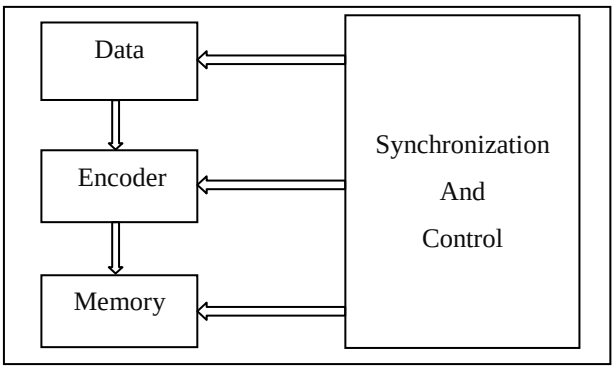

Fig. 2 A simple data encoder block

A block is required to encode the data for error correction code and the data to be stored in the memory and this data is first used to generate redundant bits. To store the redundant bits in the memory location memory interface is required. The redundant bits are used for correcting the errors from the memory locations with the help of decoder. Only some of the most reliable codes include Reed-Solomon (RS) code Bose-Choudhary-Hocquenghem (BCH) code, and Punctured Difference Set (PDS) code. These are the codes that have been used to deal with MCUs in memories. The interleaving technique is utilized to break up the bits into different physical words from the same logical word for rearrangement of the cells in the physical memory to control MCUs. The practical use of Interleaving with content-addressable memory (CAM)

is not possible with the fixed coupling hardware architecture from both comparison circuit structures.

For a single error correction and double error detection technique there are number of researches who proposed many techniques against MCUs like Built-in-Current-Sensors (BICS). For efficiently corrected the MCUs per word 2-D matrix is used for effectively. To protect the bits per rows and per columns, the Hamming code and Parity code are used and the word is divided into multiple columns and multiple rows in the code matrix. Here, the bits per row are protected by Hamming Code and the bits per column are protected by parity code. To detect the two bit error using Hamming code the vertical syndrome bits are used. The 2-D MC is capable of correcting only two errors in all cases and this has lower delay overhead as compared to other codes. A novel decimal matrix code (DMC) is reviewed in this paper. The proposed code is based on divide-symbol to provide improved memory reliability. Decimal integer addition (decimal algorithm) on the divided symbols of binary code is utilizes by the proposed DMC. To detect and correct error bits in the proposed work to find the error syndrome a logic comparator is used by the decoder. To enhance the capability of the code to provide the consistency the decimal algorithm is used. The rest of this paper is arranged as follows: section-II presents the work published by some recent scholars under the title 'Literature Review'. Section III presents the conclusion based on the literature review

II. LITERATURE REVIEW

In reference [1] novel per-word DMC was projected to give surety for reliability of memory. The proposed security code utilized decimal algorithm to detect errors, as a result of that more errors were detected and corrected. The results achieved shows that the proposed scheme has a superior protection level against large MCUs in memory. By the use of proposed decimal error detection technique to detect MCUs in CAM an adequate level of immunity is provided because it can be combined with BICS. In reference [2] presents the relative study of various error correcting codes which defines various alternate to prevail over dependability issue of memories, when exposed to radiation. For higher delay overheads the main problem is that they require complex encoder and decoder architecture to avoid the occurrence of MCUs several error correction codes (ECCs) are used. By comparing with the existing techniques like hamming, matrix codes, built in current sensor etc the proposed system uses decimal matrix code (DMC), to minimize the area and delay overheads, and improvement of the memory consistency is obtain by enhancing the error correction capability.

A decimal correction code is proposed in reference [3] for the execution of error correction technique. To protect memory cells using protection codes in order to preserve a good level of consistency, and various error detection and correction codes are used i.e., Matrix codes (MCs) based on hamming codes have been projected for storage protection. Furthermore, with the help of the encoder-reuse technique (ERT), the area overhead is minimized without interrupting the whole encoding and decoding operations. Reference [4] proposed a system for memories for detection and correction of errors was 64-bit decimal matrix code. More complex error correction codes (ECCs) are widely used to protect memory to pass up MCUs from causing data corruption, however higher delay overhead is the main problem. Recently, hamming codes based matrix codes (MCs) have been proposed for memory protection. In reference [5] the proposed mechanism which derived from hamming code are single error correction-double error detection–triple-adjacent error detection using and single error correction-double error detection –double adjacent error correction Codes resulting From Orthogonal Latin Square Codes will provide single and double adjacent error correction and double non-adjacent and triple error detection. Double adjacent errors are corrected by this combined code.

A novel DMC was proposed to assure the reliability of memory in Reference [6] to detect the errors. Proposed scheme use decimal algorithm for protection code, as a result further errors were detected and corrected. The protection level against large MCUs in memory is better chandelled by the proposed algorithm. Moreover, the proposed decimal error detection technique is an attractive opinion to detect MCUs in CAM because it can be shared with the BICS to provide an adequate level of protection. In Reference [7] two Error Correction Codes are used such as Parity Matrix Code (PMC) and Decimal Matrix Code (DMC). To obtain the maximum error detection capability Decimal algorithm uses DMC utilized. To play down the area overhead of additional circuits without upsetting the whole encoding and decoding processes, the Encoder-Reuse Technique (ERT) is utilized. PMC uses hamming algorithm to detect errors, so that more errors can be detected and corrected. PMC utilizes Encoder-Reuse Technique (ERT) to minimize the area overhead of extra circuits. The number of redundant bits is also less in PMC scheme.

In reference [8] Error Correction Codes (ECCs) are used to supply fault-tolerant memory cells, but the requirement of such codes is more power, area, and higher delay overhead. Thus with less decoding display multiple errors are detected and corrected by Matrix Codes (MCs) which is based on Hamming codes and parity codes. The correction of the error is possible with this matrix code is up to two errors. Decimal Matrix Code (DMC) based on decimal algorithm is used to take full advantage of the potential of error detection and correction. DMC uses reuse technique for encoder for fault tolerant memory protection. The use of this algorithm enables furthermore errors to be detected and corrected by the utilization of large number of redundant bits. To reduce the number of redundant bits framework can be modified by using parity matrix codes in which a 32 bit data is divided into 2bits of 16 blocks. VHDL language is used for Coding. In reference [9] by utilizing decimal algorithm the detection of the errors

or the protection code more errors were detected and corrected. The final results show that the proposed scheme has a better protection level in opposition to large MCUs in memory. Moreover, the proposed decimal error detection technique is an attractive opinion. Here the protection of trustworthiness has achieved by changing Carry Save Adder (CSA). Traditional 2-D repair approach is combined with the proposed technique such that row and column failures and defects on multiple bits are isolated and repaired and defects are handled by the SEC-DED codes. This method would provide a complete approach to protect against soft errors and in memories. Then a method has been proposed that can deal with both types of errors efficiently by applying a modified error correction process. However, for small fault rates and low failure probabilities throughout device operation, the probability of hidden failures will be negligible.

Reference [10] proposed work focuses on the design of HMC for which a hybrid matrix code improved memory consistency against multiple cell upsets. It required less number of redundant bits for security as compared to the accessible approaches. This in turn results with better-quality protection level against large MCUs in memory. In Reference [11] for the detection and correction of the errors proposed scheme introduce decimal algorithm hence, DMC was proposed to assure the reliability of the memory. The projected scheme shows that it has a superior security level against large MCUs in memory and it is accomplished from the obtained results. More redundant bits are required to maintain higher dependability of memory is the only shortcoming, therefore to minimize the number of redundant bits and maximize memory reliability a logical combination of k and m should be chosen based on radiation experiments in actual implementation. In reference [12] proposed a encoder reuse technique with DMC to correct or detect the error due to which the soft error rate in storage cell is quickly increased. To obtain the error detection and correction capability, Decimal Algorithm based Matrix Code (DMC) was proposed technique to use. To minimize the area the Encoder-reuse technique (ERT) based on DMC is used. Primarily, a 2 D matrix is prepared to set up data bits that are split into symbols. To compute Horizontal Redundant Bits (HRB) and Vertical Redundant Bits (VRB), DMC encoder performs the decimal operation. The receiving codeword that is stored in the memory after encoding the radiation affects the memory, Multiple Cell Upset problem will happen. Hence to solve the trouble that can be rectified the Decoder is used. Result outcomes shows that the ECC based DMC yields enhanced performance compared to Hamming Code.

Reference [13] proposed a decimal code matrix which is a preventive technique to protect the memories from the MCUs. For maintaining memory reliability, detection and correction of errors in the memories the proposed method implements the 128 bit Decimal Matrix code. Hence implementing the DMC results in decreases in area, increases the error detection and correction ability, reducing the redundant bits and maintains the memory reliability. Reference [14] to detect errors proposes security code DMC utilized decimal algorithm, to detect and correct more than one error.

In Reference [15] to perform decimal ex-or and addition/subtraction operation to detect and correct errors present in the memory Decimal Matrix Code algorithm is proposed. The power consumption is lower by the use of decimal matrix code than the other existing codes, but the only drawback of DMC is that it requires more number of redundant bits. Reference [16] proposed the code to guarantee the dependability of the memory using HMC (Hybrid Matrix Code).The main disadvantage of proposed HMC is that it utilizes more number of redundant bits to keep the reliability higher. Reference [17] proposes the DMC technique to Enhanced protection and memory detection for multiple MCUs which would be overcome with the help of encoder. Reference [18] proposed an error correction code which provides a competent to the; dependability and security of the memory is improved by using the DMC. The proposed code is quite different from the binary algorithm which performs bit wise logical operation whereas DMC uses decimal algorithm which acquire integer subtraction and addition which is simpler than the previous one.

III. CONCLUSION

A review on DMC based encoder and decoder is presented in this work. The DMC architecture assures dependability of a memory on the hardware design in presence of MCUs. With the help of the encoder circuit the area of DMC circuit can be minimized. As compared to other techniques this reduces the area overhead of extra circuit.

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