TINY I2C (TI2C) PROTOCOL FOR MOBILE DEVICES USING VHDL

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Abstract: Proposed work is a new design of I2C protocol which, which can be consider a Tiny I2C protocol it basically need by the mobile phone for communication of commands between camera or display devices, it is much faster and reliable then UART, SPI and PPI protocol. But as it is not using as main data communication proposed work come up with an idea that to develop a reliable simple and significantly faster protocol for commands communication between processor and camera and display. The whole design is implemented in Xilinx ISE 12.2 simulator targeted to Xilinx Spartan 6 FPGA.

Keywords: MIPI-Mobile Industry Protocol Interface, CSI-Camera Serial Interface, DSI-Display Serial Interface, I2C-Interconnect IC, TI2C-Tiny Interconnect IC

I-INTRODUCTION

I2C is critical in mechanical condition which utilizes multiprocessor for working and in this procedure commotion is probably going to influence the information and because of which control in framework is disgraceful. This proposition displays a novel VLSI usage of I2C intended for quick and mistake free correspondence. CSI-2 is a High Speed Serial Interface between camera sensor and versatile baseband processor as indicated by another Industry Standard that help unidirectional transmission of caught picture from sensor to memory of baseband processor. For controlling the sensor from baseband processor, we need an interface that trade control motions between the two sides. We utilize Tiny I2C (TI2C) convention for the same. Little I2C (TI2C) is a Tiny of I2C convention standard, we can state, it is its impression.

An idea of MIPI is that an if immense measure of information to be exchange it must be unidirectional for rapid ongoing correspondence henceforth in cell phone interfacing with camera and show are constantly unidirectional to keep up continuous circumstances CSI and DSI are MIPI standard for fast unidirectional interfacing. Be that as it may, then again processor likewise needs to discuss controls with these gadgets (I. e. camera and show) for that proposed work has concocted thought to build up a Tiny I2C convention which will be sufficiently quick for send or get controls summons amongst gadget and processor.

The I2C transport is an extremely mainstream and effective transport utilized for correspondence between an ace (different bosses) and a solitary or various slave gadgets. Figure 1.1 delineates what number of various peripherals may share a transport which is associated with a processor through just 2 wires, which is one of the biggest advantages that the I 2C transport can give when contrasted with different interfaces. This application note is gone for helping clients see how the I2C transport functions. Figure 1.1 demonstrates a regular I 2C transport for an installed framework, where various slave gadgets are utilized. The microcontroller speaks to the I2C ace, and controls the IO expanders, different sensors, EEPROM, ADCs/DACs, and significantly more. Which are all controlled with just 2 pins from the master.

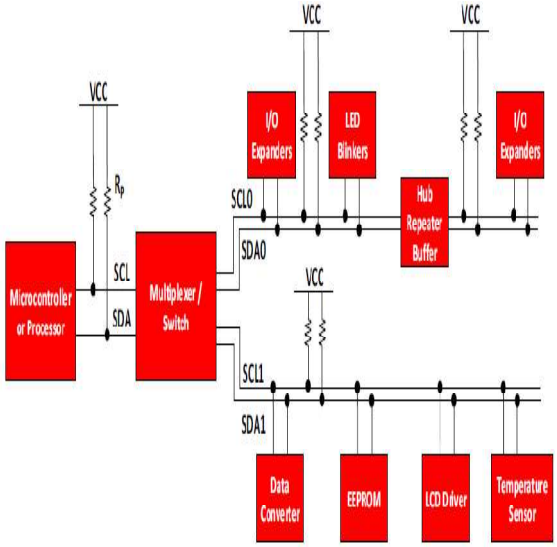

Figure 1: I2C architecture

II- METHODOLOGY

Figure 2 above shows the communication between two high speed devices and a concept of MIPI is that a if huge amount of data to be transfer it must be unidirectional for high speed real time communication hence in mobile phone interfacing

with camera and display are always unidirectional to maintain real time situations CSI and DSI are MIPI standard for high speed unidirectional interfacing. But on the other hand processor also needs to communicate controls with these devices (i. e. camera and display) for that proposed work has come up with idea to develop a Tiny I2C protocol which will be fast enough for send or receive controls commands between device and processor.

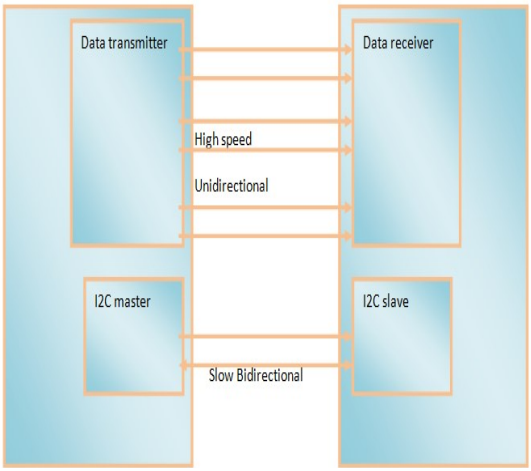

Figure 2: Tiny I2CMaster\Slave

Proposed Tiny I2C (TI2C) is a two-wire, bi-directional, half duplex, serial interface. TI2C is good with the quick mode variation of the I2C interface. TI2C might bolster 400 kHz operation and 7-bit Slave Addressing. TI2C does not bolster the overhead of Multi-ace mode which I2C do.

We can utilize I2C Master as TI2C ace yet Care must be taken with the goal that I2C aces don't attempt to use those I2C highlights that are not upheld by TI2C bosses and TI2C slaves. The Tiny I2Cdefines an extra information convention layer over I2C for The Index address from the Master. Record likewise called sub address is the address of resistor inside the comparing slave. The TI2C bolsters 8-bit file with 8-bit information or 16-bit list with 8-bit information.

HTI2C TOP MODULES: Figure 3 demonstrates the every single inner module of HTI2C RTL additionally indicates design registers modules. We can design them by APB to initiate just those modules which we required to influence it to act as TI2C slave. On the off chance that we are concerning TI2C then we require not required to comprehended working of undesired modules of HTI2C.

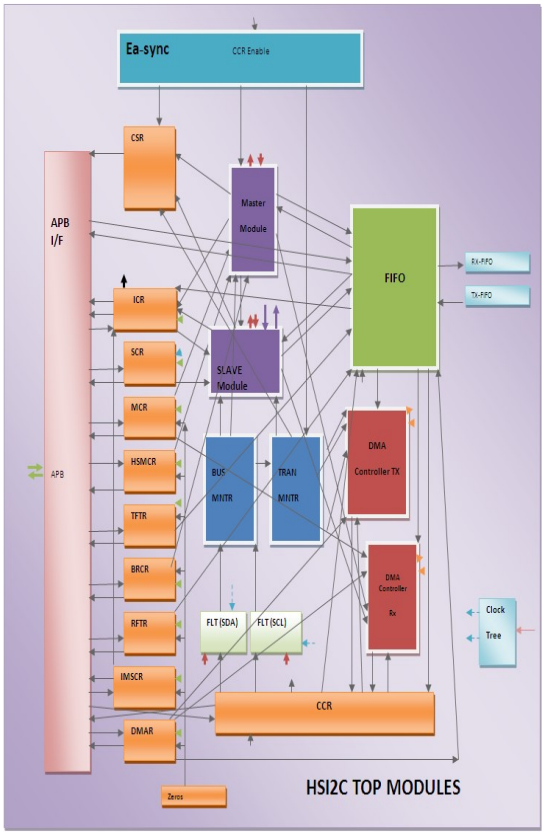

Figure 3: HTI2C Modules

Figure 4 shown below shows only those modules of HTI2C which are required it to work as TI2C slave so we can disable the unwanted modules by configuring the configuration registers. Figure 4.5 also shows TI2C registers interface with slave module of HTI2C RTL.

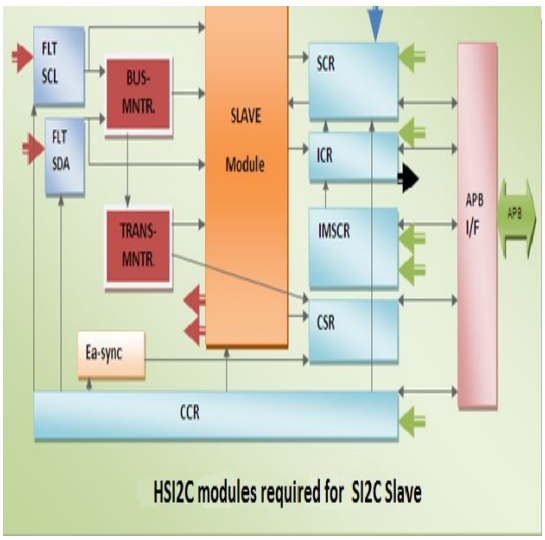

Figure 41: HTI2C Configure as proposed TI2C Slave

III-RESULTS

A dummy master has been developed to verify TI2C salve before actual integrating it with CSI TX. Dummy master can performed as original HTI2C but it has limited functionality. It has a ROM which transmits data sequentially on SDA line during write operation after start condition and it also monitors acknowledgment if positive then ROM address incremented by one send next byte on SDA line.

During read operation it send positive acknowledgement after receiving each byte. Bit [7:1] of first byte of ROM is salve address and bit [0] is set 0 for write operation & 1 for read operation. Dummy master can perform sequential read/write only, random read/write is complicated with dummy master, we can use original HTI2C master for verify all possible test case using TLM.

Verified test case and result below:-

S.N.	Test Case	Result
1.	Verify that a slave device is properly addressed	Pass
2.	Verify that a TI2C Message is properly indexed (16 bit index)	Pass
3.	Verify that a TI2C device can properly handle a sequential read	Pass
4.	Verify that a TI2C device can properly handle a sequential write	Pass
5.	Verify that no read/write when wrong index address	Pass
6.	Verify that a TI2C device can properly handle a sequential read from 16 bit registers.	Pass
7.	Verify that a TI2C device can properly handle a sequential write into 16 bit registers.	Pass
8.	Verify that a TI2C device can properly handle a sequential AHB read	Pass
9.	Verify that a TI2C device can properly handle a sequential AHB write	Pass

Table 1: Verification through dummy Master

Verification through TLM environment: Before verification using TLM, it is required to integrate TI2C register's top RTL module with Emulator top RTL module. This is done in order to form overall CSI TX RTL top module.

CSI_TX overall RTL top = Emulator top RTL+ TI2C top RTL;

TLM is a methodology in which the details of communication among computation components are separated from the details of the implementation of computation components.

Actually TLM are the software written in C or other high level language which can run along with RTL developed in any HDL for generating Top level RTL interface. In other words TLM is a generalized test case written in high level language for generating different test. TLM makes verification simple allows simulating in every aspect. We have developed TLM for overall CSI TX RTL top. Using TLM can force any value for testing and verification. Test cases and observation shown below:

Purpose: To verify that a slave device is properly addressed

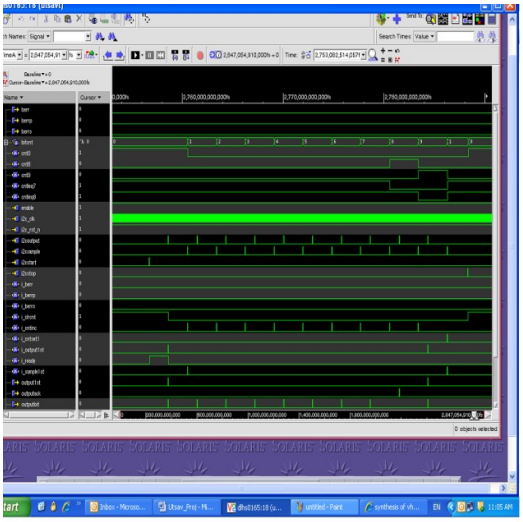

Figure 5: simulation to observe slave device address

Verify that the Master used 7 bits to define the Slave address. Verify that the Slave properly used the received 7 bit Slave address.

Purpose: To verify that a TI2C Message is properly indexed (16 bit index)

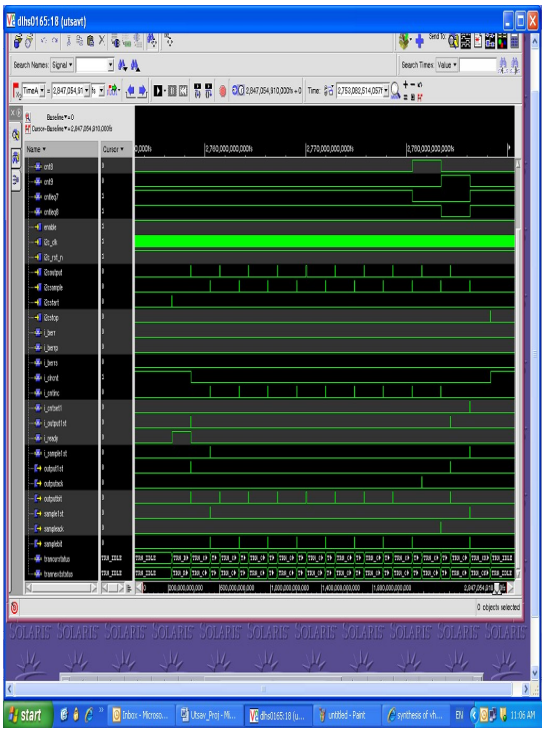

Figure 6: simulation to observe TI2C Message

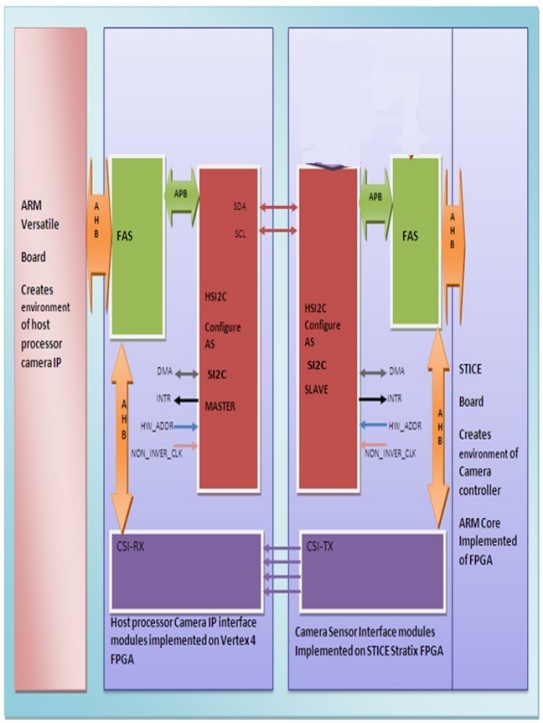

Figure 82: Hardware setup for validation of TI2C

Verify that the Slave properly decodes both index MSB & LSB.

Purpose: To verify that a TI2C device can handle a sequential read from the current location.

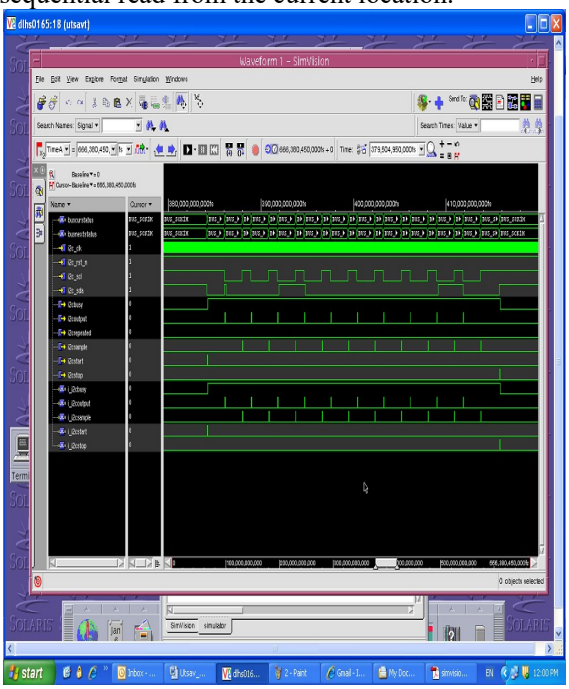

Figure 7: simulation to observe TI2C device sequential read

1	Selected Device	3s500epq208-5
2	Number of Slices	160 out of 4656 3%
3	Number of Slice Flip Flops	133 out of 9312 1%
4	Number of 4 input LUTs	299 out of 9312 3%
5	Number of IOs	93
6	Number of bonded IOBs	90 out of 158 56%
7	Number of GCLKs	1 out of 24 4%

Table2. Device Utilization summary

COMPARATIVE RESULTS

Author	Outcome
Bharath.K.B et al [1]	Power consumption 82mW, 7.80 ns time delay and 173 slices with SPARTAN-3, for implementation of I2C module.
Shah Rahil Pareshbhai et al [2]	Total 179 slice of Spartan FPGA and maximum time delay is 8.216 ns for implementation of I2C module.

Proposed work	Total 160 Slices of Spartan FPGA with 6.397ns time delay and Maximum Frequency: 156.333MHz, power consumption observe is 11.35 mW

Table 3 Comparative Results

From table 3 shows comparative results can be analyzed and it can be observe that proposed work require less time for TI2C data communication and hence faster as compare to other work. Also the number of slices for the proposed work is also less means the area requirement of proposed work is also less.

IV-CONCLUSION

This thesis presents a novel VLSI implementation of I2C designed for fast and error free communication. CSI-2 is a High Speed Serial Interface between camera sensor and mobile baseband processor according to a new Industry Standard that support unidirectional transmission of captured image from sensor to memory of baseband processor. Multiple literature papers studied for the completion this work and after its deep study the whole idea of developing Tiny-I2C is come up with an idea as explained in thesis. We have tried to implement our module as per our presented design. Form comparative results it may be monitor that presented work necessary less number of slices of Spartan FPGA as compare to available works.

Proposed work requires less time for TI2C data communication and hence faster as compare to other work. Also the number of slices for the proposed work is also less means the area requirement of proposed work is also less. It can be conclude that thesis designed TI2C module is very much area optimized & it has higher speed of computation with all sort of operations which TI2C may perform.

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