Review on Input Vector Monitoring concurrent BIST Architecture Design for a Multiplier

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***Abstract*— The problem arises at the time of testing in VLSI circuits and systems can be handled with the help of Built-In Self-Test (BIST) technique that constitute an attractive and practical solution. Input vector monitoring coexisting BIST schemes perform testing concurrently with the operation of the circuit. This paper presents a novel input vector monitoring concurrent BIST scheme that compares auspiciously to previously proposed schemes with respect to the required hardware overhead.**

***Keywords*— Error Detection, Input Vector Monitoring, Off-Line Testing, On-Line Testing, Pre-Computed Test Set, Self-Testing.**

I. INTRODUCTION

Built-in self test (BIST) is a technique that constitutes a class of schemes that give the capability of performing high fault coverage at-speed testing, whereas simultaneously they rest the dependence on expensive external testing equipment. Consequently, they represent an attractive solution to the problem of testing VLSI devices. BIST techniques are typically classified into online and offline. There were two modes normal and test, the architectures operate in either normal mode (during which the BIST circuitry is idle) or test mode is Offline architecture.

The inputs generated by a test generator module are applied to the inputs of the circuit under test (CUT) and the responses are captured into a response verifier (RV) for the entire duration. Hence, to perform the test, the standard operation of the CUT is slowed down and, consequently, degraded performance of the system in which the circuit is included obtain. To figure out that a technique is proposed to avoid such conditions is Key vector monitoring simultaneous with BIST. These architectures test the CUT at the same time with its normal operation by exploiting input vectors appearing to the inputs of the CUT; here is the condition, if the incoming vector belongs to a set called active test set, the RV is enabled to capture the CUT response The CUT has a inputs and b outputs and is tested comprehensively; hence, the test set size is N = 2a. The technique can operate in either normal or test mode, depending on the value of the signal labeled *T/N.* Normal input vector is the driver that that drives the inputs of the circuit which is to be tested this is to be done at the time of normal mode. A is a input which is driven to the concurrent BIST unit (CBU), this input

A is compared with active test set. When there is any similarity between A and any one of the vectors in active test set, we say that hit has occurred. Shown by fig.1 this is the condition in which A will be removed from the active test set after that the signal response verifier enable is given to enable the m-stage of the RV to capture the CUT response. The condition occurs when all the input vectors have performed hit, then the contents of RV are examined.

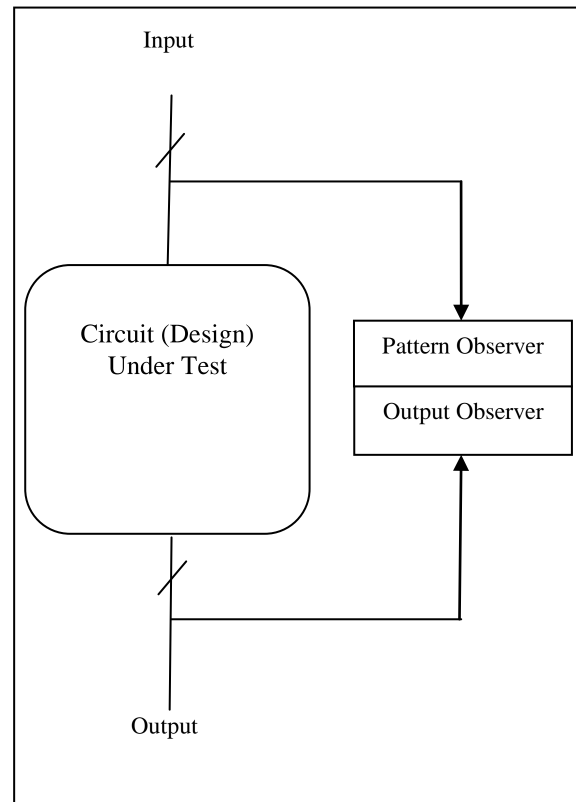

Fig1. Online testing block

CBUs output denoted by TG [n:1] is the driver of the inputs of the CUT during the test mode. The concurrent test latency (CTL) of input vector monitoring is the mean time (counted either in numbers of clock cycles or units of time) required to complete test performance while the circuit performance in normal mode. Test Pattern Generator (TPG) is a method utilize by the BIST to generate the required test patterns which are applied to the number of inputs of the Circuit Under Test (CUT). In brief, an input vector monitoring concurrent BIST is proposed, which will compares favourably to the previously proposed schemes in order to the hardware overhead/CTL trade off. The block diagram of an input vector monitoring concurrent BIST architecture is shown in Fig.2

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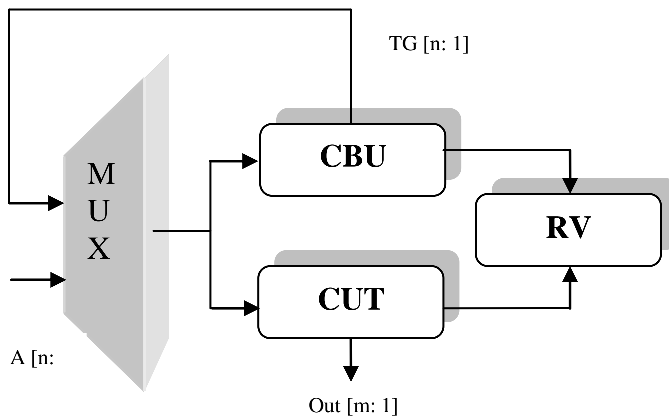

Fig2. Input vector monitoring concurrent BIST architecture

II. Literature review

In reference [1] a novel input vector monitoring concurrent BIST architecture is presented which is based on the use of a SRAM-cell like structure for storing the information, whether an input vector has appeared or not during normal operation. The proposed scheme is shown to be more efficient in terms of hardware overhead and CTL (concurrent test latency). In reference [2] the work is performed for avoiding performance degradation of a system by proposing a novel input vector monitoring concurrent BIST technique for combinational circuits termed R-CBIST. This work compares to the other techniques proposed earlier with respect to the Hardware Overhead/Concurrent Test Latency tradeoffs. The paper also addressed the issue concerning to the testing of RAM utilization. For ROM testing, R-CBIST was demonstrated that shows a typical requirement of ROM sizes for the exits R-CBIST configuration within certain hardware overhead such that the concurrent test completes within specific time limits. Furthermore, this paper shows that, for the case of the ROM BIOS, a circuit implemented in most current personal computers, the application of R-CBIST results in suitable hardware overhead, with concurrent test latency on the order of a few seconds.

Reference [3] proposed a RAO-DDR technique for faults detection at the duration of system operation. This technique not only locate the fault but also capable to correct the faults and for this no additional hardware is required because reprogrammable logic is used for the test architecture. This paper also shows the practical approach by applying this scheme to the controllers of OC8015 and compared with the concurrent online fault detection methods. Reference [4] proposed a window monitoring concurrent BIST and input vector monitoring concurrent BIST using SRAM cells. This paper shows compassion with respect to delay and area between online build- in- self test using SRAM cells and window monitoring concurrent BIST. A result obtain from this compression shows that online –build- in self-test will reduce more delay when compared to offline BIST. Here, compaction method is used to reduce the delay, area and hardware requirements based on Accumulator. Reference [5] proposed a technique using window monitoring concurrent BIST and input vector monitoring concurrent BIST using modified SRAM cells. The proposed method gives an attractive solution for the problem of testing VLSI devices. The proposed scheme performs the testing during the circuit normal operation on both offline and online system. Therefore the method can prevent problems appearing in offline BIST technique. This is applicable for both normal and test mode. In normal mode the outputs from the CUT and logic block are verified using response verifier RV. At the time of test mode the values are generated and the output is verified based on that values.

Reference [6] presents an inventory model incorporating some of the realistic features like deterioration, displayed stock dependent demand and two storage facilities. In this paper proposed model can be extended by incorporating shortages, discount and inflation rates. In addition demand can be considered as a function of price, quality as well as time varying. Reference [7] present a novel input vector monitoring concurrent BIST scheme, which is based on the idea of monitoring a set (called window) of vectors reaching the circuit inputs during normal operation, and the use of a static-RAM like structure to store the relative locations of the vectors that reach the circuit inputs in the examined window; the proposed scheme is shown to perform significantly better than previously proposed schemes with respect to the hardware overhead and CTL tradeoff. Reference [8] presents a Modified BIST based on the utilization of SRAM cell like structure which stores the information about whether an input vector appears or not in normal operation. BIST schemes provide an attractive solution for the problem which arrives during testing VLSI devices. The presented scheme is more significant than the traditional input vector monitoring BIST schemes in terms of hardware overhead and CTL.

Reference [9] proposed method is three weight pattern generation pseudorandom built-in-self-tests (BIST) method to achieve complete fault coverage in BIST applications by reducing number of vectors. Weighted sets are 0, 0.5, and 1 have been used generate test pattern generation and achieve low testing time less power consumption, The proposed scheme is simulated and synthesized using Xilinx 12.1 software. The proposed method introduces a key vector monitoring simultaneous BIST scheme that is used to avoid problems in online and offline BIST schemes. In this paper proposed scheme use SRAM–cell to store the information. Reference [10] proposed technique, a novel input vector monitoring concurrent BIST architecture has been presented, based on the use of CAM-cell like structure for storing the information of whether an input vector has appeared or not during normal operation. The proposed scheme is shown to be more efficient than previously proposed input vector monitoring concurrent BIST techniques in terms of hardware overhead and CTL.

Reference [11] proposed input vector monitoring concurrent BIST architecture has been presented, based on the usage of a SRAM-cell like structure for storing the information data, whether an input vector has appeared or not during normal operation. This paper mainly introduced new methods to implement and use of saboteurs and mutants into

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VHDL models. The new models of saboteurs prevent some of the problems that the previously had. These problems prevented the automatic insertion. Moreover, the new models have been implemented in a way that they diminish the hardware overhead, by reducing the number of signals that is required to manage bidirectional saboteurs. Another enhancement is respect to prior models that they allow injecting of more fault models. The advantages of the new proposal is to implement mutants are especially relevant. These saboteurs and mutants have been applied to example circuits at gate level and register level. Reference [12] a novel input vector monitoring concurrent BIST architecture has been presented, based on the use of a SRAM-cell like structure for storing the information of whether an input vector has appeared or not during normal operation. The proposed scheme is shown to be more efficient than previously proposed input vector monitoring concurrent BIST techniques in terms of CTL and hardware.

Reference [13] proposed a novel input vector monitoring concurrent BIST architecture based on the use of a SRAM-cell like structure for storing the information of whether an input vector has appeared or not during normal operation. The proposed scheme shows to be more efficient than previously proposed input vector monitoring concurrent BIST techniques in terms of hardware. Reference [14] presents a novel input vector monitoring concurrent BIST scheme, which is based on the idea of monitoring a set (called window) of vectors reaching the circuit inputs during normal operation, and the use of a static RAM like structure to store the relative locations of the vectors that reach the circuit inputs in the examined window; the proposed scheme is shown to perform significantly better than previously proposed schemes with respect to the hardware overhead and CTL tradeoff. As an extension, in the CUT we are using data multiplier (8*8).we are using Xilinx version to verify the output. The performance analysis of the dada multiplier is verified using BIST.

Reference [15] proposed a method in which a weighted Pseudo-random built-in-self-test (BIST) scheme utilized in order to drive down the number of vectors to achieve complete fault coverage in BIST applications. Weighted sets comprising three weights, namely 0, 0.5 and 1 have been successfully utilized so far for test pattern generation, since they result in both low testing time and low consumed power. Reference [16] proposed a method for fault monitoring using input vector concurrent BIST based on SRAM-cell used to store information at normal operation. Input vector monitoring concurrent BIST scheme thus overcomes problem appearing separately in online and in offline BIST schemes appearing separately in online and in offline BIST schemes .The proposed method is a weighted Pseudo-random built-in-self-test (BIST) scheme utilized in order to drive down the number of vectors to achieve complete fault coverage in BIST applications.

Reference [17] proposed a new novel input monitoring BIST scheme for VLSI circuit testing. BIST has an advantage over cost and memory storage reduction and it can test many units in parallel without disturbing the normal operation. In the proposed method functionality reduction method is used to reduce the area, power than the previous methods. Here the logic module was modified with the component reduction and also another change in application. The memory is replaced with the new processor design. A Roving STAR algorithm is used for testing. With these modifications, the functions of testing circuit have been improved using novel input vector monitoring BIST. Area overhead, concurrent test latency and power consumption are reduced and speed has also been improved. In Reference [18] concurrent BIST architecture for online testing has been presented, based on the use of a SRAM-cell like structure for storing the information of whether an input vector has appeared or not during normal operation. The proposed scheme is shown to be more efficient than previously proposed input vector monitoring concurrent BIST techniques.

Reference [19] proposed a a novel input vector monitoring concurrent BIST architecture based on the use of a SRAM-cell like structure for storing the information. This paper presents BISD and BISR scheme to perform the fail pattern identification and repairing of the fail pattern in the test cubes. Thus this method is shown to be more efficient than the previously proposed method because it not only detect the error in the circuit, however additionally repair and correct the error in the test pattern. Reference [20] presents a modification i.e. Multiple Hardware Sig nature Analysis Technique (MHSAT), Order Independent Signature Analysis Technique (OISAT), RAM-based Concurrent BIST (R-CBIST), Window-Monitoring Concurrent BIST (w-MCBIST), and Square Windows Monitoring Concurrent BIST (SWIM). This architecture has been presented, based on the use of a SRAM-cell like structure for storing the information of whether an input vector has appeared or not during normal operation. The proposed scheme is shown to be more efficient than previously proposed input vector monitoring concurrent BIST techniques in terms of hardware overhead and CTL.

III. Conclusions

Problem occurrence for testing of VLSI devices can be handle with the BIST schemes that gives an attractive solution. Input vector monitoring simultaneously perform BIST schemes for testing during the circuit normal operation without imposing a need to set the circuit offline to perform the test, therefore they can avoid problems appearing in offline BIST techniques. The assessment criteria for the class of testing schemes are the hardware overhead and the CTL, i.e., the time required for the test to complete, when the circuit operates in its normal mode. This paper presents a review of number of scholar’s research paper which presents number of solutions for the problem arises at the time of VLSI testing.

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