Analyzation & Implementation of Full Subtractor Circuits Designs Using Modified Gate Diffusion Technique

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Abstarct: This paper mainly focused on designing Full Subtractor by a new technique called MGDI technology. Here two basic design of full subtractor has been designed using MGDI technique. The software used to design schematic circuit is DSCH tool and for layout generation Microwind has been used.

Keywords: - Full Subtractor, half subtractor, CMOS, Modified gate diffusion technique MGDI, gate diffusion technique GDI.

I. INTRODUCTION

Digital signal processing, image & video processing are the example of some of VLSI applications, widely use arithmetic operations. Subtractor, division, addition, multiply and accumulate MAC are mostly used arithmetic functions. The 1-bit full-subtractor cell is the building block of all these modules. Thus, enhancing its performance is critical for enhancing the overall module performance. The design criterion of a full subtractor cell is usually multi-fold. Transistor count is, of course, a primary concern which largely affects the design complexity of larger circuit. For such submicron CMOS technology area, topology selection, power dissipation and speed are very important aspect for high speed and low power application. These issues can be overcome by incorporating Gated Diffusion Input (GDI) technique. Several optimization techniques for full subtractor design are reported in the literature [1-10]. Among Gate Diffusion Input (GDI) is a lowest power design technique which offers improved logic swing and less static power dissipation. Using this technique several logic functions can be implemented using less number of transistor counts. This method is suitable for design of fast, low-power circuits, using a reduced number of transistors (as compared to TG and CMOS).

The rapid growth in market of electronic devices had boomed the IC engineers. Meanwhile, as the daily used portable IC devices, such as, mobile phones, laptop etc., VLSI engineers are working to improve the performance of existing operation modules in some aspects, especially in reducing the power consumption and size. [1]- [4] Low power for devices can be achieved by selecting new technology or implementing a new logic. Technology means scaling down the size of transistor, which further help in reducing the area and power. Second term is logic, which implies reducing power and area by changing the logic while keeping the transistor size constant.

This paper is organized as follows: some basic of MGDI technique are presented as essential fundamentals in Section II. Section III contains two logic equations relevant to 1-bit full subtractor and full subtraction logic based on logic gates and half subtractor is presented. Section IV includes design of sub-modules, which helps in designing of the subtractor circuit. Section V includes result analysis of all the two designs and calculation of delay and power analysis. After all design and analysis, circuit with least delay and power was selected and layout was designed for the same using Microwind software.

II. MGDI TECHNIQUE

The basic primitive of GDI cell consists of NMOS and PMOS containing four terminals G is common gate input of NMOS and PMOS transistors, P is the outer diffusion node of PMOS transistor, N is the outer diffusion node of MOS transistor, and D is common diffusion node of both transistors. In this work a modified primitive GDI logic gates have been implemented in 65nm technology and it is compared with existing GDI and CMOS logic. Fig 1 shows the construction of modified GDI basic gates of AND, OR, NOR, NAND, XOR, XNOR and MUX.

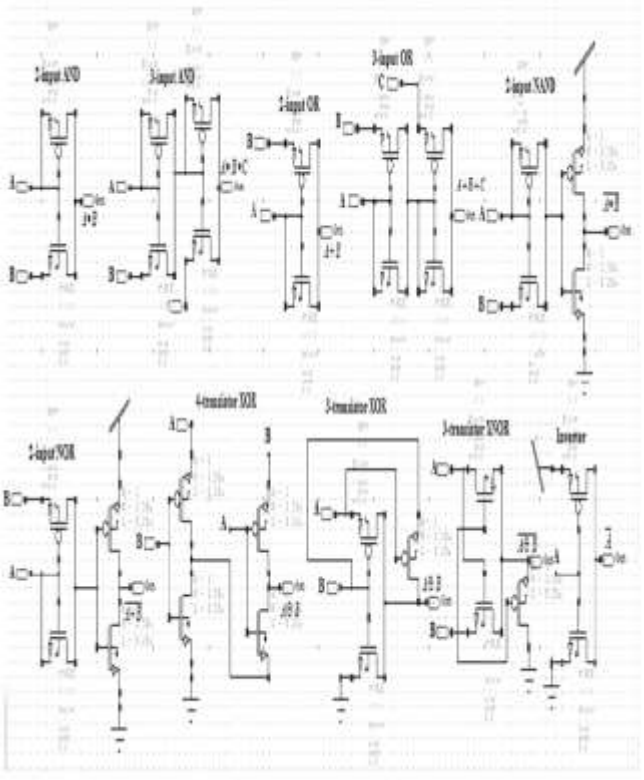


Fig.1 Basic gates design by MGDI technique

subtractor is a combinational circuit that based on the subtractor design by logic gates made by CMOS, performs a subtraction between two binary bits and one of

$$Diff = A - B - Cin \quad (1)$$

$$Bout = 1\_if\_A < (B + Cin) \quad (2)$$

$$Diff = A \oplus B \oplus Bin \quad (3)$$

$$Bout = Bin.\overline{(A \oplus B)} + \overline{A}.B \quad (4)$$

Full subtractor using half subtractor:- By using two half subtractors a full subtractor can also be design. This method is very easy and convenient for designing a full subtractor. As we know half subtractor can easily be design by one XOR, one inverter and by one AND gate.

The operation of OR gate is described here. For OR gate, the source of pMOS is connected with input "B" and the source of nMOS is connected with input "A". The gate terminal G is connected with "A". When both the inputs are at low level then pMOS will operates in linear whereas nMOS is cut-off. When A is at high and B is at low level then pMOS is in linear region and nMOS is in linear region thereby producing the output as 1. Similarly for A at low level and B is at high level then pMOS is in linear and nMOS is also in linear region again producing the output as 1 Similarly when A and B both are at high level , then pMOS and nMOS are again in linear region thereby producing the output as 1.

III. DESIGNS OF FULL SUBTRACTOR

Conventional design of full subtractor:- The conventional design for full subtractor is shown as figure 4.1 and the equations are present in equation 1-4. The conventional one-bit full

the signals may be borrowed by a lower significant bit. This circuit has three inputs and two outputs. Here we considering the three inputs are A, B and Bin and the output are Diff for difference and Bout for borrow output. [14]

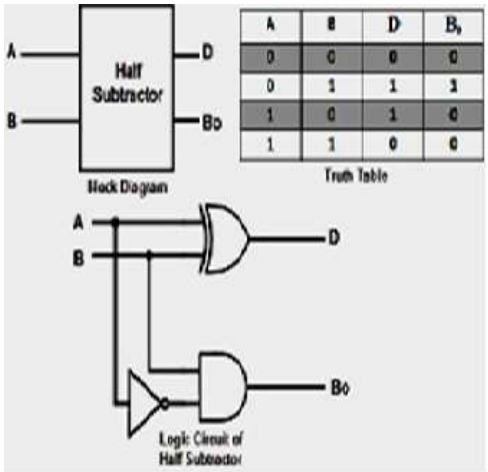


Figure 2 Block diagram, circuit diagram & truth table of Half Subtractor

So by using two half subtractors and one OR gate full subtractor circuit can be design or can be easily obtained by the designers.

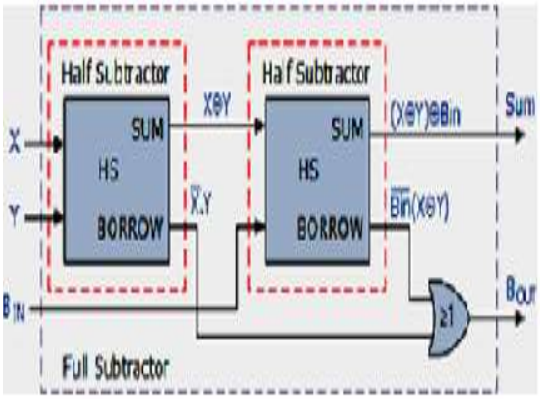
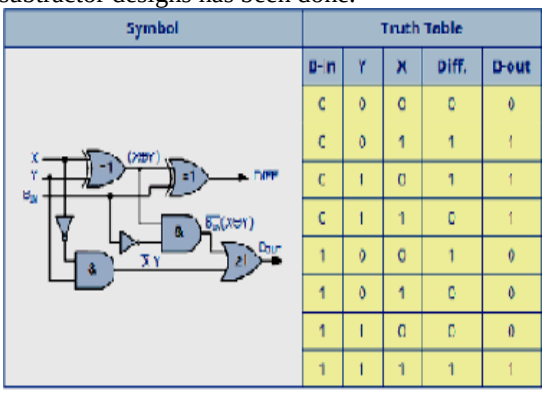


Figure 3 Block diagram of Full Subtractor using HS

IV. DESIGN SCHEMATIC OF MODULES

All the basic gates AND, OR, XOR, INVERTOR are first design in DSCH tool after that conventional full subtractor designs has been done.



Symbol	Truth Table				
	B-in	Y	X	Diff.	B-out
	0	0	0	0	0
	0	0	1	1	1
	0	1	0	1	1
	0	1	1	0	1
	1	0	0	1	0
	1	0	1	0	0
	1	1	0	0	0
	1	1	1	1	1

Figure 4 Schematic of Full Subtractor and truth table

And from these logic gates half subtractor is designed and by use of that full subtractor is implemented.

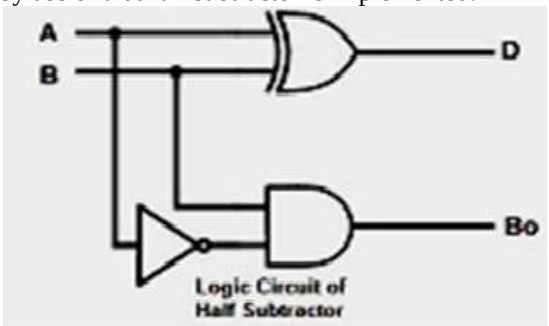


Figure 5 DSCH Schematic of Half Subtractor for MGDI Technique

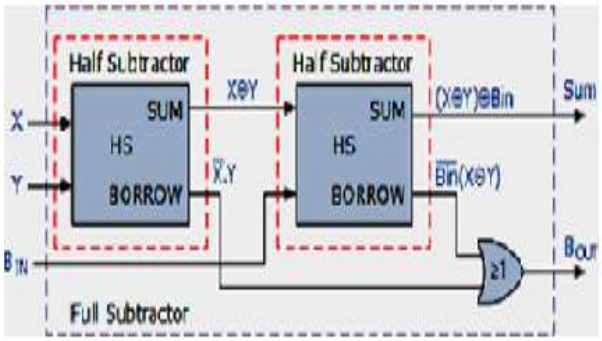


Figure 6 DSCH Schematic of full subtractor by half subtractor using MGDI technique

V. LAYOUT AND RESULT

Following layouts are generated by Microwind software full subtractor designs by conventional method and half subtractor.

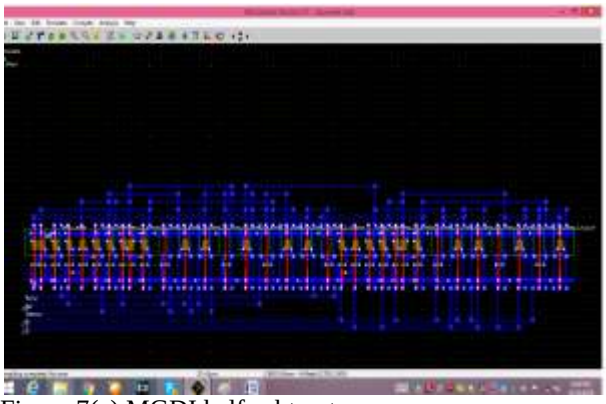
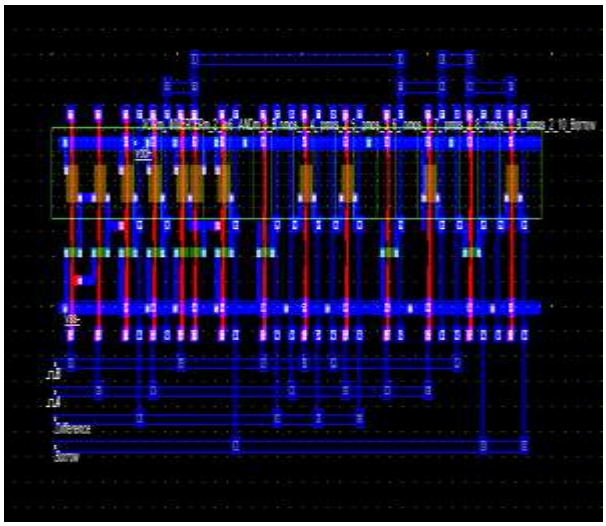


Figure 7(a) MGDI half subtractor



7(b) MGDI Full Subtractor using HS

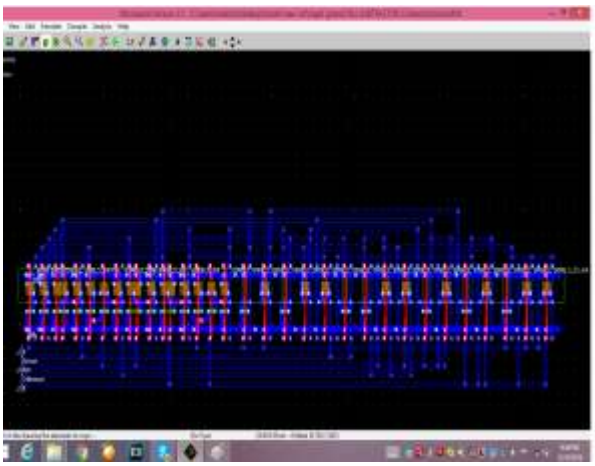


Figure 8 MGDI conventional Full Subtractor

S.NO.	PARAMETERS	CMOS TECH.	MGDI TECH.
1	SWITCHING DELAY (ns)	0.11	0.055
2	VERILOG FILE SIZE (Lines)	79	43
3	NO. OF SYMBOLS USED	62	28
4	COMPILED CELLS	57	23
5	ROUTED WIRES	109	56
6	NO. OF NMOS TRANS. USED	26	7
7	NO. OF PMOS TRANS. USED	26	9
8	ELECTRICAL NODES COMPILED	47	32
9	AREA (μm^2)	625.9	234.7
10	TRANSISTORS USED	52	16

VI. RESULTS

By these parameter study it is clear that modified gate diffusion technique has batter performance over CMOS technique

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S.NO.	PARAMETERS	CMOS TECH.	MGDI TECH.
1	SWITCHING DELAY (ns)	0.055	0.04
2	VERILOG FILE SIZE (Lines)	43	28
3	NO. OF SYMBOLS USED	29	14
4	COMPILED CELLS	25	10
5	ROUTED WIRES	49	25
6	NO. OF NMOS TRANS. USED	10	3
7	NO. OF PMOS TRANS. USED	10	4
8	ELECTRICAL NODES COMPILED	22	15
9	AREA (μm^2)	205.6	77.3
10	TRANSISTORS USED	20	7

VII. ACKNOWLEDGMENT

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VIII. CONCLUSION

The current work proposes the design of a full subtractor using Modified Gate Diffusion Input (MGDI) procedure which on simulation has been found to consume low power in conjunction with lesser delay time and fewer transistors while maintaining proper output-voltage swing. In order to establish the technology independence the present work has been performed in 65nm technology using DSCH and the layout has been concocted in Microwind.

In switching delay, power dissipation and transistor count. The significant difference is shown in XOR gate performance because transistor count is much lesser than basic Cmos technique.

References

[1] Laxmi Kumre, Ajay Somkuwar, Ganga Agnihotri "*Implementation of radix 4 booth multiplier using MGDI technique*", 2013

[2] Massoud Pedram, "*Design Technologies for Low Power VLSI",* to spearing Encyclopaedia of Computer Science and Technology, 1995.

[3] Anantha P Chadrakasan and Robert W Brodersen, "*Minimizing Power Consumption in CMOS Circuits*", Proceedings of IEEE, Vol.83, No.4,April 1995.

[4] I.S. Abu I.S.Abu-Khater, A. Bellaouar, and M. I. Elmastry, "*Circuit techniques for CMOS low-power high-performance multipliers," IEEEJ. Solid-State Circuits*, vol. 31, pp. 1535–1546, Oct. 1996.

[5] Book by Dimitris Soudris, Christian Piguet and Costas Goutis,"*Designing CMOS circuits for Low Power*", May 2002

[6] Arkadiy Morgenshtein, Alexander Fish, and Israel A. Wagner, *"Gate-Diffusion Input (GDI)-A Power-Efficient method for digital combinatorial circuits* "IEEE Transactions on VLSI systems, vol.. 10,No. 5, October 2002

