Design and implementation of high speed and area efficient hybrid subtractor using M.G.D.I Technique

1Ankita Jain, 2Utsav Malviya
1Research Scholar, 2Associate Professor
Department of Electronics and Communication Engineering
GGITS Jabalpur, MP

Abstract: Subtractors form one of the important components of every contemporary integrated circuit. The basic requirement of the subtractor is that it should be fast and efficient in terms of power consumption and chip area. Optimization of several devices for speed and power is a significant issue in low-voltage and low-power applications. These issues can be resolved by incorporating Modified Gated Diffusion Input (MGDI) technique. The current work proposes the design of a full subtractor using Modified Gate Diffusion Input (MGDI) procedure which is proposed to consume low power in conjunction with lesser delay time and fewer transistors while maintaining proper output-voltage swing. Here four design of full subtractor has been designed using MGDI technique. All these design are based on 65nm CMOS foundry. The software used to design schematic circuit is DSCH tool and for layout generation Microwind has been used.

Keywords: - Full Subtractor, half subtractor, CMOS, Modified gate diffusion technique MGDI, gate diffusion technique GDI

I-INTRODUCTION

A subtractor is one of the significant building blocks in the construction of a binary divider [1], [2]. In recent times, applications are aimed at battery operated devices so that power dissipation becomes one of the primary design constraints [3]–[10].

In the past processor speed, circuit speed, area, performance, cost and reliability were of prime importance. Power consumption was of secondary concern. However, in recent years power consumption is being given equal importance. The reason for such a changing trend is attributed probably due to the rapid increase in portable computing devices and wireless communication systems which demand high speed computations and complex functionality with low power consumption. In addition to this high performance processors consume severe power which in turn increases the cost associated with packaging and cooling. Subsequently there is a rise in the power density of VLSI chips thereby disturbing the reliability. It has been found that every 10o rise in operating temperature roughly doubles the failure rate of components made up of Silicon due to several Silicon failure mechanisms such as thermal runaway, junction diffusion, electro migration diffusion, electrical parameter shift; package related failure and Silicon interconnect failure [11]. From the environment point of view, the lesser the power dissipation of electronic components, lesser will be the heat dissipated in rooms which in turn will have a positive impact on the global environment. Also, lesser electricity will be consumed.

Therefore, for further optimization of performance of a full subtractor in terms of switching delay, area, transistor count, a new low power, high speed energy efficient

full subtractor is being proposed using Modified Gate Diffusion Input (MGDI) technique.

Modified gate diffusion input MGDI:- The basic primitive of GDI cell consists of NMOS and PMOS containing four terminals G is common gate input of NMOS and PMOS transistors, P is the outer diffusion node of PMOS transistor, N is the outer diffusion node of MOS transistor, and D is common diffusion node of both transistors. In this work a modified primitive GDI logic gates have been implemented in 65nm technology and it is compared with existing GDI and CMOS logic. Fig 1 shows the construction of modified GDI basic gates of AND, OR, NOR, NAND, XOR, XNOR and MUX.

© 2016 IJAIR. All Rights Reserved

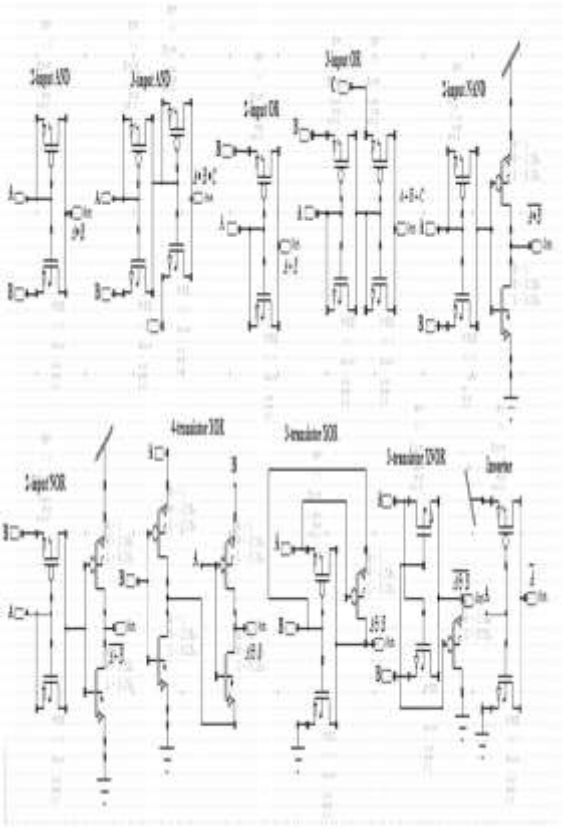


Figure 1 basic gates implementation by MGDI

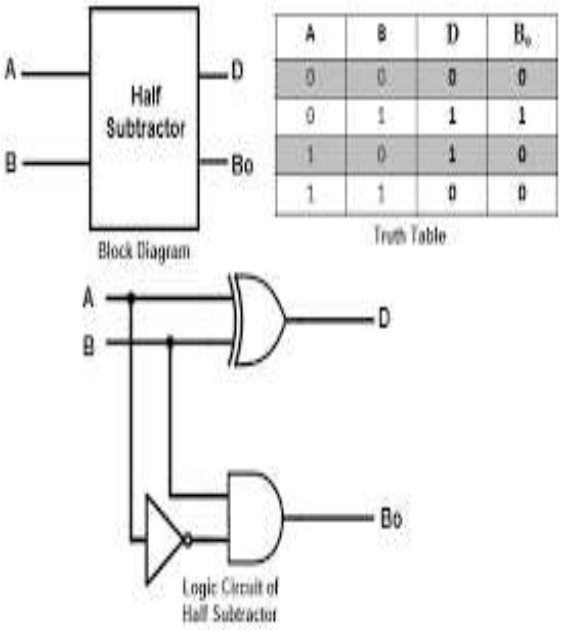
Different subtractor designs: Conventional design of full subtractor:- The conventional design for full subtractor is shown as figure 4 and the equations are present in equation 1-4. The conventional one-bit full subtractor is a combinational circuit that based on the subtractor design by logic gates made by CMOS, performs a subtraction between two binary bits and one of the signals may be borrowed by a lower significant bit. This circuit has three inputs and two outputs. Here we considering the three inputs are A, B and Bin and the output are Diff for difference and Bout for borrow output. [14]

$$Diff = A - B - Cin \quad (1)$$

$$Bout = 1\_if\_A < (B + Cin) \quad (2)$$

$$Diff = A \oplus B \oplus Bin \quad (3)$$

$$Bout = Bin.\overline{(A \oplus B)} + \overline{A}.B \quad (4)$$



A	B	D	B_o
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Truth Table

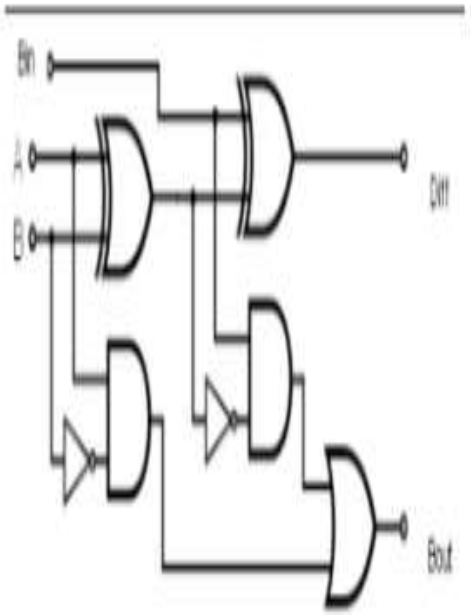


Figure2 Block diagram, circuit diagram & truth table of Half Subtractor

© 2016 IJAIR. All Rights Reserved

Full subtractor using half subtractor:- By using two half subtractors a full subtractor can also be design. This method is very easy and convenient for designing a full subtractor. As we know half subtractor can easily be design by one XOR, one inverter and by one AND gate.

So by using two half subtractors and one OR gate full subtractor circuit can be design or can be easily obtained by the designers.

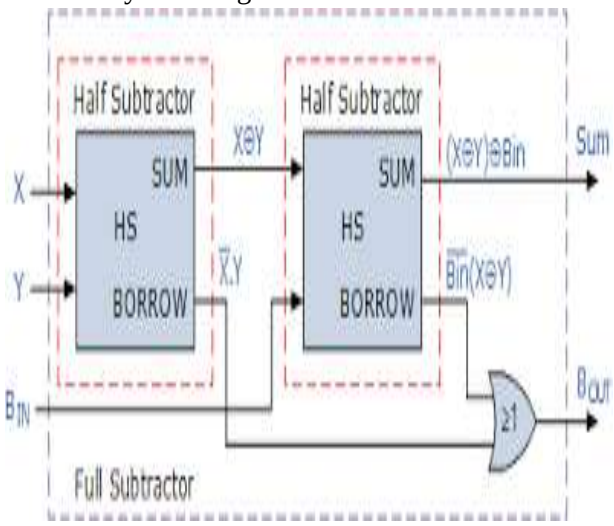
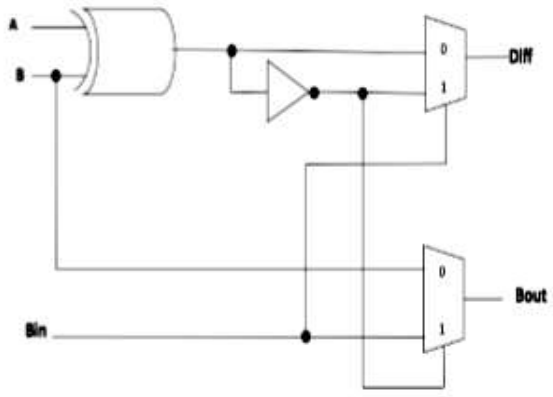


Figure 3 block diagram of full subtractor using half subtractor



Layouts & result analysis

Following layouts are generated by Microwind software full subtractor designs by conventional method and half subtractor.

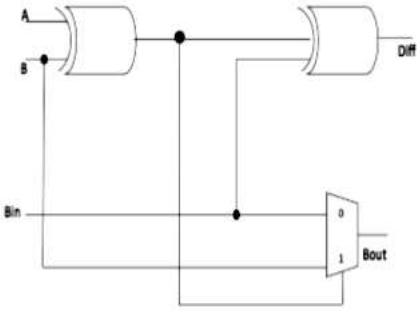


Figure 4: diagram of Conventional Full Subtractor

XOR BASED SUBTRACTOR IMPLEMENTATION: Based on conventional design, new design for full subtractor was designed using XOR or XNOR gate. Figure 4.1, 4.2 display the XOR based design, which is derived from equation 3 and 4 and it include XOR gate and multiplexer. Firstly XOR gate was designed, which include four transistors instead of 16 transistors as observed in CMOS technology. Figure display the XOR gate design using GDI technique.

.

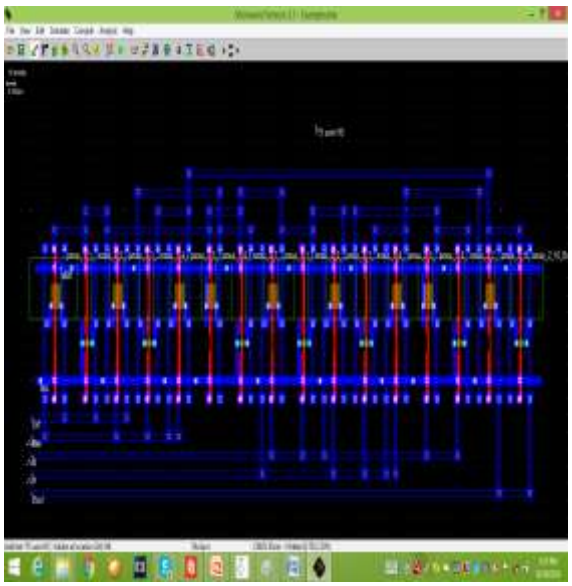


Figure 5: diagram of Conventional Full Subtractor

© 2016 IJAIR. All Rights Reserved

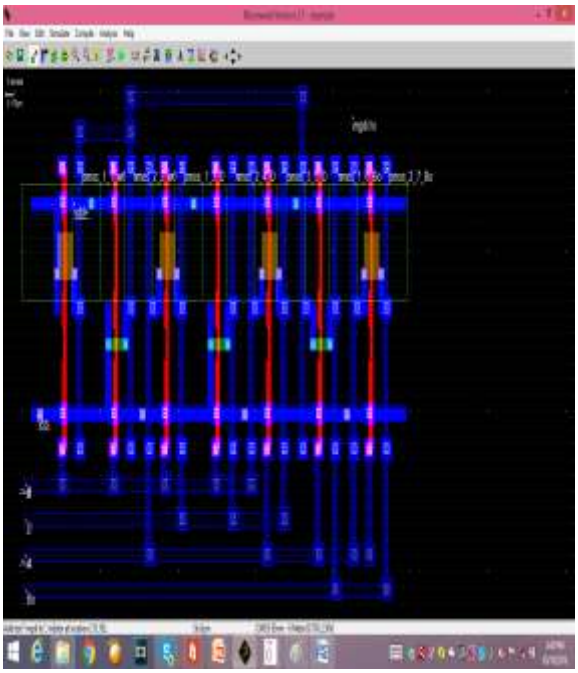


Figure 6 MGDI CMOS half Subtractor

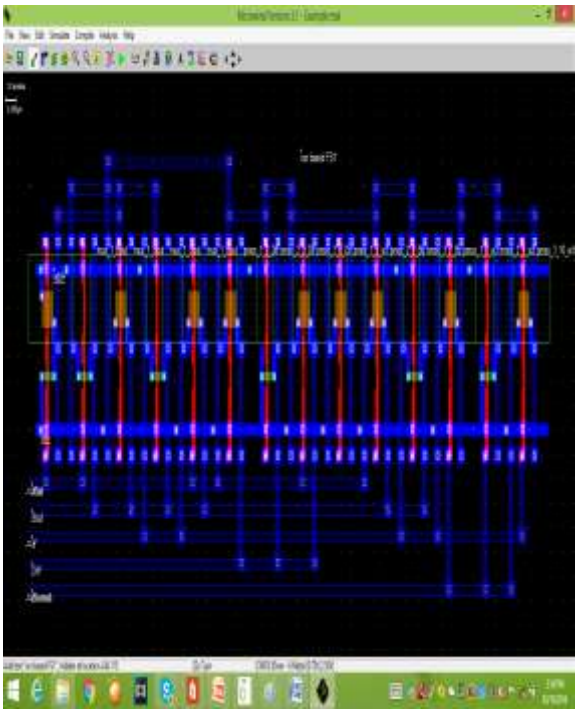


Figure 7 MGDI half subtractor

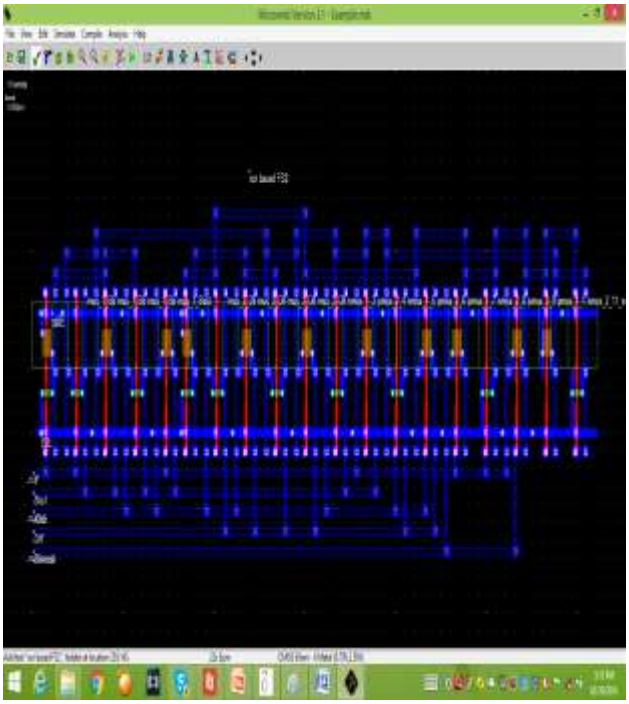


Figure 8 MGDI Full Subtractor using half subtractor And by using XOR gates and multiplexers following two designs are done.

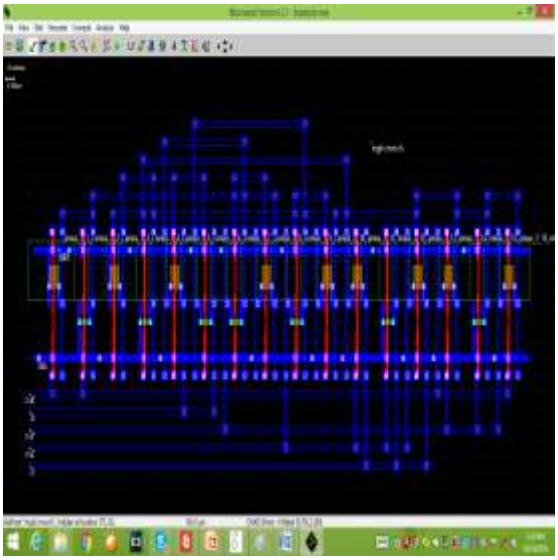


Figure9 XOR BASED SUBTACTOR 1USING MGDI TECHNIQUE

© 2016 IJAIR. All Rights Reserved

Results

The table 1 showing the result of all four subtractor designs measurements of switching delay, transistor count and area for both CMOS & MGDI techniques.

DESIGN COMPARISON

S.No.	Design Technique Used	Switching Delay (ps)		Transistors Used						AREA (μm^2)	
				CMOS Technique			MGDI Technique				
		CMOS Technique	MGDI Technique	NMOS	PMOS	TOTAL	NMOS	PMOS	TOTAL	CMOS Technique	MGDI Technique
1	Conventional Full Subtractor	110	15	26	26	52	7	9	16	625.9	354.7
2	Full Subtractor Using Half Adder	25	20	23	23	46	7	9	16	572.9	222.7
3	Full Subtractor Based on XOR Design 1	20	15	15	15	30	3	5	8	365.7	87.2
4	Full Subtractor Based on XOR Design 2	20	15	12	12	24	4	5	9	365.9	90.3

Table 1 result of different subtractor design

COMPARITIVE ANALYSIS

Parameter	CMOS Technique		MGDI Technique	
	From Base Paper	Proposed Method	From Base Paper	Proposed Method
Number of transistors used	50	30	14	8
Delay time (ps)	118.92	28	18.02	15
Surface area	324	365.7	89.2	87.2

Table 2 comparison between GDI & MGDI technique

And table 2 shows the comparative results of GDI & MGDI techniques.

Conclusion

An extensive performance analysis of modified primitive cells of AND, OR, NAND, NOR, XOR and XNOR has been presented. The performance of these MGDI was analyzed in terms of transistor count, switching delay area, and power dissipation using Design Schematic DSCH and Microwind using 65 nm technology and it is compared with conventional GDI and CMOS logic. Subsequently different 1-bit full-subtractor cells have been presented.

The significant change occurs due to the design of XOR and XNOR gate. In GDI the number of transistor to implement XOR will take 4 transistors whereas in modified GDI it is implemented with 3 transistors. In case of CMOS the transistor count is approximately double that of MGDI subtractors.

VII. ACKNOWLEDGMENT

I would like to say thanks to my guide Associate Prof. Mr. Utsav Malviya who gave knowledge and time in order to complete this paper. This paper will never complete without the support faculty member of ECE department of G.G.I.T.S College, Jabalpur

Reference

[1] Laxmi Kumre, Ajay Somkuwar, Ganga Agnihotri "Implementation of radix 4 booth multiplier using MGDI technique", 2013

[2] Addanki Purna Ramesh, Dr.A.V. N. Tilak and Dr.A.M.Prasad,"Implementation of 16-Bit Multilier – Accumulator using Radix -2 Modified Booth Algorithm and SPST adder using Verilog",(VLSICS) Vol.3, No.3, June 2012

[5] R.Uma and P. Dhavachelvan, "Modified Gate Diffusion Input Technique: A New Technique for Enhancing Performance in Full Adder Circuits", 2nd[ICCCS-2012]

[6] Design Of An Energy Efficient, High Speed, Low Power Full Subtractor Using GDI Technique, Proceeding of the **2014 IEEE** Students' Technology Symposium, Krishnendu Dhar, Aanan Chatterjee

[3] "Modified Gate Diffusion Input Technique: A New Technique For Enhancing Performance In Full Adder Circuits**"ELSEVIER 2012**. R.Uma and P.

[4] "10-t Full Subtraction Logic Using GDI Technique," **IEEE 2014.** Haramardeep Singh

© 2016 IJAIR. All Rights Reserved