Heavy Functioning Address Generator for WIMAX Deinterleaver Using FPGA

R.G.Vidhya[1], S.Sathyadevi[2], M.Niranjana Priyadharshini[3]

[1,2,3]PSNA College of Engineering &Technology,Dindigul,Tamilnadu,India
Vidhya50.ece@gmail.com[1]

Abstract— A small downward-difficulty and effort of novel procedure is able to capably execute the address generation circuitry of the 2-D deinterleaver used in the WiMAX transreceiver using the Xilinx field-programmable gate array (FPGA).The make use of an internal multiplier of FPGA and the allocation of resources for quadrature phase-shift keying(QPSK), 16-QAM quadrature-amplitude modulation, 64-QAM, and Pulse width modulations(PWM) all by the side of all the feasible code rates make my approach to be the work of fiction and exceedingly competent after compared with conventional look-up table-based approach. I suggest a bulk logic circuit for the interleaver structure to diminish hardware complication and fault rate in WiMAX structure. And also the Walsh Hadamard generation and bi-orthogonal demodulation is suggested to get better hardware using up resourcefully. The future approach gives you an idea about secret code of major improvement in the utilization of FPGA resources.

Keywords— *Address generator, 16QAM, 64QAM, PWM, FPGA, WIMAX*

INTRODUCTION

Broadband wireless access (BWA) is constantly becoming an additional demanding competitor to the predictable wired last mile access technologies[2]. IEEE has urbanized standards for mobile BWA (IEEE 802.16e) generally referred toward as mobile WiMAX. The channel interleaved functioning in the WiMAX transceiver acting an essential role in minimizing the outcome of burst error. In this brief a work of literature, small downward-difficulty, high-speed, and source fine-planned address generator for the channel deinterleaver worn out within the WiMAX transceiver by eliminating the requirement of floor function is estimated. Remarkably a small sum of industrial plant connected to hardware recognition of the interleaver/deinterleaver used in a WiMAX structure is usable in the journalism. The attempt in demonstrating the arrangement of incoming data streams obsessed to the building block towards dropping the frequency of memory access in a deinterleaver by means of a conventional look-up table (LUT) - based CMOS address generator used for WiMAX. It describes a hardware description language (VHDL) base understanding of the address generator planned in favor of IEEE 802.16e channel interleaved through the capital of only a 1/2 code rates[6]. The authors incorporated a finite-state machine (FSM) based address generator of the identical interleaver intended for all allowed code rates as well as modulation schemes. The final results are qualified by resting on the field-programmable gate array (FPGA) stage. Asghar has finished the 2-D translation of the functions damaged in WiMAX channel deinterleaver resting on the way to announce fine-planned hardware design lying on the other hand the derivations does not obviously gives the information regarding the design issues, mainly for 64-quadrature-amplitude3 modulation (QAM). Hardware is accepting of floor function be extremely not simple and consumes the oddly enormous amount of resources. Conventional LUT-based method is put up to be as horrible as many aspects such as slowness in operation, by means of huge logic assets most important to lavishness in resource burning up. A proportional learn by means of a LUT-based technique confirms the benefit of my predictable plan, at the similar time, as compared by means of the arduous and extensive expressions mostly for 16-QAM and 64-QAM, a compressed and easy to use mathematical symbol and successive algorithm is offered[6]. The mathematical terminology has officially been verified by means of 2D translations. Our estimated algorithm while is realized by means of digital hardware result in low down-problem structural plan for the address generator compared from side to side obtainable method. A complete vision of the predictable hardware compared by means of Asghar and Liu's 2D translation function is obtainable clearly. On the technique to create the diagram compressed the authors adopted optimization by the wealthy of distributing the general hardware sandwiched stuck between the modules intended for quadrature phase-shift keying (QPSK), 16-QAM, and 64-QAM. This structural plan is modeled in VHDL as fit as implemented insincere on top of the Xilinx Spartan-3 FPGA. Software imitation by means of ModelSim is performed resting on the way to show the functionality of the expected algorithm as well as hardware. FPGA understanding outcome with all possible, feasible comparison with current related work have been prepared In this concise, use of FPGA's embedded multiplier provides concert development by dropping interconnection delay, well-organized resource employment, and minor power consumption while comparing with a configurable logic block-based multiplier. My work shows betterment superior than the LUT method on the way to the tune of about 49% in terms of maximum operating frequency.

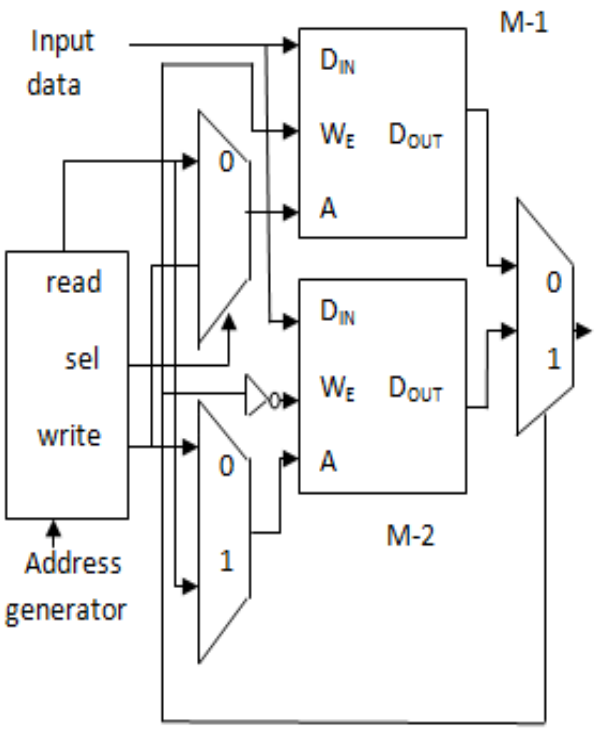

FIG1:INTERLEAVER STRUCTURE

Modulation and the structure of orthogonal frequency-division multiplexing symbols are performed through the two succeeding blocks, that is, mapper and inverse fast Fourier transforms. In the receiver, the blocks are arranged in the reverse order which enables the reinstatement of the imaginative data sequence at the output. Two-dimensional block interleave or deinterleaver structure, which is used as a channel interleave/deinterleaver in the WiMAX system, is described in fig1. It has two memory blocks, namely, M-1 & M-2 in addition to an address generator. In block interleaving, it's shown at what time one memory block is being written and read, and the process goes on vice versa.Data flow recognized from a source is randomized being a member of programmed by two forward error correction (FEC) coding techniques specifically, Reed–Solomon (RS) and convolutional coding (CC).The channel interleaver permutes the prearranged bit flow to reduce the effect of burst error. While the conventional turbo code (CTC) be used for FEC, being non-compulsory in WiMAX, the channel interleaver is not necessary since CTC it includes an interleaver contained by it[7] . Modulation and the structure of orthogonal frequency-division multiplexing symbols are performed through the two succeeding blocks, that is, mapper and inverse fast Fourier transforms. In the receiver, the blocks are arranged in the reverse order which enables the reinstatement of the imaginative data sequence at the output. Two-dimensional block interleave or deinterleaver structure, which is used as a channel interleave/deinterleaver in the WiMAX system, is described in fig1. It has two memory blocks, namely, M-1 & M-2 in addition to an address generator. In block interleaving, at what time one memory block is being written, the extra one is read, and vice versa.

II PROPOSED DEINTERLEAVER STRUCTURE

QPSK Consists of row counter and column counter where row counts gets used for generating row numbers and column counter gets used for generating column numbers in certain limit by implementing the permissible numbers $N_{cbps.}$

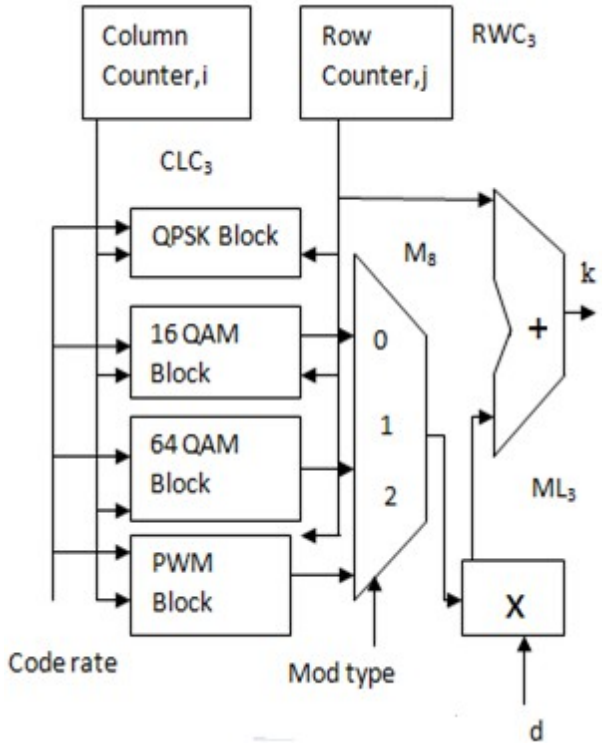

FIG2: PROPOSED DEINTERLEAVER STRUCTURE

In addition to the row counter and column counter a multiplier and adder is added in the 16QAM thereby the desired operations can be performed and implemented. Following 16QAM, 64QAM has an identical structure with some additional modules and finally PWM structure has 4bit synchronous counter instead of row counter and column counter with separate. And also its structure includes flipflops, and basic logic gates to perform the addition and other operations.

In the existing system[1], the architecture works at low speed, and also it consumes high power while analyzing with our proposed work. Therefore, we propose the Bi-orthogonal de-modulation and ML Decoder to increase the speed of the architecture and also to reduce the amount of power consumed

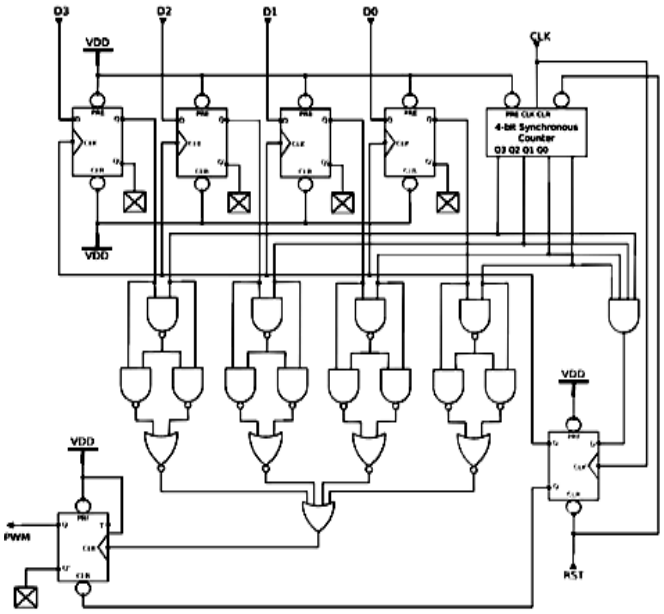

FIG3: PWM BLOCK

Walsh Hadamard is one of the orthogonal generators used in the Bi-orthogonal de- modulation. Here the two codes are said to be orthogonal when the sum of their inner product is zero. For example, if the given 4x4 matrix is said to be orthogonal only when their rows and columns are orthogonal to each other.

$$H = \begin{vmatrix} 1 & 1 & 1 & 1 \\ 1 & 1 & -1 & -1 \\ 1 & -1 & 1 & -1 \\ 1 & -1 & -1 & 1 \end{vmatrix}$$

Here if, code1={1,1,1,1} and code2={1,1,-1,-1} then their Inner Product is calculated by means of the following formula If zero exists in the answer, then the given code1 and code2 are said to be orthogonal

IV BI-ORTHOGONAL DE- MODULATOR

)+(

The received bits from the input stream entered into the modulator circuit. Basically the Bi-orthogonal De-modulator circuit consist of Correlator bank, decision device and Walsh Hadamard with Orthogonal Demux

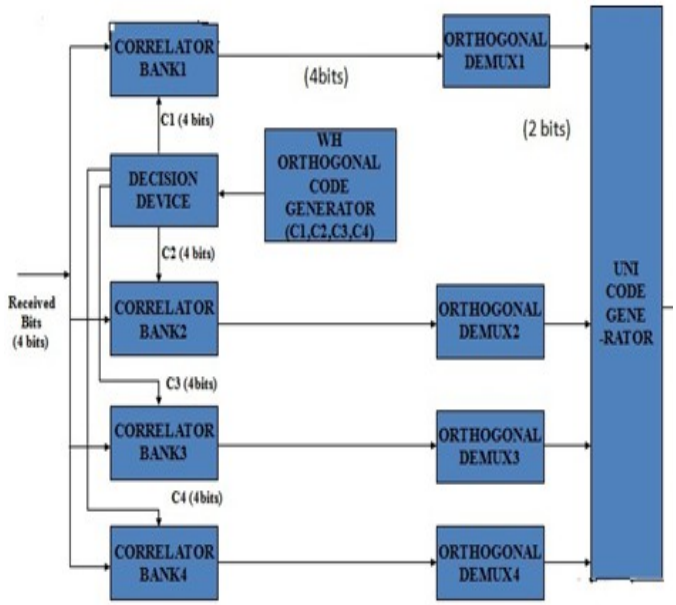

FIG4: BIORTHOGONAL DE-MODULATOR

Correlator bank is used to perform the orthogonal multiplication. Decision Device produces output 1 when the input is greater than 0. Decision Device produces output 0 when the input is lesser than 0.

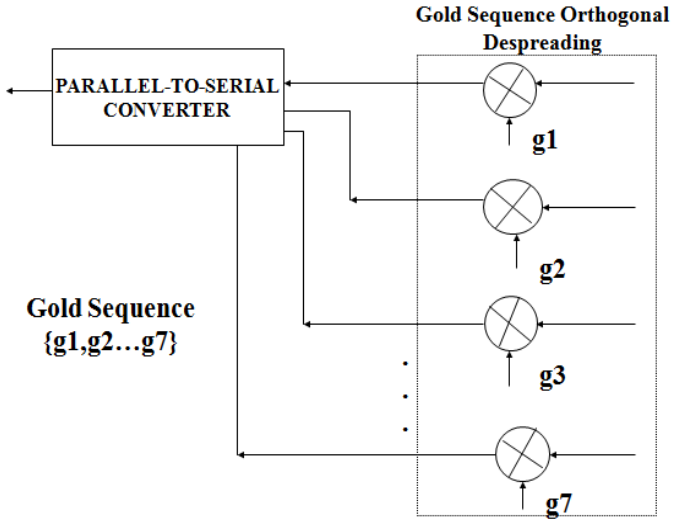

FIG5: UNICODE GENERATOR

The Unicode generator consists of two blocks,namely parallel to serial converter,and Gold Sequence Despreader. Where the P/S Converter converts the data bits into the number of branches according to the length of Gold Sequence

V. SIMULATION RESULT

The planned hardware of the address generator is transformed into a Verilog program by means of the Xilinx ISE. Simulation Outcomes are obtained for all allowable modulation types and code rates by means of ModelSim XE-III and a part of the same for N_{cbps} = 576-bits, 3/4 code rate, 64-QAM and PWM has been offered in Fig.2. The initial portion of Fig.2 shows the last part of addresses for the first row (j = 1),and the latter part (from ruler) shows the addresses for the second row (j = 2). And the simulation Outcomes are established with the output obtained from the Modelsim version 6.1.

VI. IMPLEMENTATION RESULT

The Verilog program urbanized for the planned WiMAX deinterleaver address generator is downloaded on the Xilinx Spartan-3E (Device XCS3S100E) using FPGA . Table2 shows the HDL fusion report. As the FPGA-based implementation of the WiMAX deinterleaver address generator has been created and the direct comparison of the results is carried out in our proposed work[10]. In the conventional LUT-based technique of address generation for the WiMAX 2-D deinterleaver , the LUTs are modeled by means of FPGA's embedded memory, i.e., block RAM is mainly used to decrease the memory access time. For the equality of comparison,three block RAMs gets used,.In the proposed method in addition to the three block RAM one extra block RAM is added to decrease the latency thereby the speed gets increased.and also the power compression is deeply discussed using the Bi-orthogonal demodulation . Table2 shows the comparison between the two implementations with respect to FPGA resources (XCS3S100E). This evaluation clearly proves the low difficulty. That is,the address generator using the proposed technique can work 5% faster than the latter and consumes 34mWatts power.

Hardware Specifications	Requirements
VLSI Technology	90nm
Family	Spartan 3E
Device	XCS3S100E
Package	PQ208

TABLE1: HARDWARE SPECIFICATIONS

Performance Evaluation Parameters	BIJOY KUMAR[1]	Proposed Method
Latency	4.93ns	4.655ns
Power Consumption	82mW	34mW

TABLE2: PERFORMANCE ANALYSIS

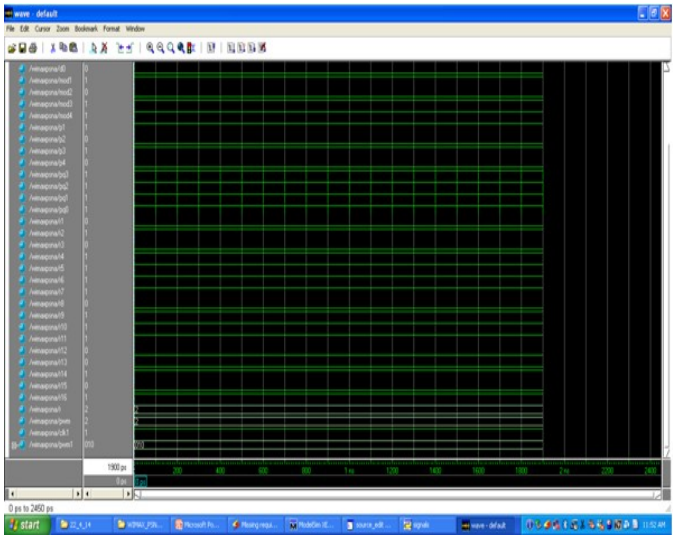

FIG6: SIMULATION RESULT FOR ADDRESS GENERATOR

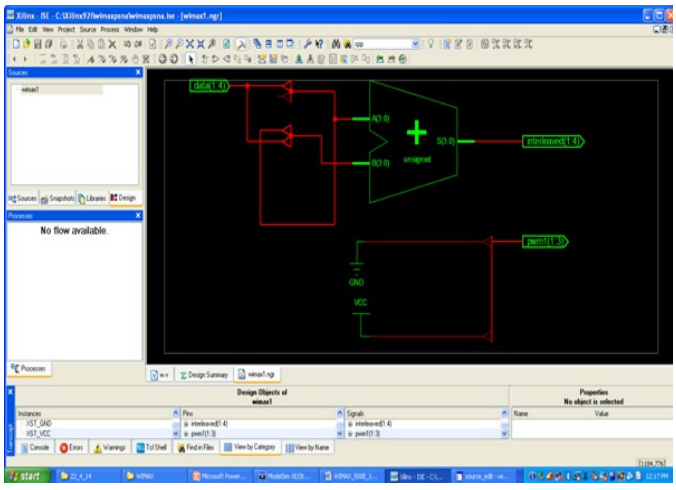

FIG7: RTL SCHEMATIC VIEW OF ADDRESS GENERATOR

VII. CONCLUSION

This concise has projected a novel algorithm all along with its mathematical formulation, together with the evidence for the address generation circuitry of the WiMAX channel deinterleaver sustaining all promising code rates and the modulation patterns as per IEEE 802.16e. The projected algorithm is also transformed into an optimized digital hardware circuit. The hardware is implemented on the Xilinx FPGA by means of Verilog. A evaluation of our projeced work with a conventional LUT-based method and also with a recent work shows major enhancement on resource utilization and operating frequency.

REFERENCES

[1]Bijoy Kumar Upadhyaya" Efficient FPGA Implementation of Address Generator for WiMAX Deinterleaver*" IEEE Transactions On Circuits And Systems—Ii: Express Briefs, VOL. 60, NO. 8, Aug2013*

[2]W. Konhauser, "Broadband wireless access solutions—Progressive challenges and potential value of next generation," *Wireless Pers. Commun.*,vol. 37, no. 3/4, pp. 243–259, May 2006

[3]B. Li, Y. Qin, C. P. Low, and C. L. Gwee, "A survey on mobile WiMAX,"*IEEE Commun. Mag.*, vol. 45, no. 12, pp. 70–75, Dec. 2007.

[4]] *Xilinx Spartan-3 FPGA Family: Complete Data Sheet*, Xilinx, Inc., San Jose, CA, USA, 2012.

[5]B. K. Upadhyaya, I. S. Misra, and S. K. Sanyal, "Novel design of address generator for WiMAX multimode interleaver using FPGA based finitestate machine," in *Proc. 13th Int. Conf. Comput. Inf. Technol.*, Dhaka,Bangladesh, 2010, pp. 153–158.

[6] R. Asghar and D. Liu, "2D realization of WiMAX channel interleaver for efficient hardware implementation," in *Proc. World Acad. Sci. Eng.Technol.*, Hong Kong, 2009, vol. 51, pp. 25–29.

[7] *IEEE Standard for Local and Metropolitan Area Networks —Part 16: Air Interface for Fixed Broadband Wireless Access Systems—Amendment 2*, IEEE Std. 802.16e-2005, 2005.

[8] M. N. Khan and S. Ghauri, "TheWiMAX 802.16e physical layer model,"in *Proc. IET Int. Conf. Wireless, Mobile Multimedia Netw.*, Mumbai,India, 2008, pp. 117–120.

[9] J. G. Andrews, A. Ghosh, and R. Muhamed, *Fundamentals of WiMAX:Understanding Broadband Wireless Networking*. Upper Saddle River,NJ, USA: Prentice-Hall, 2007, ch. 8.

[10] B. K. Upadhyaya and S. K. Sanyal, "An improved LUT based reconfigurable multimode interleaver for WLAN application," *Int. J. Recent Trends Eng. Tech., ACEEE*, vol. 6, no. 2, pp. 183–188, 2011

.

