A Review on FM0/Manchester Encoder Design and Implementation on FPGA

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***Abstract*— Now a day's secure data transmission is becoming the concern area and demand of providing security to data before transmission is become important task in communication system to provide such task some schemes were used called encoding scheme. Various applications use these encoding schemes to protect the data which is not to be disclosed to unauthorized user. Miller, FM0, and Manchester encoding are some names which is basically used to obtain this task. Each technique has its own importance depends on the application and used according to the need. Each of the technique is so robust so that it can provide results without losing any of its parameter. All these encoding techniques generally use finite state machine to provide the output at a high speed. The architecture of Miller, FM0, and Manchester encoders has balanced DC output that is the advantage of using this technique. And that also reduced the requirement of number of transistors. This paper presents a review on number of scholars work.**

***Keywords*— VLSI architecture, DSRC, Manchester encoder, Miller encoder, FM0 encoder, SOLS technique, FPGA.**

I. INTRODUCTION

DSRC (dedicated short-range communication) is a technique used especially for intelligent transportation systems based on one- or two-way medium range communication. Vehicle-to-vehicle and vehicle-to- roadside are the two categories of DSRC. The main aim for deploying DSRC is to enable collision avoidance applications. These applications depend on frequent data exchanges among vehicles, or between vehicle and roadside infrastructure. The U.S.Department of Transportation (DOT) has conclude that vehicle-to-vehicle (V2V) communication based on DSRC can address up to 82% of all crashes in the United States involving unimpaired drivers, potentially saving thousands of lives and billions of dollars. The National Highway Traffic Safety Administration (NHTSA) within the U.S. DOT plans to decide in 2013 whether to use rules to require or encourage deployment of DSRC equipment in new vehicles in the US. In vehicle-to-vehicle, for safety issues and public information announcement DSRC activated the message sending and broadcasting among vehicle. The Safety issues consist of inters cars distance, blind-spot, collision-alarm, and intersection warning. The vehicle-to-roadside focuses on the intelligent transportation service, such as automatic electronic toll collection (ETC) system. With ETC, the toll collecting is electrically or automatically accomplished with the contactless IC-card platform. Moreover, the ETC has application such as payment for parking-service, and gas- refueling. Thus, the DSRC plays an important role in automobile industry. The DSRC standards have been implemented by several organizations in different countries. These DSRC standards are shown in Table I.

TABLE I
DSRC STANDARDS

	Europe	**America**	**Japan**
Organization	CEN	ASTM	ARIB
Carrier Frequency	5.8GHz	5.9GHz	5.8GHz
Data Rate	500kbps	27 Mbps	4 Mbps
Modulation	ASK/PSK	OFDM	ASK
Encoding (Downlink)	FM0	Manchester	Manchester

The data rate individually targets at 500 kbps, 27 Mbps, and 27 Mbps with carrier frequency of 5.8 and 5.9 GHz. The modulation methods includes such as amplitude shift keying, phase shift keying, and orthogonal frequency division multiplexing. Generally, the Waveform of transmitted signal is expected to have zero mean for robustness noise, and this is also referred to as dc-balance. The transmitted signal consists of arbitrary binary sequence, (1 or 0) which is difficult to obtain dc-balance. The goal of FM0 and Manchester codes can provide the transmitted signal with dc- balance. Both FM0 and Manchester codes are widely designated in encoding for downlink.

The encoding techniques used in communication convert information into a suitable form for transmission. Encoding techniques can also be used for security purposes. In general, different types of encoding techniques can be used for serial communication application. There are several types to encode the data such as Miller encoding, Manchester encoding, FM0, NRZ, FM1, RZ, etc. This type of encoding techniques is used on the transistor level, so it can be used with optical communication as well as minimizing the critical path, area, delay, and buffer size by adding a minimum number of buffers. A baseband processor consist of a UHF RFID Reader, PIE encoder, FM0 decoder, or Miller decoder are used for encoding and decoding purposes application, achieving higher efficiency and accuracy. But in order to do this, it needs to

have a high frequency clock. The system architecture of DSRC transceiver is shown in Fig. 1.

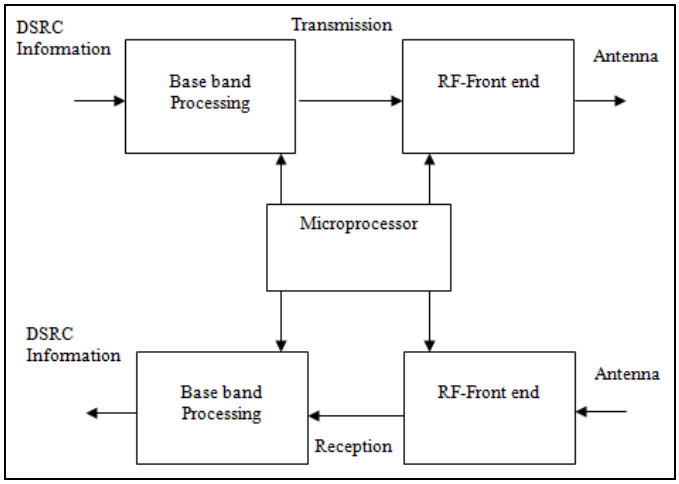

Fig. 1 Example of an image with acceptable resolution

II. Literature Review

Reference [1] proposed a fully reused VLSI architecture using SOLS technique for both FM0 and Manchester encoding. SOLS technique eliminates the limitation on hardware utilization by two core techniques: area compact retiming and balance logic-operation sharing. Area-compact retiming reduces the hardware like number of transistors and with the help of balance logic operation sharing identical logic components can be efficiently combines with the FM0 and Manchester encoding. The proposed method works on some parameters like TSMC, maximum operating frequency, Power consumption etc. This paper not only develops a fully reused VLSI architecture, but also exhibits a competitive performance compared with the existing works. Reference [2] presents a review on Manchester, Miller, and FM0 Encoding Techniques. This paper presents the design strategies of the entire circuits Manchester, Miller, FM0, and a finite state machine. This paper also presents compression studies of all the techniques.

Reference [3] presents a review paper that presents a theoretical background of FM0 and Manchester and this paper also describe the utility of FM0 and Manchester encoding and how it can be used for DSRC. In DSRC DC-Stability and signal reliability is the requirement that is fulfill by FM0 and Manchester. In Reference [4] unbalance computation time results in the glitch at the input of MUX−1 that causes logic-fault on coding. In this paper this problem can be overcome by using XNOR with the inverter rather that XOR and this becomes the input of the MUX-1. And this can balance the computational time. The adoption of FM0 or Manchester code depends on Mode and CLR signal. In this design both modes separately allocated to system controller. Whether FM0 or Manchester code is adopted, all the logic component of the proposed VLSI architecture is utilized and provides better results.

In Reference [5], presents a review that presents a system of VLSI architecture of FMO/ Manchester encoding using SOLS technique and also compare this technique with other techniques. The SOLS consists of two core methods such as area-compact retiming and balance logic-operation sharing. The area-compact retiming technique relocates the hardware resource to reduce 22 transistors. The balance logic- operation sharing technique efficiently combines FM0 and Manchester encodings with the fully reused hardware architecture. With SOLS technique, we constructs a fully reused VLSI architecture of Manchester and FM0 encodings for DSRC applications. This paper not only implements a fully reused VLSI architecture, but also exhibits a competitive performance compared with the existing techniques. Reference [6] proposed a system to minimizing the problem of coding-diversity between FM0 and Manchester encodings that causes the limitation on hardware utilization of VLSI architecture design. In this paper, the fully reused VLSI architecture using SOLS technique for both FM0 and Manchester encodings is proposed. Area compact retiming and balance logic operation sharing are the two core techniques that are used to eliminate the limitation on hardware utilization by reducing the number of transistor and by combining the resources of FM0 and Manchester encodings. This paper is realized in180nm technology with outstanding device efficiency. The power Consumption is 29392.843nW for Manchester encoding and FM0 encoding.

Reference [7] proposed a fully reused VLSI architecture using SOLS technique for both FM0 and Manchester encodings. The coding diversity between FM0, Manchester and Miller encodings causes the limitation on hardware utilization of VLSI architecture design. The area compact retiming and balance logic operation sharing techniques eliminates the limitation on hardware utilization. Area compact retiming concept relocates the hardware resource and to reduce the number of transistors effectively. The Balance Logic operation sharing technique combines FM0 and Manchester encodings with the identical logic components to produce balanced computation time. Every component is active in both FM0 and Manchester encodings and it will greatly improve the hardware utilization rate to 100% and reduce the power consumption. The FM0 and Manchester encoders are designed with these techniques to achieve high speed and fully reconfigured VLSI architecture for application system. In future the design can be implemented using high performance FPGA devices. Reference [8] proposed a fully reused VLSI architecture using SOLS technique for both FM0 and Manchester encodings. The SOLS technique eliminates the limitation on hardware utilization by two core techniques: area compact retiming and balance logic-operation sharing. The SOLS technique improves the hardware utilization rate from 57.14% to 100% for both FM0 and Manchester encodings. The performance of this paper is evaluated on the post layout simulation in Taiwan Semiconductor Manufacturing Company (TSMC) 0.18-µm 1P6M CMOS technology. The maximum operation frequency is 2 GHz and 900 MHz for Manchester and FM0 encodings, respectively.

The power consumption is 1.58 mW at 2 GHz for Manchester encoding and 1.14 mW at 900 MHz for FM0 encoding. The core circuit area is 65.98×30.43 μm2. This paper not only develops a fully reused VLSI architecture, but also exhibits an efficient performance compared with the existing works.

Reference [9] presents a review on Evaluation of various forms of DSRC system. DSRC is the only short-range wireless alternative today that provides Fast Network Acquisition, Low Latency, High Reliability when Required, Priority for Safety Applications, Interoperability, Security and Privacy which is one of the challenging task faced by all in the worldwide. This article deals with active Dedicated Short Range Communications (DSRC) application for Intelligent Transport Systems (ITS) and its economic evaluation focused on many wireless systems like vehicle communication, mobile Communication etc. Reference [10] proposed SOLS technique to prevent wide code diversity that limits the hardware utilization rate of such a reusable encoder. To implement a system that has its own advantages like smooth traffic control, vehicular safety etc DSRC communication protocol is used this system encode the message and transmit it to other DSRC. The data is encoded using FM0 and Manchester encoding that causes the problem and can be overcome by using SOLS technique. The SOLS encoder is of better advantage than the normal reusable encoder in terms of device utilization. Besides the logic delay and memory usage of the system also get reduced.

Reference [11] presents Miller encoding which is integrated with FM0 and Manchester encoding architecture for the application of Dedicated Short Range Communication (DSRC). These three encodings have same similarities and clock rate embedded within the transmitted data. Using similarities in the FM0, Manchester and Miller techniques, hardware architecture is to be developed using SOLS technique. This paper not only develops a fully reused VLSI architecture, but also exhibits a competitive performance compared with the existing works. In reference [12] SOLS technique is introduced to solve the hardware utilization problem caused at the time when both the FM0 and Manchester encoding is used to encode the message in DSRC. By considering two parameters area compact retiming and balance logic-operation sharing. This reduces the hardware setup problem by reducing transistor and combines FM0 and Manchester encodings with the identical logic components respectively.

Reference [13] in this paper, the fully reused VLSI architecture using SOLS technique for both FM0 and Manchester encodings is proposed. The SOLS technique eliminates the limitation on hardware utilization by two core techniques: area compact retiming and balance logic-operation sharing. The area-compact retiming relocates the hardware resource to reduce the transistors. The balance logic-operation sharing efficiently combines FM0 and Manchester encodings with the identical logic components. This paper is realized in 180nm technology with outstanding device efficiency. The power consumption is 29392.843nW for Manchester encoding and FM0 encoding. Reference [14] proposed SOLS technique to overcome the problem of hardware utilization of VLSI design used for the DSRC dedicated short-range communication. The DSRC standards typically adopt FM0 and Manchester codes to succeed in dc-balance, enhancing the signal irresponsibleness. Still, the coding-diversity between the FM0 and Manchester codes seriously limits the potential to style a completely reused VLSI design for each. The SOLS technique improves the hardware utilization rate from fifty seven.14% to 100% for each FM0 and Manchester encodings.

Reference [15] This paper shows the encoding technique of FMO and Manchester with SOLS technique eliminates the limitation of hardware utilization by two core techniques (a)Compact of Area Retiming (b)Sharing of Logic Operation. Using compact of area retiming, the number of transistor is reduce to 22 transistors. The sharing of logic operation combines FMO and Manchester encodings. The maximum operating frequency of Manchester, FMO encodings are 2 GHz, 900MHz with consumption of power 1.58mW, 1.14mW respectively. Reference [16] the limitation on hardware utilization of VLSI architecture design can be caused due to coding-diversity between FM0 and Manchester encodings. A limitation analysis on hardware utilization of FM0 and Manchester encodings is discussed in detail. In this paper, SOLS technique is used fully reused VLSI architecture for both FM0 and Manchester encodings. The limitation on hardware utilization can be eliminating by using SOLS technique by two core techniques: area-compact retiming and balance logic-operation sharing. The area-compact retiming relocates the hardware resource to reduce the number of transistors. The balance logic operation sharing efficiently combines FM0 and Manchester encodings with the identical logic components.

Reference [17] proposed a method for power reduction in VLSI architecture using FM0 and Manchester encoding. Power is reduced by reducing the number of components used and improves the performance of the FM0 and Manchester encoding. These results are observed using spice. The power consumed is 0.72 mw for Manchester encoding. The power consumption is 0.14 mw for FM0 encoding. The FM0 and Manchester encoding is used widely in dedicated short range communication. Signal reliability could be achieved in dedicated short range communications by adopting FM0 and Manchester encoding. In reference [18] the paper presents coding diversity between FM0 and Manchester encodings that causes the limitation on hardware utilization of VLSI architecture design. The fully reused VLSI architecture using SOLS technique for both FM0 and Manchester encodings are proposed. Which can eliminates the limitation on hardware utilization. The ACR technique relocates the hardware resource to reduce the transistor count. The BLOS efficiently combines the FM0 and Manchester encodings with the identical logic components. The SOLS technique improves the Hardware Utilization Rate (HUR) from 57.14% to 100% for both FM0 and Manchester encodings. The balanced hardware architecture is realized in different CMOS technology this paper not alone develops a fully reused VLSI architecture, but also exhibits an efficient performance compared with the

existing works. In reference [19] coding diversity becomes the problem that limits the potential to design the VLSI logic, to overcome the problem SOLS(Similarity oriented logic simplification) technique is designing encoder architecture which eliminates the limitation of two core technique such as area- compact retiming Balance logic operation sharing. This Project Not only develops encoder VLSI architecture but also Exhibits an efficient performance compared with existing encoder in terms of power and area. Due to the improved hardware utilization, area is compact and Power consumption gets reduced in encoding techniques.

Reference [20] proposed multimode hardware architecture for a digital baseband encoder which incorporates Manchester, Differential Manchester and FM0 codes. These codes help in achieving good DC balance thereby improving signal reliability. Alternating Manchester with Differential Manchester for different intervals of time improves security at the physical layer level. This work aims at efficient integration of hardware components for the three coding modes. The design has been implemented in Xilinx Virtex 5 FPGA. This multimode encoder operates at a maximum frequency of 434 MHz. The power consumption is 34 mW at 434 MHz. When compared with the similarity-oriented logic simplification (SOLS) based integrated FM0/Manchester encoder, this encoder poses the advantage of an extra encoding operation– Differential Manchester encoding despite a slight increase in area and power.

III. CONCLUSIONS

The study on papers already published gives an overview about the technique and design strategies basically used to provide security. This paper presents a common review that explains the entire explanation for Manchester and FM0 encoders. This encoding concept will be used in future for various applications.

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