Designing of High Speed, Low Cost 32-bit Modified SQRT Carry Select Adder in 45nm Technology

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Abstract **—Digital logic circuits have became the indispensible part for all electronics gadgets based on arithmetic and logical operations, the complexity of designs are increasing with each generation due to increasing need of number of task, since all the arithmetic operation are dominated by addition, therefore increasing the performance of the adder will increase the performance of the whole design. In this work, A comparison between Carry Select Adder and Square root Carry Select Adder has been done as they provide tradeoffs between area, power, delay (latency). By providing schematic changes in regular design, a significant improvement has been done in area, power, and delay. In this work a modified basic circuit that is the core digital circuit in design has been used, beside this a significant schematic change has been done in half adder and Ex-OR Gate circuit design, Entire work has been completed in 45nm CMOS process Technology using TANNER TOOL.**

***Keywords*— Low Cost Design, BEC, Modified Ex-OR Gate, High Speed Digital ICs, SQRT CSLA, Tanner Tool**

I. INTRODUCTION

Addition is the process used frequently in most digital arithmetic and logical operation, since all the binary arithmetic operation viz. addition, subtraction, multiplication, division etc. are based on the addition. Computer uses binary addition and requires adders. Number of adders have already designed and provide tradeoffs between power, delay and area. Ripple carry adder, having the most basic and simple structure with small area, but suffer from high delay. Just opposite carry look ahead adder having the high speed but suffer from large area and high power consumption. Carry select adder also have same improvement results in high speed but has large area problem with high power consumption [2]. In square root carry select adder a significant enhancement in speed has been achieved by applying some schematic changes in design but still suffer with large area problem. Which is solved by use of Modified BEC circuit in place of RCA with C_{in} =1. Transistor level modification has been applied in Exclusive OR circuit which is the most common circuit used in whole design either that is half adder, full adder or Binary to Excess-1 converter. Due to this modification, a drastic reduction in area of square root CSLA design has been achieved with high speed.

II. BASIC CARRY SELECT ADDER

A carry-select adder performs two additions in parallel, one assuming a C_{in}= 0, the other a C_{in}= 1. The speed of the Carry Select Adder is improved by predicting the carry input and performs the addition. Carry select adder presume the carry as '0' and '1' and calculate carry and sum. Ultimate result is determined by selecting accurate carry by Multiplexer [1]. CSL approach reduces "addition time" to "addition selection time" for the higher stages. The internal logic schematic of a carry select adder constructed using the conventional 4-bit ripple carry adder (RCA) shown in fig.1. The RCA uses multiple full adders and half adder to perform addition operation. Although Half adder is used only at very first stage (LSB) of the Binary adder, where C_{in}=0. Each full adder inputs a carry-in, which is the carry-out of the preceding adder. The CSLA divides the bits to be added into blocks and forms two sums for each block in parallel, one with assumed carry in (C_{in}) of 0 and the other with C_{in} of 1. As shown in Fig. 1, the carry-out from one stage of 4-bit RCA is used as the select signal for the multiplexer. This selects the corresponding sum bit from the next block of data. This speeds-up the computation process of the Binary adder. Thus, the Carry Select Adder achieves higher speed of operation at the cost of increased number of devices used in the circuit [3]. This in turn increases the area and cost of the circuits.

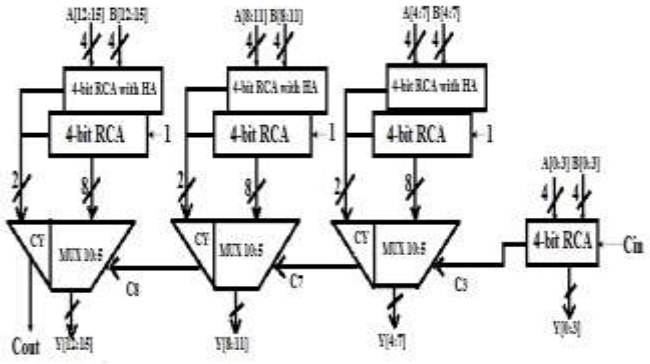

Fig.1: 16-Bit Carry Select Adder

III. Modified SQRT CARRY SELECT ADDER

The major drawback of the CSLA is its large area because double RCAs used. To overcome this drawback Single RCA and BEC are used instead of double RCAs [1]. In Modified Square Root Carry Select Adder, Importance of BEC logic is to reduced transistor count in comparison of regular carry select adder, moreover Modified SQRT Carry Select Adder is better than Regular Carry Select Adder because in regular CSLA, the overall delay is the sum of 4-bit RCA (LSB) delay and sum of multiplexer's delay while in Modified SQRT CSLA, The overall delay will be the sum of 2-bit RCA (LSB) delay and sum of delay of multiplexers as shown in Figure 2, i.e. greatly reducing the overall delay. Therefore, resultant Modified SQRT CSLA is area efficient, Providing High speed than regular CSL. For possible area reduction we used a modified Ex-OR Gate.

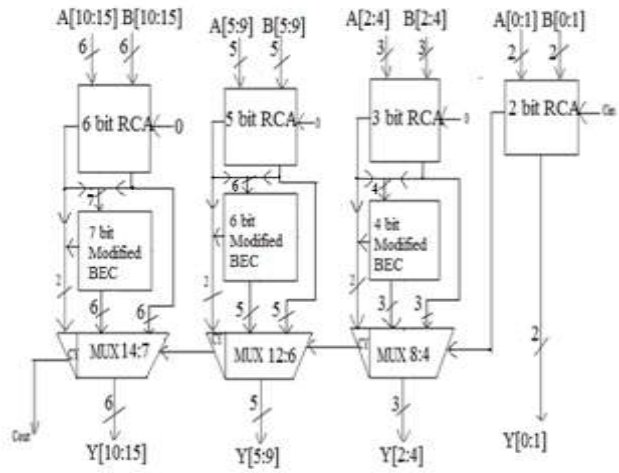

Fig.2: 16-bit Modified SQRT Carry select adder

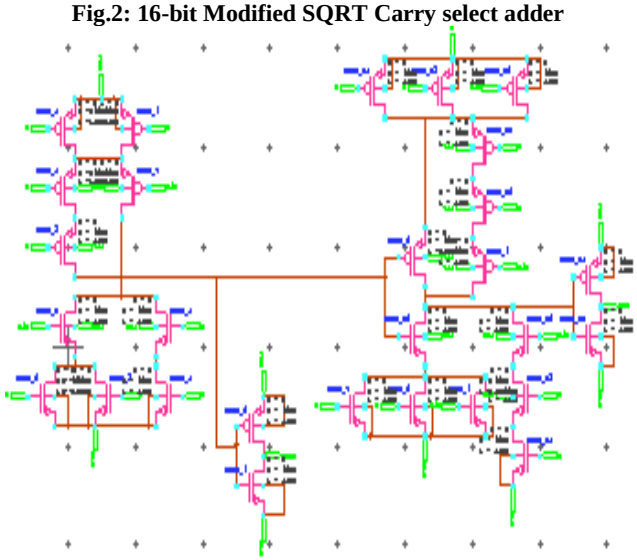

Fig.3: Schematic diagram of Full Adder on Tanner

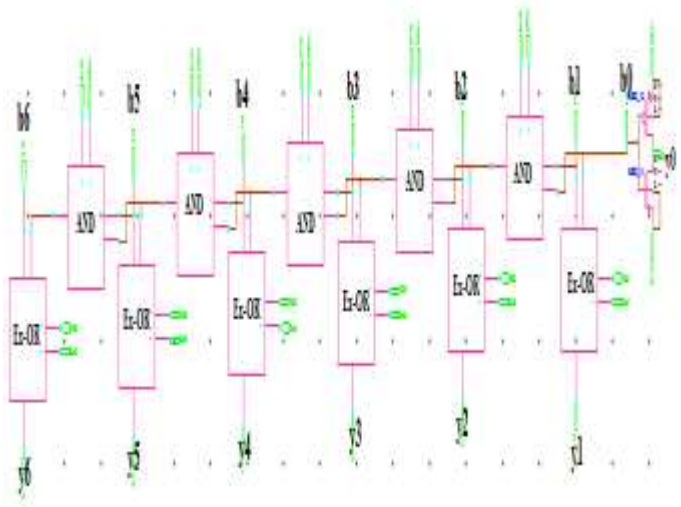

Fig.4: 7-bit BEC implemented on Tanner

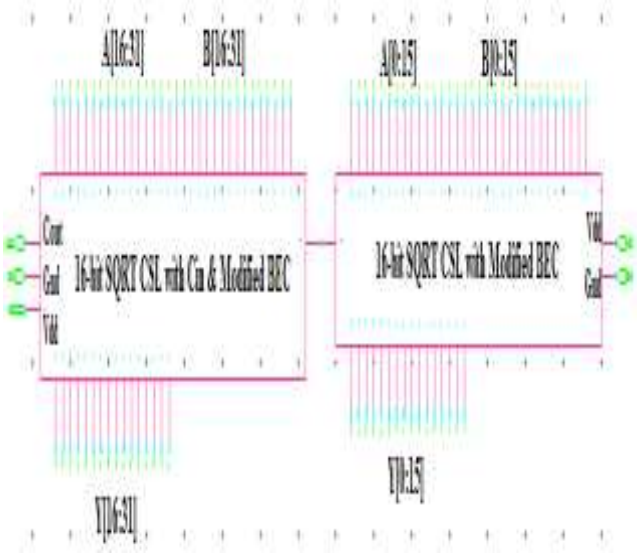

Fig.5: 32-bit Modified SQRT Carry Select Adder implemented on Tanner

IV. IMPLEMENTATION AND RESULT

The entire circuit designs in this paper have been developed and simulated using TANNER TOOL 14.11 version in 45nm CMOS Process technology. Results and comparison of performance parameters after the simulation of proposed design and regular CSLA Design are shown in Table 1 in figure 7 respectively. It is clear with the analysis of results and comparison chart that proposed design is a High Speed and Low Cost (Area Efficient) Design with the negotiable penalty of power consumption as compared to regular Carry Select Adder Design (CSLA).

TABLE 1 (RESULTS)

S. No.	Design Name	Average Power(µW)	Area (in terms of transistor count)	Delay (ns)
1.	32-bit CSLA (Regular)	19.97	1916	3.253
2.	32-bit Modified SQRT CSLA (Proposed)	23.06	1772	2.416

Comparison Charts for Area, Delay and Power Consumption between Regular Carry Select Adder (CSLA) and Modified SQRT Carry Select Adder (SQRT CSLA) are given in figure 7, 8 and 9.

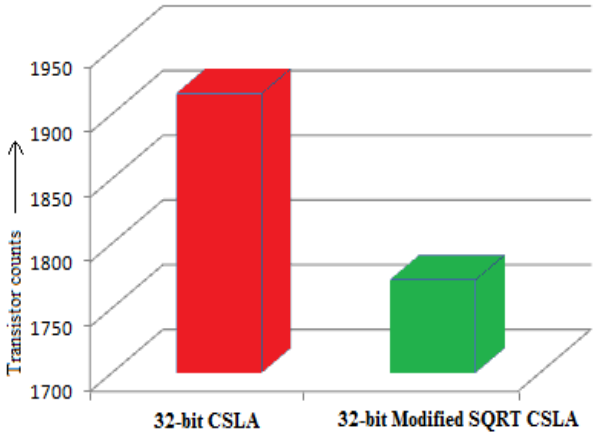

Fig.6: Comparison of Area in terms of Transistor count

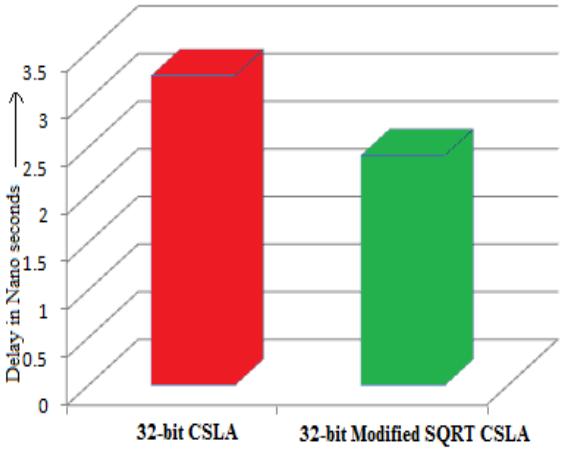

Fig.7: Comparison of Delay in nanoseconds

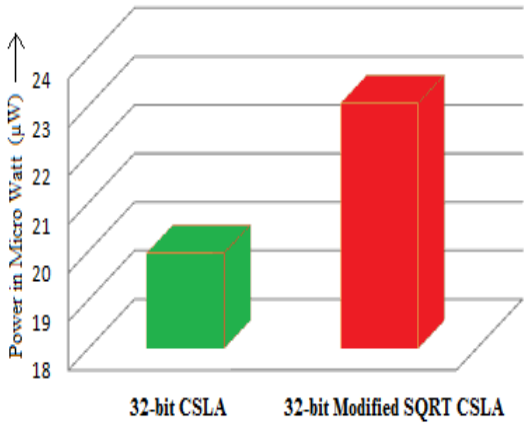

Fig.9: Comparison of Power Consumption in (µW)

V. CONCLUSION

The Proposed Modified SQRT Carry Select Adder, provide tremendous improvement in Delay and Area with a negligible penalty of Power Consumption. Modified SQRT Carry Select Adder based on the characteristic of Conventional digital VLSI design. The Modified SQRT Carry Select Adder design performs at high speed better than other adders in high speed category with a negligible power loss that is compensated by its significant low cost because large number of transistors are saved by Efficient Transistor level Modeling used to design the Modified SQRT Carry Select Adder as compared to Regular CSLA and SQRT CSL. The proposed modified SQRT CSLA architecture is therefore, Low Cost, High Speed Binary Adder. It would be interesting to test the design of the modified 64-bit, 128-bit SQRT CSLA.

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