Multiple Cell Upset Correction using Decimal Matrix Code for Enhanced Memory Reliability–A Review

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***Abstract*— An important issue in the field of data storage is the transient multiple cells upsets (MCUs) when the consideration is reliability of memories exposed to the radiation environment. There are many enhanced packaging techniques are offered which defend the memory data from radiations and transients. On the other hand, a particular packaging provides safety from a limited variation of radiations. Owing the increasing demand in the application in wireless communication field the devices are exposed to surrounding switch is having a very wide range of radiations. Subsequently, some additional data protection techniques like Error correction codes (ECCs) are always chosen for authenticating the data before it is processed. These protection techniques use encoded data to be stored in memories. An error correction code uses redundant bits to minimized delay overhead in data correction are be stored in the memory. A review on memory data error detection and correction code is presented in this paper.**

***Keywords*—Decimal Addition, Error Correction Codes (ECCs), Error Syndrome, Hardware Memory, Multiple Cell Upsets (MCUs).**

I. INTRODUCTION

The rising demand of scaling down of CMOS technology to deep nano-scale and that are exposed to space environment radiations are the cause for rapidly increasing the soft error rate in memory cells. The charge stored as data in semiconductor memory are affected by the radiations that have ionizing characteristics introduces the soft error in the memory. The phenomena of error generation due to radiation that affect the memories t are exposed to the environmental radiations is represented with the help of memory block are shown by fig. 1. In figure it is shown that M0 - M7 is the Memory Data Byte (eg, 10110101) to be send when this memory data is exposed to the Radiation memory data is being affected by the radiation and the send bits gets changed to eg, (10111100). Here now a major concern about memory reliability is single-bit error but in some cases "multiple-bit error" or "multiple cell upset" (MCUs) becomes a serious dependability concern. In order to tolerant the faults in the memory up to the maximum possible level there are many researchers recommend some error correction codes (ECCs). A simple block diagram of the fault tolerant memory encoder implementation is shown in fig. 2.

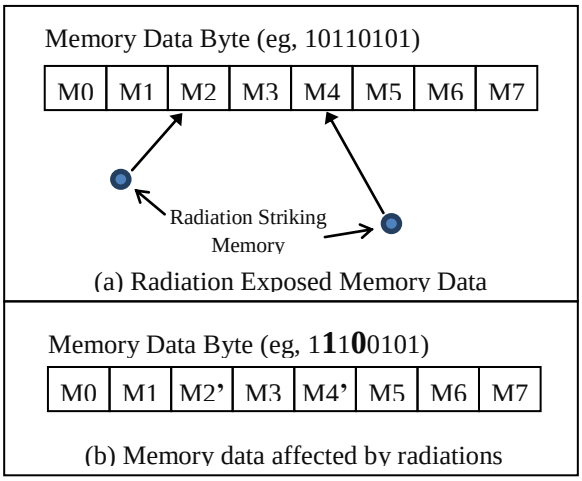

Fig. 1 Soft Error caused in Semiconductor Memory due to exposure to Energy Radiation

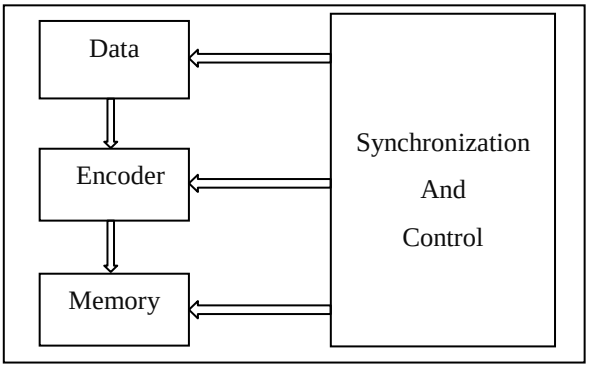

Fig. 2 A simple data encoder block

For error correction codes a block is needed to encode the data to be stored in the memory and these data is first generate redundant bits. Memory interface is use to store the redundant bits in the memory with the help of memory interface. The errors from the memory data is corrected by these redundancy bits handled by Decoder. Only some of the most reliable codes include Reed-Solomon (RS) code Bose-Choudhary-Hocquenghem (BCH) code, and Punctured Difference Set (PDS) code. These are the codes that have been used to deal with MCUs in memories. The rearrangement of the cells in the physical arrangement to break up the bits into different physical words from the same logical word is done by interleaving technique to control MCUs. The practical use of Interleaving with content-addressable memory (CAM) is not

possible with the fixed coupling hardware architecture from both comparison circuit structures. There are number of researches proposed against MCUs for a single error correction and double error detection technique like Built-in-Current-Sensors (BICS). 2-D matrix is a code for efficiently corrected the MCUs per word .In this code matrix the word is divided into multiple columns and multiple rows, and Hamming code and Parity code were use to protect the bits per rows and per columns. Here, the bits per row are protected by Hamming Code and the bits per column are protected by parity code. Vertical syndrome bits are used to detect the two bit error using Hamming code. The 2-D MC is proficient of correcting only two errors in all cases. As compared to other codes this code has a lower delay overhead.

A novel decimal matrix code (DMC) is proposed in this paper. To provide improved memory reliability the proposed code is based on divide-symbol. Decimal integer addition (decimal algorithm) on the divided symbols of binary code is utilizes by the proposed DMC. A logic comparator is used by the decoder to detect and correct error bits in the proposed work to find the error syndrome. The decimal algorithm is used to enhance the capability of the code to provide the consistency. The rest of this paper is arranged as follows: section-II presents the work published by some recent scholars under the title 'Literature Review'. Section III presents the conclusion based on the literature review. Work is discussed in section-V.

II. LITERATURE REVIEW

In reference [1] novel per-word DMC was proposed to assure the reliability of memory. To detect errors the proposed security code utilized decimal algorithm, as a result of that more errors were detected and corrected. The results achieved shows that the proposed scheme has a superior protection level against large MCUs in memory. Furthermore, an adequate level of immunity is provided by the proposed decimal error detection technique to detect MCUs in CAM because it can be combined with BICS.

In reference [2] presents the relative study of various error correcting codes which defines variousalternate to prevail over dependability issue of memories, when exposed to radiation. To avoid the occurrence of MCUs several error correction codes (ECCs) are used, though for higher delay overheads the main problem is that they require complex encoder and decoder architecture. To minimize the area and delay overheads by comparing with the existing techniques like hamming, matrix codes, built in current sensor etc the proposed system uses decimal matrix code (DMC), and improvement of the memory consistency is obtain by enhancing the error correction capability. A decimal correction code is proposed in reference [3] for the execution of error correction technique In order to preserve a good level of consistency, and various error detection and correction codes are used to protect memory cells using protection codes i.e Matrix codes (MCs) based on hamming codes have been proposed for storage protection. Furthermore, the area overhead is minimized without interrupting the whole encoding and decoding operations with the help of the encoder-reuse technique (ERT).

Reference [4] proposed a system for memories for detection and correction of errors was 64-bit decimal matrix code. To pass up MCUs from causing data corruption, more complex error correction codes (ECCs) are widely used to protect memory, however higher delay overhead is the main problem is that they would require. Recently, hamming codes based matrix codes (MCs) have been proposed for memory protection. In proposed system 32-bit decimal matrix code increased error detection and correction rate.

In reference [5] the proposed mechanism which derived from hamming code are single error correction-double error detection–triple-adjacent error detection using and single error correction-double error detection –double adjacent error correction Codes resulting From Orthogonal Latin Square Codes will provide single and double adjacent error correction and double nonadjacent and triple error detection. Double adjacent errors are corrected by this combined code. To assure the reliability of memory novel DMC was proposed in Reference [6] hereto detected the errors proposed scheme use decimal algorithm for protection code, as a result further errors were detected and corrected. The protection level against large MCUs in memory is better chandelled by the proposed algorithm. Moreover, the proposed decimal error detection technique is an attractive opinion to detect MCUs in CAM because it can be shared with the BICS to provide an adequate level of protection.

In Reference [7] two Error Correction Codes are used such as Parity Matrix Code (PMC) and Decimal Matrix Code (DMC). Decimal algorithm is uses DMC utilized to obtain the maximum error detection capability. Furthermore, the Encoder-Reuse Technique (ERT) is utilized to play down the area overhead of additional circuits without upsetting the whole encoding and decoding processes. PMC uses hamming algorithm to detect errors, so that more errors can be detected and corrected. To minimize the area overhead of extra circuits PMC utilizes Encoder-Reuse Technique (ERT). The number of redundant bits is also less in PMC scheme.

In reference [8] to supply fault-tolerant memory cells, Error Correction Codes (ECCs) are used, but the requirement of such codes is more power, area, and higher delay overhead. Thus with less decoding display multiple errors are detected and corrected by Matrix Codes (MCs) which is based on Hamming codes and parity codes. The correction of the error is possible with this matrix code is up to two errors. Hence to take full advantage of the potential of error detection and correction, Decimal Matrix Code (DMC) based on decimal algorithm is used. For fault tolerant memory protection DMC uses reuse technique for encoder. The use of this algorithm enables furthermore errors to be detected and corrected by the utilization of large number of redundant bits. To reduce the number of redundant bits framework can be modified by using parity matrix codes in which a 32 bit data is divided into 2bits of 16 blocks. VHDL language is used for Coding.

In reference [9] the detection of the errors or the protection code is utilized by decimal algorithm, thus more errors were

detected and corrected. The final results show that the proposed scheme has a better protection level in opposition to large MCUs in memory. Moreover, the proposed decimal error detection technique is an attractive opinion. Here the protection of trustworthiness has achieved by changing Carry Save Adder (CSA). Traditional 2-D repair approach is combined with the proposed technique such that row and column failures and defects on multiple bits are isolated and repaired and defects are handled by the SEC-DED codes. This method would provide a complete approach to protect against soft errors and in memories. Then a method has been proposed that can deal with both types of errors efficiently by applying a modified error correction process. However, for small fault rates and low failure probabilities throughout device operation, the probability of hidden failures will be negligible. Reference [10] proposed work focuses on the design of HMC for which a hybrid matrix code improved memory consistency against multiple cell upsets.For security it required less number of redundant bits as compared to the accessible approaches. The proposed scheme results with better-quality protection level against large MCUs in memory.

In Reference [11] proposed scheme introduce decimal algorithm for the detection and correction of the errors hence, DMC was proposed to assure the reliability of the memory. The projected scheme shows that it has a superior security level against large MCUs in memory and it is accomplished from the obtained results. Here the only shortcoming is that more redundant bits are required to maintain higher dependability of memory, therefore a logical combination of k and m should be chosen to minimize the number of redundant bits and maximize memory reliability based on radiation experiments in actual implementation.

In reference [12] to correct or detect the error due to which the soft error rate in storage cell is quickly increased proposed a encoder reuse technique with DMC. Decimal Algorithm based Matrix Code (DMC) was proposed technique that uses decimal algorithm to obtain the error detection and correction capability. The Encoder-reuse technique (ERT) based on DMC is use to minimize the area. Primarily, a 2 D matrix is prepared to set up data bits that are split into symbols. DMC encoder performs the decimal operation to computed Horizontal Redundant Bits (HRB) and Vertical Redundant Bits (VRB). After encoding, the receiving codeword that is stored in the memory. Condition arises when the radiation affects the memory, Multiple Cell Upset problem will happen. Hence the Decoder is used to solve the trouble that can be rectified. Result outcomes shows that the ECC based DMC yields enhanced performance compared to Hamming Code.

Reference [13] proposed a prevention technique to protect the memories from the MCUs that is decimal code matrix. In the proposed method implementation of the 128 bit Decimal Matrix code for detection and correction of errors in the memories and maintaining memory reliability are used. The proposed DMC increase the error detection and correction ability, power, decrease the area, maintain the memory reliability, and redundant bits will be reduced. Reference [14] proposed security code DMC utilized decimal algorithm to detect errors, so that more than one error were detected and corrected.. In Reference [15] Decimal Matrix Code algorithm is proposed and that perform decimal ex-or and addition/subtraction operation to detect and correct errors present in the memory. The power consumed less power by the decimal matrix code than the other existing codes. The only drawback of DMC is the more number of redundant bits.Reference [16] proposed HMC (Hybrid Matrix Code) to assurance the dependability of the memory.The main disadvantage of proposed HMC is which more number of redundant bits is obliged to keep up higher reliability.

In reference [17] Enhanced protection to memory detection is proposed DMC for multiple MCUs which would be overcome with the help of encoder that use technique DMC. Reference [18] proposed DMC which provides an competent error correction code in which the dependability and security of the memory is improved. The proposed code uses decimal algorithm which acquire integer subtraction and addition which is simpler than the binary algorithm which performs bit wise logical operation.

III. Conclusion

To assure dependability of a memory a 128-bit word is encoded and decoded with the help of proposed DMC in presence of MCUs with reduced performance overheads. The circuit area of DMC can be minimized with the help of the encoder circuit. This represents the reduction of the area overhead of extra circuits.

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