Design and Implementation of Serializer for SERDES Transceivers

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***Abstract*— Serial interconnects are the backbone of the modern communication, so the choice of SerDes architecture can have a good impact on system cost and performance. With the help of serializer and deserializer in the communication system, the power consumption and number of interconnects in the circuit can be reduced with respect to parallel communication. This paper reports a design of serializer architecture with the help of multiplexer and double edge trigger flip flop. Concept used behind designing the block of serializer is of CMOS Transmission Gate i.e. Pass Gate. The advantage of this technique in which input is sampled with clock which is half of the original clock and is distributed for the same functional throughput, which results in power saving in clock distribution network. This proposed Serializer architecture is designed using GDPK- 180 CMOS Technology and simulation is done using Cadence Virtuoso with a supply voltage of 1.8V.**

***Keywords*— DETFF, Serializer, SerDes, Cadence Virtuoso**

I. INTRODUCTION

Future technologies will allow the integration of hundreds of billions of transistors on a single chip allowing the fabrication of chips with hundreds of processing cores. System on chip and system in package technologies provide a path for continuous improvement in cost, size, power and performance at the system level without relying upon conventional CMOS scaling alone. So, IC designers should focus on the communication between these cores in order to meet the design requirements in terms of speed, area, power consumption, and time to market constraints.

Using conventional parallel buses to transmit data on-chip is not efficient anymore in terms of area, given that in new technologies interconnects do not scale at the same rate as transistors do and in terms of power due to large number of drivers, repeaters and buffers. Also, parallel buses suffer from timing errors due to jitter, and crosstalk that eventually limit the performance. One of the solutions to solve these on-chip communication issues is to replace conventional parallel buses with serial links.

As Serial link has been used from many decades for Off- chip communication since it provides many advantages over parallel link which includes lesser pins, reduced space requirements, less complexity, lower power consumption, smaller interconnects, less electromagnetic interference hence better noise immunity. The increasing trends in SoCs and SiPs technologies demand integration of large number of buses and metal tracks for interconnections.

On-Chip SerDes Transceiver is a promising solution which can reduce the number of interconnects and offers remarkable benefits in context with power consumption, area congestion and crosstalk. Use of SerDes is beneficial when frequency rate increases beyond 500MHz (i.e. 1000Mbps). Fig. 1 shows the block diagram of on- chip SerDes Transceivers for the on-chip networking.

In this paper Serializer are implemented using multiplexer. But the circuit has limitation with the multiplexer due to which it is implemented using DETFF. During the transition of the clock, the data is also changing. This creates a condition where the system does not understand whether the data is 1 or 0. DETFF (double edge trigger flip flop) emphasize on the concept of setup time. Hence, in this paper circuit is implemented using DETFF.

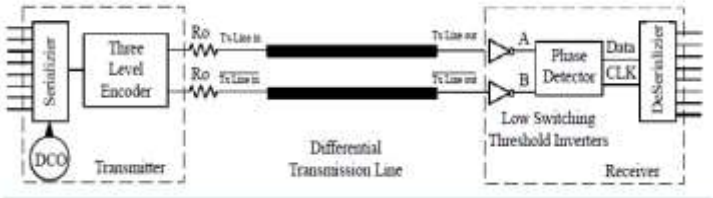

Fig. 1 Block Diagram of SerDes Transceivers

II. SERIALIZER ARCHITECTURE

The block diagram representation of the serializer is shown in Fig. 2. In this serializer is implemented using DETFF (double edge trigger flip flop). DETFF is implemented using two D flopflops, 1 latch (D Latch) and a multiplexer i.e., 2*1 MUX. The DETFF architecture and block diagram is shown in figure 3 and figure 4 respectively. These flipflops are implemented using the input D and clock signal. Also figure shows Serializer produced the data sequence in order of D1, D2, D3, D4, D5, D6, D7, D8, D1, D2,..... which means output is produced according to the input provided. The schematic of Serializer using Multiplexer and DETFF is shown in the figure 5 and figure 6 respectively.

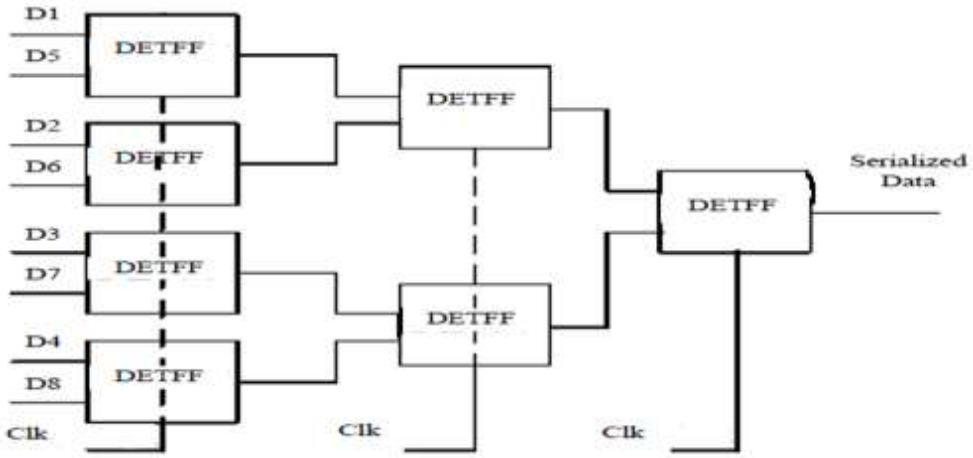

Fig.2 Block Diagram of Serializer

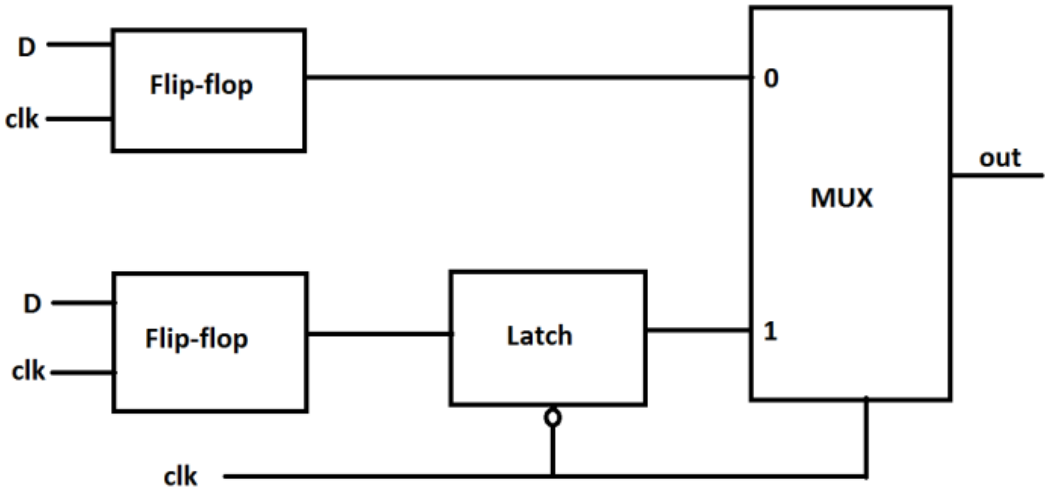

Fig. 3 Block Diagram Of DETFF

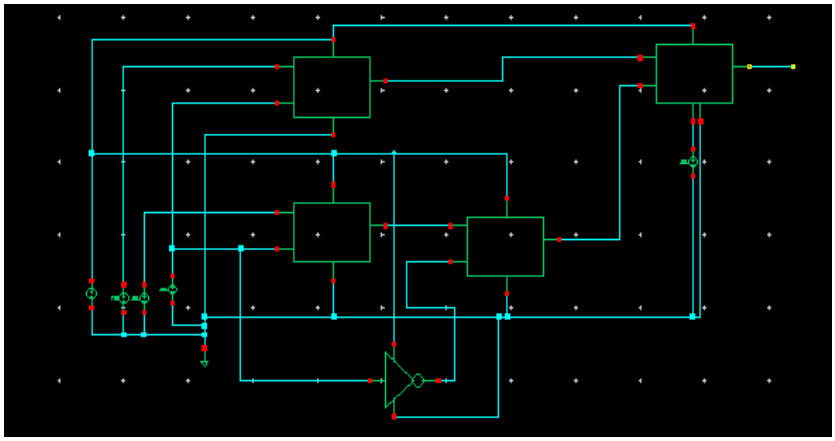

Fig. 4 Design/ Schematic of DETFF

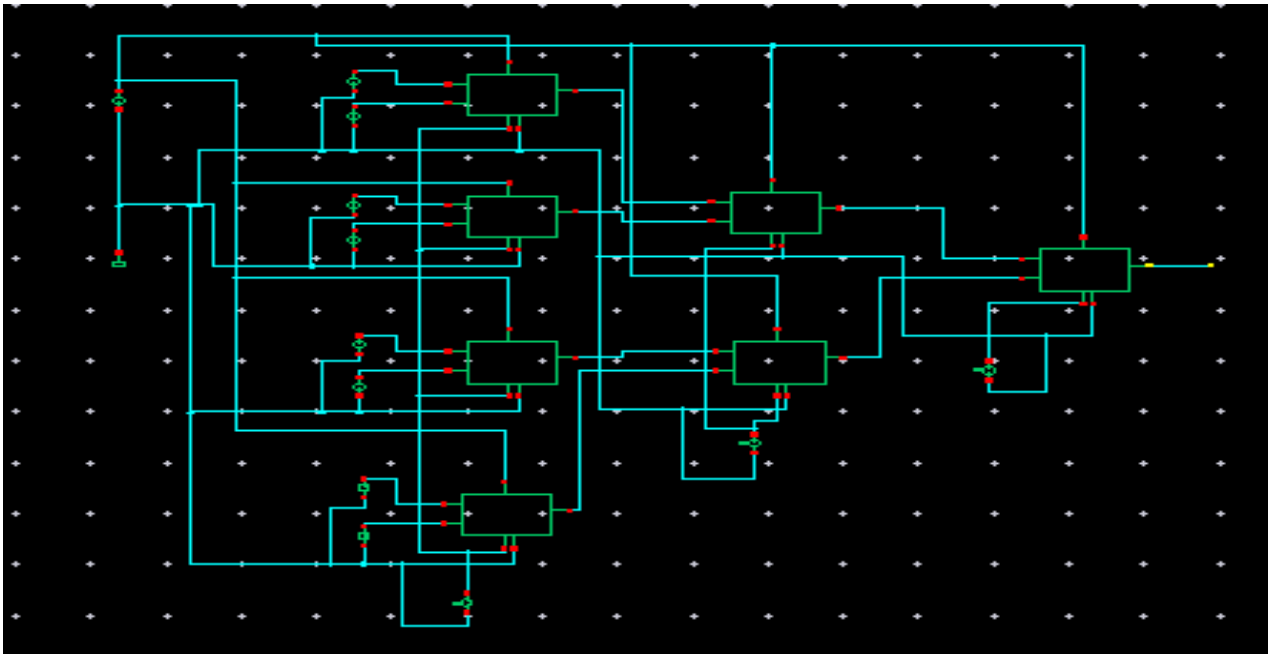

Fig.5 Design/ Schematic of Serializer using Multiplexer

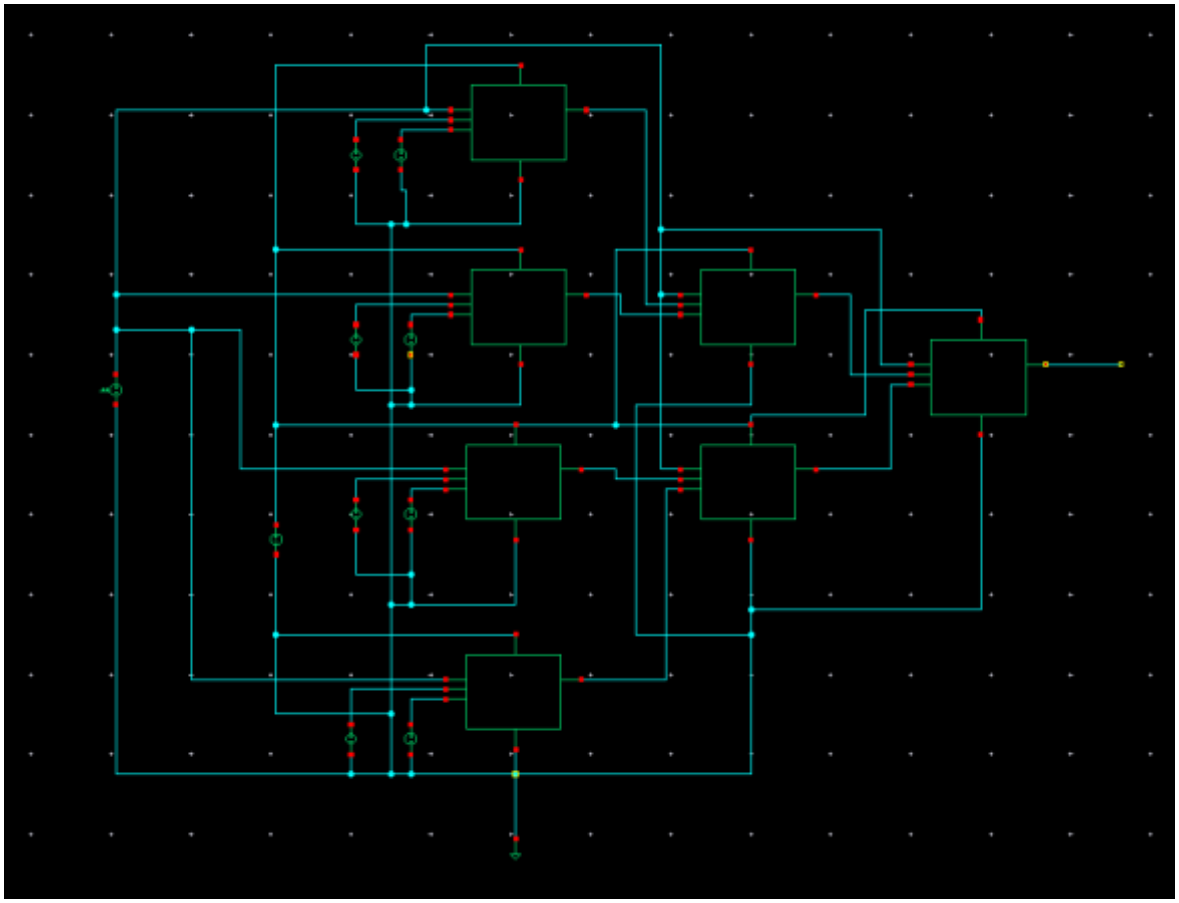

Fig.6 Design/ Schematic of Serializer using DETFF

The Serializer architecture is designed using a GDPK-180 library of Cadence and simulation is done using Cadence Virtuoso with a supply voltage of 1.8V.

Here the parallel data inputs is 1, 1, 0, 1, 0, 1, 1, 0 and used voltages for each individual parallel data input is as follows: D1=1.8V, D2= 1.8V, D3= 0V, D4= 1.8V, D5= 0V, D6= 1.8V, D7=1.8V, D8= 0V.

Both the design of the serializer i.e., serializer with multiplexer and DETFF serialize the 8- bit parallel data at 625 MHz, 312.5 MHz and 156.25 MHz.

III. CONCLUSION

In this paper, serializer is designed and implemented using multiplexer and DETFF for the basic functional blocks of SerDes transceivers. The serializer implemented with the help of CMOS Transmission gates i.e. Pass gates. Firstly Pass gates is implemented with the help of which Multiplexer, D latch, D flip flop, DETFF and finally Serializer is implemented using both the multiplexer and DETFF.

The advantage of using the serializer with DETFF is mentioned in the introduction of the paper. The whole circuit is implemented in Cadence Virtuoso (library used- gdpk-180)

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