Bypassing Technique Based Braun Multiplier for Low Power Consumption with Improved Speed

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***Abstract*— A multiplier is one of the key hardware blocks in most digital and high performance systems such as FIR filters, digital signal processors and microprocessors etc. If the power consumption of the multiplier block reduced, then reduction of the power consumption of various digital signal processing chips and communication systems could be possible. In this paper 4/8/16 bit Braun multiplier has been designed using bypassing technique and a comparative study of all bypassing techniques on the basis of their power consumption is done. At the last stage of the multiplier KSA (Kogge Stone Adder) and RCA (Ripple Carry Adder) is used for high speed and the low power consumption. The implementation of Braun multipliers and its bypassing techniques is done using Verilog HDL Xilinx 14.4 ISE and it is verified using the Spartan6, device xc6slx45. After comparing, it is concluded that mixed bypass multiplier is best suited for situations where both delay and power are low. The number of slices & LUT used is also less when compared to other techniques. For 16 bit Row and Column Bypassing Technique using KSA the delay and power found to be 28.118 ns and 0.184 Watt From other two methods (Row Bypass and Column Bypass) it is found to be (28.679ns & 0.190 Watt) and (28.518 ns and 0.184 Watt) respectively.**

***Keywords*— Column Bypass, KSA, Mixed Bypass, RCA, Row Bypass, Verilog HDL.**

I. Introduction

Multiplication is one of the essential operations in Digital Signal Processing (DSP) applications like Fast Fourier Transform (FFT), Digital filters etc. [1]. In DSP applications, most of the power is consumed by the multipliers, hence low power multipliers must be designed in order to reduce the power dissipation in DSP applications. With advancement in the technology, many investigators have examined and are trying to design multipliers which will offer the following design characteristic – Accuracy, low power consumption, high speed, regularity of layout, less complexity and less area or the combination of all these characteristic in one multiplier thus making them appropriate for several low power consumption, high speed, less area in compact VLSI implementation. The multiplication is an arithmetic operation for common DSP application, such as digital filter, digital communication system, microprocessor, Fast Fourier Transform (FFT), portable and battery operated devices. In order to achieve the high speed and low power demand in DSP applications, parallel array multipliers are generally used. One such commonly used parallel array multiplier is the Braun's multiplier. The Braun's multiplier is generally called as the CSA (Carry Save Array Multiplier). The architecture of a Braun's multiplier consists of AND gates and full adders. Power consumption is mainly due to the Static and Dynamic power consumption. Static power consumption is very small so our major concern is the Dynamic power Consumption which have to be reduced using Braun Multiplier so that our portable devices will have a long life. When Braun multiplier is used without Bypassing technique then power consumption can be increased this disadvantage can be removed by using Braun multiplier using bypassing technique and at the last stage of the bypassing based multiplier KSA and RCA can be used to improve the switching speed and for the low power consumption.

II. The Adders

Ripple Carry Adder Ripple carry adder can be designed by cascading full adder in series i.e. carry from previous full adder is connected as input carry for the next stage [1]. Multiple full adder circuits can be cascaded in parallel to add an N-bit number. For a 4- bit parallel adder, there must be 4 number of full adder circuits. A Ripple Carry Adder is a logic circuit in which the carry-out of each full adder is the carry in of the succeeding next most significant full adder. It is called a Ripple Carry Adder because each carry bit gets rippled into the next stage. In a Ripple Carry Adder the sum and carry out bits of any Half Adder stage is not valid until the carry in of that stage occurs.

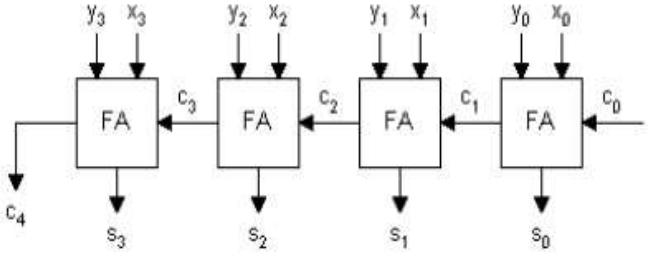

Fig1. 4-bit Ripple Carry Adder

Kogge Stone Adder The Kogge-Stone Adder concept was given by Peter M. Kogge and Harold S. Stone and was published in 1973. In Ripple Carry Adder the carry input of Full Adder is dependent on the carry output of the previous Full Adder and present Full Adder wait until the previous Full Adder has generated output. Hence delay is more for the Ripple Carry Adder if no. of bit increases, then delays also

increases, so for reducing this delay Kogge Stone Adder (KSA) is used. Three computational stages are used in Kogge Stone Adder these are Preprocessing, Carry generation network, Post processing.

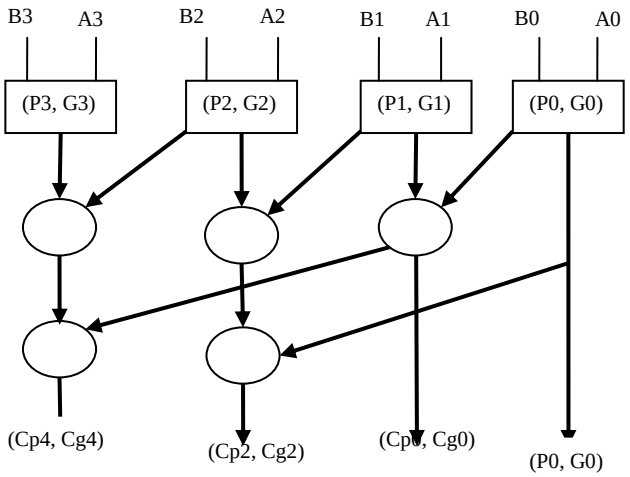

Fig2. 4 bit Kogge Stone Adder

III. Bypassing Technique

Bypassing means to turn off some row or column when their outputs are known or in other words, we can say that Row or Column may be turn off when either multiplicand or multiplier or both bits have zero value. To reduce the switching activities three types of bypassing techniques are used in this project these are: -

- Row bypassing multiplier
- Column bypassing multiplier
- Row and Column bypassing multiplier

The Basic building blocks used for the construction of all these Bypassing based multiplier is FA cell (Full Adder cell). This Full Adder cell is constructed by using one Full Adder, Multiplexers and Buffers.

IV. Row Bypassing Multiplier

In Row bypassing multiplier if multiplier bit b_2 is zero in below figure then partial products output is directly given to the third row from the first row and the second row is disabled. But when the rightmost full adder in the second row is disabled then addition is not executed and it would not give a correct answer so some extra circuitry is required which is shown in the triangle area. This is the drawback of Row Bypassing Multiplier.

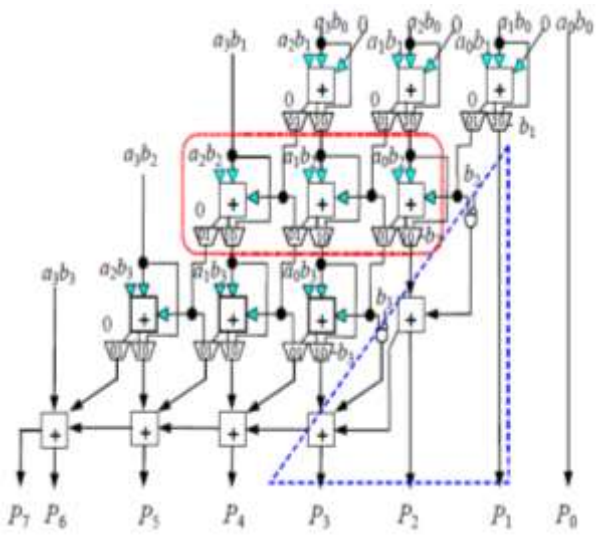

Fig3. A 4*4 Braun Multiplier with Row Bypassing

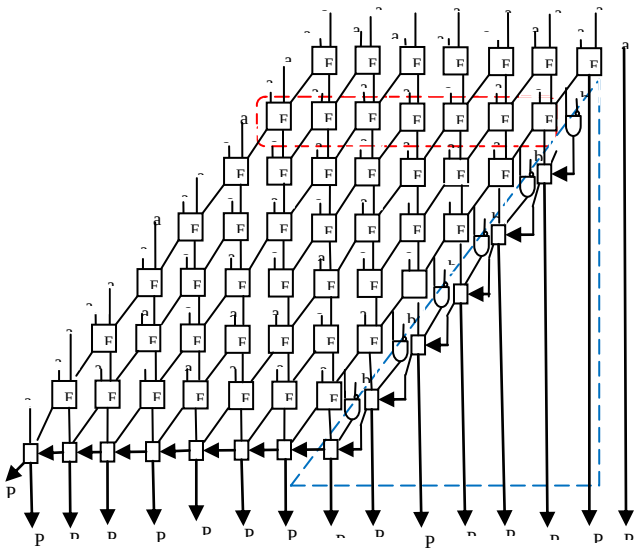

Fig4. A 8*8 Braun Multiplier with Row Bypassing

One of the drawbacks of this Row bypassing Braun multiplier is that if the rightmost FA cell in the second row is disabled then it would not give a correct result, so to obtain an accurate result in some extra circuitry is required which is shown in the above figure enclosed by the blue triangle area. This drawback can be reduced by using a Column bypassing multiplier.

V. Column Bypassing Multiplier

The drawback of the Row Bypassing technique can be minimized by using column bypassing multiplier and it is used when multiplicand bit is zero. To design 4*4, 8*8 and 16*16 bit Braun multiplier with Column bypassing, the basic building block is FACELL (Full adder cell). This FACELL can be designed by using full adder, multiplexer, buffer. A 4*4 column bypassing multiplier can be implemented by using (n-1)*(n-1) full adders, (n-1)*(n-1) multiplexers and 2*(n-1)*(n-1) buffers.

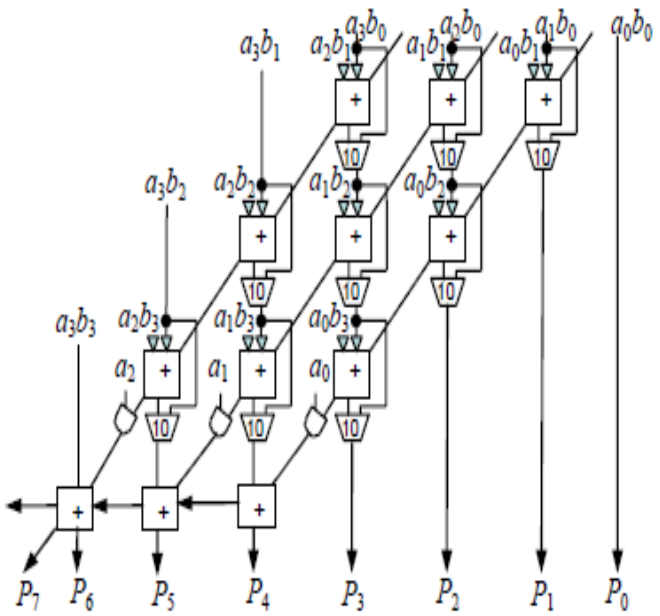

Fig5. 4*4 Column Bypassing Based Braun Multiplier

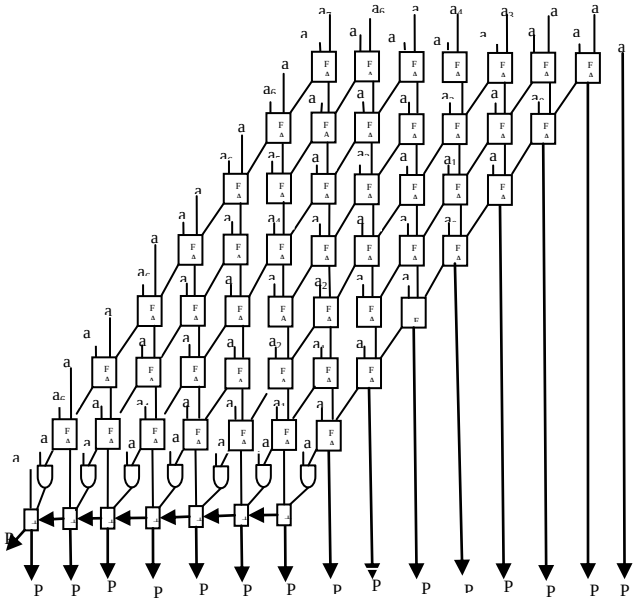

Fig6. 8*8 Column Bypassing Based Braun Multiplier

VI. Row and Column Bypassing

In mixed bypassing multiplier the addition operations in the i-th column or the j-th row can be bypassed if the a_i bit in the multiplicand is 0 or the b_j bit in the multiplier is 0. The basic building block for the designing a 4*4 Row and Column bypass multiplier is FA cell and it can be implemented by using (n-1)*(n-1) full adders, 2*(n-1)*(n-1) multiplexers and 2*(n-1)*(n-1) buffers.

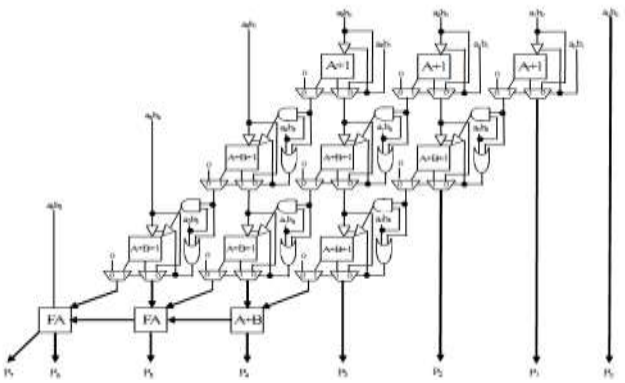

Fig7. 4*4 Column Bypassing Based Braun Multiplier

The circuitry of this Row and Column bypassing multiplier is complex from other two bypassing techniques. In this, in each stage of CSA array AND gate and OR gate is used which increases the hardware complexity.

VII. Synthesis and Simulation Result

The synthesis of Braun multiplier has been performed by using Xilinx ISE 14.4 tool & simulation has been done using Isim 14.4 simulation tool on Spartan 6 family, device Xc6slx45, package as csg324 with speed grade -3. The RTL schematic of 16 bit Braun multiplier with Row Bypassing using RCA and KSA is shown in below fig. 8, 9 and the simulation view of 16 bit Braun multiplier with Row Bypassing is shown in below fig 10.

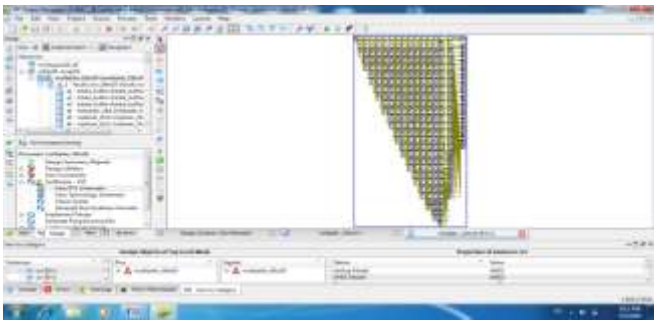

Fig8. RTL Schematic of 16 Bit Row Bypassing Multiplier with RCA

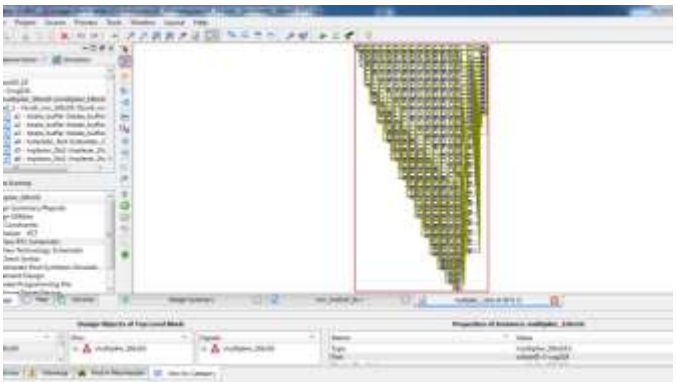

Fig9. RTL Schematic of 16 Bit Row Bypassing Multiplier with KSA

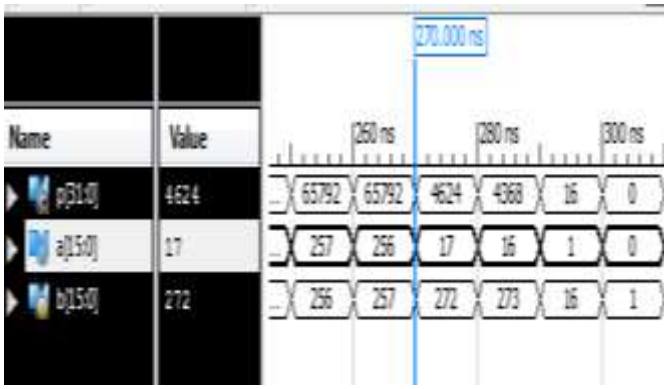

Fig10. Simulation result of 16 bit row bypassing multiplier with RCA and KSA

The RTL schematic of 16 bit Braun multiplier with Column bypassing using RCA and KSA is shown in below fig. 11, 12 and the simulation result of 16 bit Braun multiplier with Column bypassing using RCA and KSA is shown in below fig. 13.

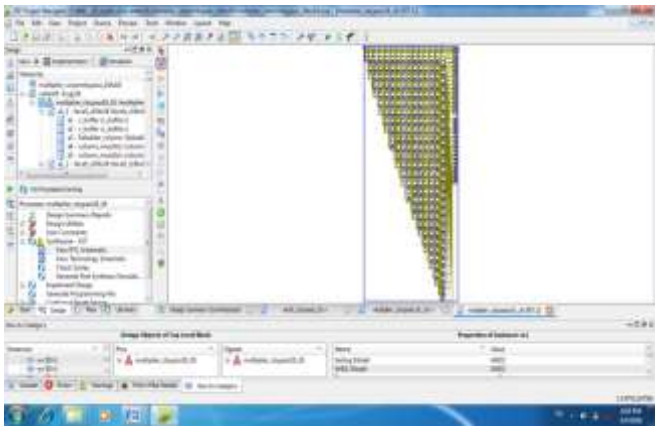

Fig11. RTL Schematic of 16 Bit Column Bypassing Based Braun Multiplier with RCA

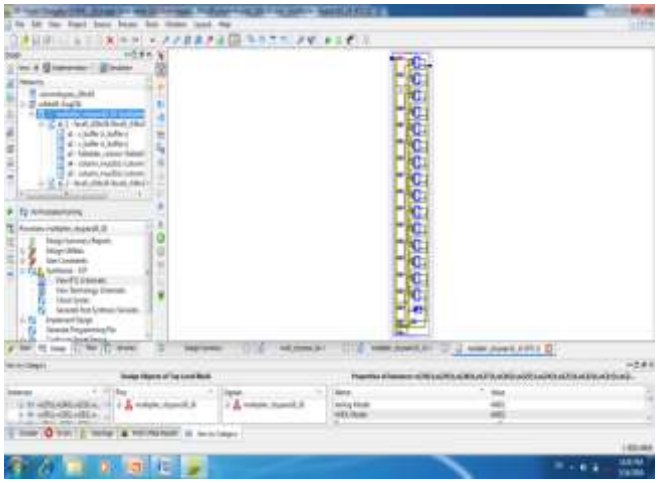

Fig12. RTL Schematic of 16 Bit Column Bypassing Based Braun Multiplier with KSA

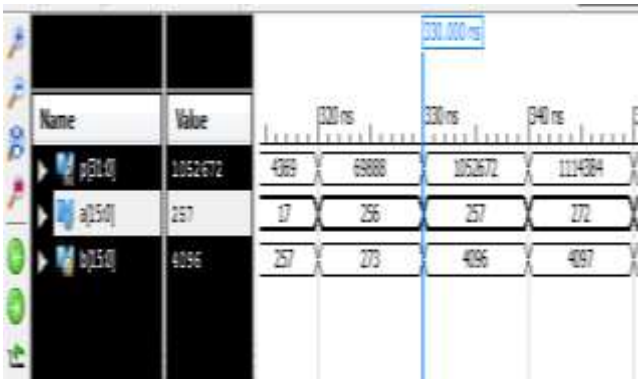

Fig13. Simulation Result of 16 Bit Column Bypassing Based Braun Multiplier with KSA

The RTL schematic of 16 bit Braun multiplier with Row and Column (mixed) bypassing using RCA and KSA is shown in below fig. 14, 15 and the simulation view of 16 bit Braun multiplier with Row and Column (mixed) bypassing using RCA and KSA is shown in below fig. 16.

Fig14. RTL Schematic of 16 Bit Row and Column Bypassing Based Braun multiplier with RCA

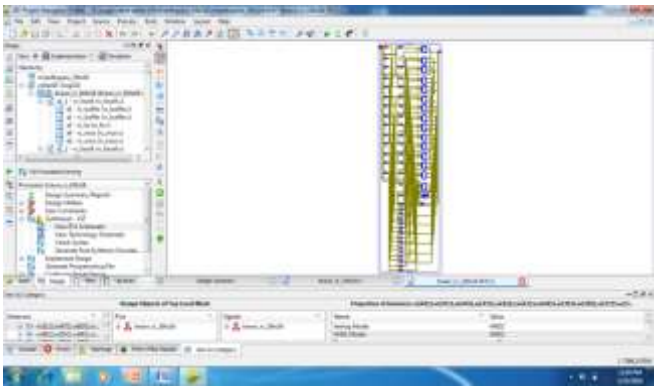

Fig15. RTL Schematic of 16 Bit Row and Column Bypassing Based Braun multiplier with KSA

Fig16. Simulation result of 16 bit Row and Column bypassing based Braun multiplier with RCA and KSA.

VIII. Comparison Table for All Bypassing Technique using RCA & KSA

Bit Length	Temp. / Adder	Power Consumption (in Watt)			
		10^0	25^0	50^0	75^0
4 bit row Bypass	RCA	0.039	0.058	0.090	0.156
	KSA	0.029	0.057	0.075	0.138
8 bit row Bypass	RCA	0.075	0.085	0.116	0.186
	KSA	0.029	0.039	0.069	0.137
16 bit row Bypass	RCA	0.087	0.095	0.130	0.200
	KSA	0.080	0.094	0.125	0.190
4 bit column Bypass	RCA	0.035	0.045	0.087	0.140
	KSA	0.028	0.055	0.068	0.135
8 bit column Bypass	RCA	0.069	0.059	0.110	0.127
	KSA	0.056	0.045	0.110	0.115
16 bitcolumn Bypass	RCA	0.085	0.087	0.123	0.187
	KSA	0.075	0.082	0.120	0.184
4 bit mixed Bypass	RCA	0.028	0.037	0.062	0.133
	KSA	0.026	0.034	0.060	0.128
8 bit mixed Bypass	RCA	0.045	0.043	0.110	0.137
	KSA	0.029	0.039	0.101	0.123
16 bit mixed Bypass	RCA	0.080	0.083	0.117	0.185
	KSA	0.073	0.082	0.114	0.184

IX. Conclusion

4/8/16 bit Row Bypassing, Column Bypassing and mixed (Row and Column) bypassing is implemented using RCA and KSA in Xilinx ISE 14.4 tool and it is simulated by using ISIM 14.4 simulator and both are compared. From the above comparison table it is concluded that for 4/8/16 bit Row, Column bypassing and mixed bypassing Braun multiplier less power is consumed using KSA when compared from RCA and hence speed can be improved. For 16 bit Row and Column Bypassing Technique using KSA the consumed power is found to 0.184 Watt. From other two methods (Row Bypass and Column Bypass) it is found to be 0.190 Watt and 0.184 Watt respectively

X. Future Work

In this paper 4*4, 8*8 and 16*16 bit multipliers are designed for unsigned bit multipliers. The bypassing techniques can also be applied to signed array multiplier architectures. It can also be implemented for the higher bit length like 32*32 and 64*64 bit in future. The design of multipliers considered here involved the use of RCA and KSA. The value of delay and power can also be reduced by using some other PPAs like BKA, SKA, LDA, and HCA etc.

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