Low Power Square Root Carry Select Adder

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Abstract: **Carry Select Adder (CSLA) is faster than any other adders used in many data-processing processors to perform arithmetic functions speedily. By observing the structure of the CSLA, it is clear that there is way for reducing the area and power consumption. This work uses an efficient gate-level modification to significantly reduce the area and power of the carry select adder. Conventional carry-select adder is still area-consuming due to the dual ripple carry adder structure. The logic operations involved in conventional carry select adder (CSLA) and binary to excess-1 converter BEC based CSLA are analyzed to study the data dependency and to identify minimized logic operations. The sum for each bit position in an elementary adder generated sequentially only after the previous bit position has been summed and a carry propagated into the next position. This paper introduces a proposed logic block as a D latch with replacing RCA block in conventional design to evaluate the power consumption and area. In order to minimize area and power of 16 bit carry select adder we have replaced a BEC with D latch.**

Keywords: power efficient, area efficient, CSLA, D-Latch. , etc…

I. INTRODUCTION

Adders have a special significance in VLSI designs and it is used in computer and many other processors. It is used to calculate addresses, table indices and similar applications. Adders are also used in multipliers, in high speed integrated circuits and in digital signal processing. Now a days design of low power and area efficient high speed data path logic systems are most substantial area in the research of VLSI design. Number of fast adders can be used for addition. In digital adders the sum of each bit position is added and the generated carry is propagated into the next position. The propagated carry reduces the speed of addition. The carry select adder can be used to alleviate this problem.

Carry Select adder designing involves ripple carry adder pairs which will work for summation either for Cin = 0 or and Cin = 1. Ripple carry adder is one of the adder which added three digit and reflects carry bit into next process. In conventional design two RCA's are used for summation for Cin = 0 and Cin =1 and final selection process will be carried out by multiplexer. Binary to Excess one converter is just the replacement of one RCA block for Cin = 1 in regular design because it gives added sum by considering Cin = 1. This paper describes the designing methodology of various fundamentals logic design simulation which helps in making the process running as in digital adder speed of addition is limited by propagation of carry through adder. Adders are an almost obligatory component of every contemporary integrated circuit. The prerequisite of the adder is that it is primarily fast and secondarily efficient in terms of power consumption and chip area. This paper presents the choice of selecting the adder topologies. The adder topology used in designing carry select adder work are ripple carry adder, binary to excess one converter and D-latch. Addition is an indispensable operation for any digital system, DSP or control system. Adders are also very significant component in digital systems because of their widespread use in other basic digital operations such as subtraction, multiplication and division. Hence, for improving the performance of the digital adder would extensively advance the execution of binary operations inside a circuit compromised of such blocks.

Ripple carry adder is the simplest but slowest adders with n operand size in bits. The carry-ripple adder is composed of many cascaded single-bit full-adders. As in initial conventional case each part of adder is composed of two carry ripple adders with cin_0 and cin_1, respectively. Through the multiplexer, we can select the correct output result according to the logic state of carry-in signal. The carry-select adder can compute faster because the current adder stage does not need to wait the previous stage's carry-out signal. Next we replace this ripple carry adder with BEC (Binary to Excess-1) converter in second terminology and in next one this BEC is also replace D latch as proposed here because latches are used to store one bit information.

II. LITERATURE SURVEY

Author Yajuan .He and et.al described an area efficient square root CSL scheme based on a new first zero detection logic. This carry-select adder partitions the adder into several groups, each of which performs two additions in parallel. Therefore, two copies of ripple-carry adder act as carry evaluation block per select stage. One copy evaluates

the carry chain assuming the block carry-in is zero, while the other assumes it to be one.

Author Ram Kumar et al. proposed a design which replaces a ripple carry block in conventional CSLA design with BEC-1 block named as binary to recess one converter. The main idea of this work is to use BEC instead of the RCA because with BEC-1 in order to reduce the area and power consumption is reduced than the regular CSLA. The idea is to use binary to excess one converter instead of RCA with carry is equal to one. The deficiency in this project that it will increase delay slightly greater than previous technique.

Paper by I-Chyn Wey, Cheng-Chen Ho, Yi-Sheng Lin, and Chien-Chang Peng proposed area efficient carry select adder by sharing the common boolean logic term. After boolean simplification, they can remove the duplicated adder cells in the conventional carry select adder. Alternatively, they generate duplicate carry-out and sum signal in each single bit adder cell.

The paper by Basant Kumar Mohanty and et.all proposed a new idea to made the performance of CSLA is fast instead with the use of BEC-1. They have designed a new logic formulation for CSLA. The carry select operation is scheduled before calculation of final sum which is different from conventional approach. They have used one RCA and one add one circuit instead of two RCA circuit. This method is known as sort of analysis because it divides main logic of operation into two parts first part gives half sum and carry calculation as it has done by HSC generator means half sum and carry generator and rest of the calculation part will be done by FSC (Full Carry Sum) generator . Therefore original sum and carry will be obtained by performing both this operation. There is consumption of quite large time to produced result sum.

III. METHODOLOGY

In this paper the basic approach is simply to design 16 bit carry select adder with D latch, which will minimized the power consumption as well as area in comparative with 16 bit carry select adder, here we refer as a base paper [12]. So here we have to make a comparative design study between BEC based CSLA and D latch based CSLA, as proposed. The involvement of blocks is as follows.

1. BINARY TO EXCESS ONE CONVERTER

The main advantage of this BEC logic comes from the lesser number of logic gates than the n-bit Full Adder (FA) structure. The logic diagram of BEC as follows.

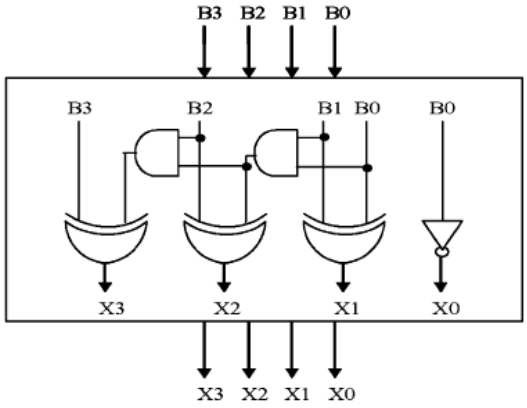

Fig1. 4-Bit Binary to Excess 1 Converter.

Truth Table:-

Binary logic B0,B1,B2,B3	Excess-1logic X0,X1,X2,X3
0000	0001
0001	0010
0010	0011
0011	0100
0100	0101
0101	0110
0110	0111
0111	1000
1000	1001
1001	1010
1010	1011
1011	1100
1100	1101
1101	1110
1110	1111
1111	0000

BEC consist of 4 inputs and the result is obtained by adding 1 with each of it. This logic is replaced in RCA with Cin=1. This logic can be implemented for different bits which are used in the modified design, here we refer as base papers [17] and [18].The main advantage of this BEC logic comes from the fact that it uses lesser number of logic gates than the n-bit Full Adder (FA) structure. The BEC structure has a feature that it can perform the similar operation as that of the replaced RCA with Cin=1.The basic work is to use Binary to Excess-1 Converter (BEC) in the regular CSLA to achieve lower area and increased speed of operation.

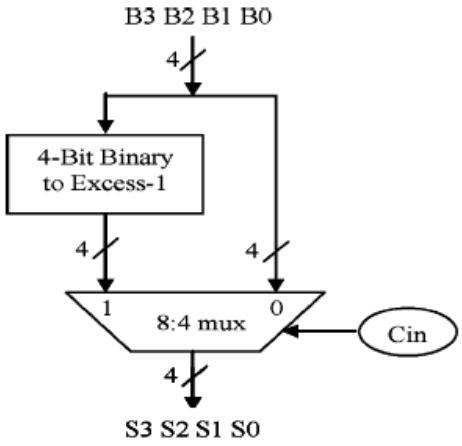

Fig2. 4 Bit Binary to excess-1 logic with 8:4 mux

Addition is achieved using BEC together with multiplexer as shown in figure 2 .If the select line of MUX is 0 then input is (B3,B2,B1 and B0) otherwise input is BECs output. Thus modified CSLA is designed such that it occupies less area and low power than regular CSLA. Also RCA is replaced with BEC.

2. CSLA USING BEC [BINARY TO EXCESS ONE]

The structure of 16 bit CSLA using BEC instead of RCA with Cin=1 to optimize the area and power is shown in Fig 3. One input to the multiplexer goes from the RCA with Cin=0 and other input from the BEC. It is clear that BEC structure reduces the area and power. But the disadvantage of BEC method is that the delay may increase slightly than the regular CSLA.

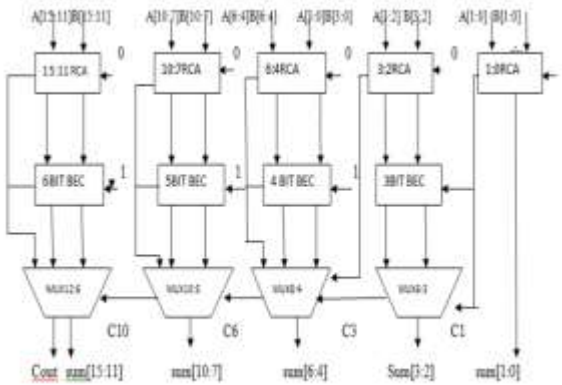

Fig3.Block diagram of CSLA using BEC

3. D LATCH TERMINOLOGY

To compensate power consumption in previous technology we are proposing a new technique with D latch. D latches are used for load and store operation because it will give output as one when clock is equal to one.

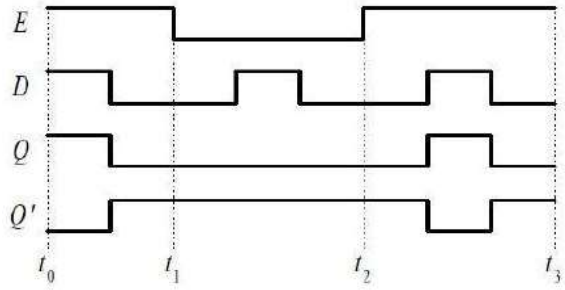

Fig4.waveform of D latch

Latches are used to store one bit information. The outputs are constantly affected by the inputs as long as the enable signal is asserted. In other words, when they are enabled, contents changes immediately according to the inputs. D-latch and it's waveforms are shown in Fig4.

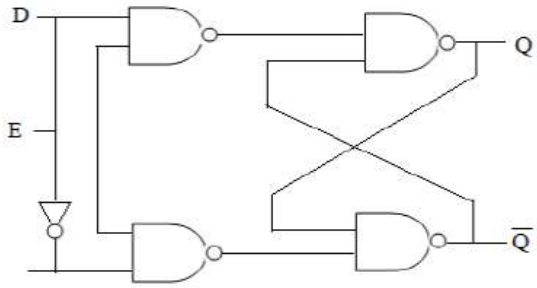

Fig5.Flip flop structure of D latch

4. CSLA USING D LATCH

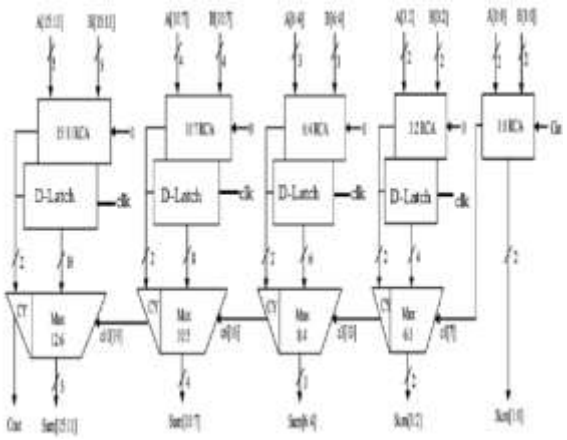

Fig6.Block diagram of CSLA using D Latch

This proposed architecture of 16 bit CSLA using D latch consists of five clusters of bit word size starting from n bit RCA and D latch later on 3b, 4b, 5b, 6b word size simultaneously .Instead of using two separate adders in regular CSLA, in this method only one adder is used to reduce area, power consumption and delay and each of two addition is performed in one clock cycle, here we refer as base papers [13] and [15]. In this 16-bit adder the LSB is ripple carry adder which is 2 bit. The upper half of adder i.e. MSB which is 14-b wide works on the principal of clock.

Whenever clock goes high the addition for carry input zero is performed and when clock goes low carry is assumed to be zero and addition is stored in adder itself. Carry out from the previous stage i.e., least significant bit adder is used as control signal for multiplexer to select final output carry and sum of the 16- bit adder. If the actual carry input is one, then computed sum and carry latch is accessed and for carry input zero MSB adder is accessed. Cout is the output carry.

IV. SIMULATION RESULT

This work is developed using Xilinx tool. The area-efficient carry select adder achieves an outstanding performance in power consumption. Power consumption can be greatly saved in our proposed area-efficient carry select adder because we only need XOR gate and as well as AND gate and OR gate in each carry-out operation. Modified SQRT CSLA has lesser number of logic gates and hence less area. The Xilinx ISE 9.2i software is used for synthesizing the adders, & Modelsim6.4a is used to compile & simulate to verify the VHDL code.

1. 16 BIT CSLA USING BEC

Fig 6. Output of Regular SQRT CSLA a (15:0) to i15

Fig7. Output of Regular SQRT CSLA i16 to d112

2. 16 BIT CSLA USING D LATCH

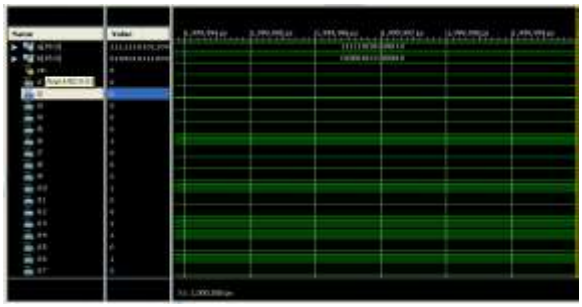

Fig 8.Output of Modified SQRT CSLA a (15:0) to i17

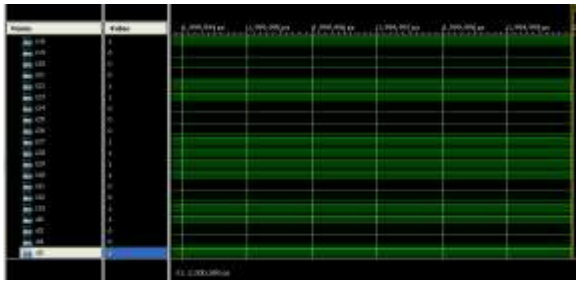

Fig 9. Output of Modified SQRT CSLA i18 to d5

V. COMPARISON TABLE

Table -1

Name	Delay [ns]	Power (UW)	Technology [nm]
conventional version [using BEC]	17.76	220	0.18
Modified Version [using D Latch]	24.57	160	65 To 90

All practical simulation results are shown in the table shows that practical simulation values of parameters with the help of software XILINX.

Table -2

Logic Utilization	No. of LUT	No. of slices	No. of IOB	Total
Regular version	60	33	50	143
Proposed Version	32	24	50	106

From the table we have concluded that the CSLA using D latch will give reduce power output than using CSLA using BEC. Here among two powers i.e. data power and I/O power we have reduce data power to great extent, but delay should be increased as number of logic blocks could get increased. Similarly area is also reduced as shown below but this area is the individual addition of (slices + lut's +I/O, s) as used in the design. Hence we cannot define in particular unit. Ratings should be changed for different FPGA technology if we consider implementation of this design yet it is not discussed here.

VI. CONCLUSION

An efficient approach was proposed in this project to reduce the area of SQRT Carry Select Adder and a comparison of the advancements in the features of SQRT CSLA was discussed. D-latch is a circuit which gives an output if status of clock is active else result won't get latched for next stage come after. By considering all circuit study it is concluded that proposed design will show the values of component parameter such as power and delay in reduced manner with earlier version as it is design methodology of BEC. The proposed design uses VHDL (Xilinx 12.1& 9.2i) module.

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