A High Speed Axi2ahb Interfacing Bridge Design for Amba Based SOC Architecture

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ABSTRACT- Microprocessor performance has improved rapidly these years. In contrast memory latencies and bandwidths have improved little We are using advanced microcontroller bus architecture with its advanced high performance bus. The Advanced Microcontroller Bus Architecture (AMBA) is a widely used interconnection standard for System on Chip (SoC) design. In order to support high-speed pipelined data transfers, AMBA supports a rich set of bus signals, making the analysis of AMBA-based embedded systems a challenging proposition. The goal of this work is to synthesize and simulate complex interface bridge between Advanced High performance Bus (AHB) and Advanced Peripheral Bus (APB) known as AHB2APB Bridge. To achieve high performance proposed architecture is FSM based pipelined APB-to-AHP Bridge and Vice-versa. This also involves the Back notation for Synthesized of Bridge module and to perform Functional and Timing Simulation using Xilinx ISE.

1. INTRODUCTION

Integrated circuits has entered the era of System-on-a-Chip(SoC), which refers to integrating all components of a computer or other electronic system into a single chip. It may contain digital, analog, mixed-signal, and often radio-frequency functions – all on a single chip substrate. With the increasing design size, IP is an inevitable choice for SoC design. And the widespread use of all kinds of IPs has changed the nature of the design flow, making On-Chip Buses (OCB) essential to the design. Of all OCBs existing in the market, the AMBA bus system is widely used as the de facto standard SoC bus. ARM announced availability of the AMBA 4.0 specifications. As the de facto standard SoC bus, AMBA bus is widely used in the high-performance SoC designs. The AMBA specification defines an on-chip

Communication standard for designing high-performance embedded microcontrollers. The AMBA 4.0 specification defines five buses/interfaces.

- Advanced extensible Interface (AXI)
- Advanced High-performance Bus (AHB)
- Advanced System Bus (ASB)
- Advanced Peripheral Bus (APB)
- Advanced Trace Bus (ATB)

AXI, the next generation of AMBA interface defined in the AMBA 4.0 specification, is targeted at high performance; high clock frequency system designs and includes features which make it very suitable for high speed sub-micrometer interconnection.

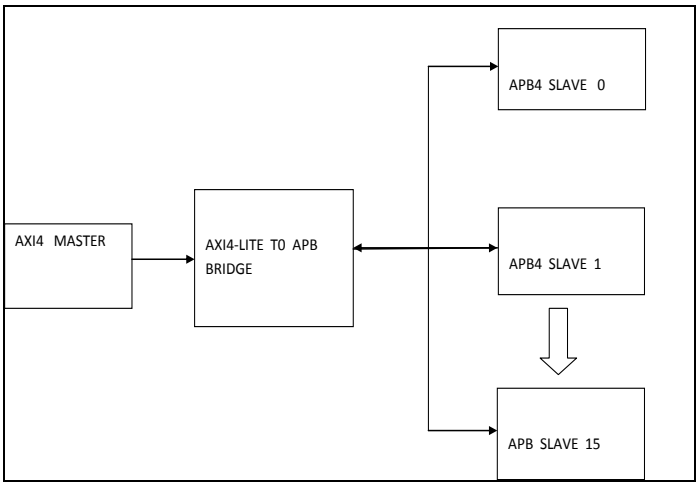


FIGURE1 BLOCK DIAGRAM

1.1 SIGNAL CONNECTION

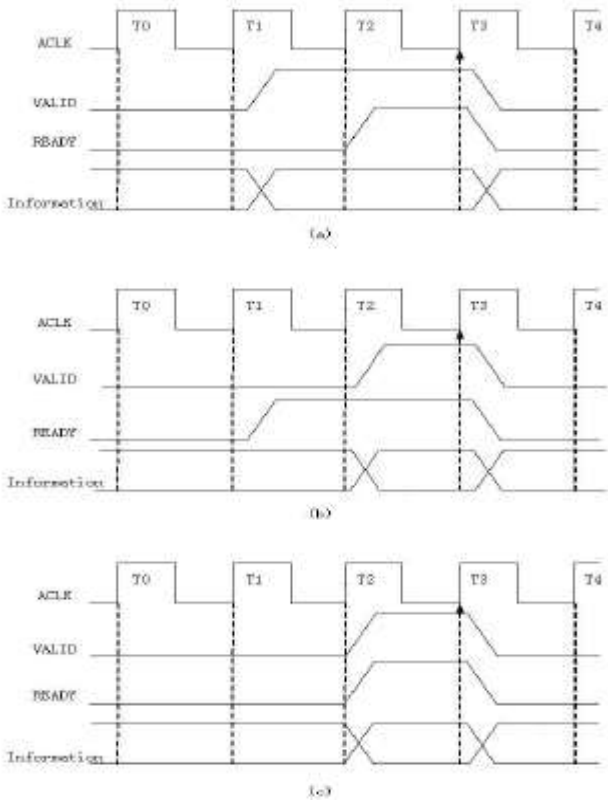
The bridge uses:

- AMBA AXI-Lite signals as described in the AMBA.
- AXI-Lite 4.0 protocol specification.
- AMBA APB signals as described in the AMBA APB.
- 4.0 protocol specification.

FIGURE 2-SIGNAL CONNECTION

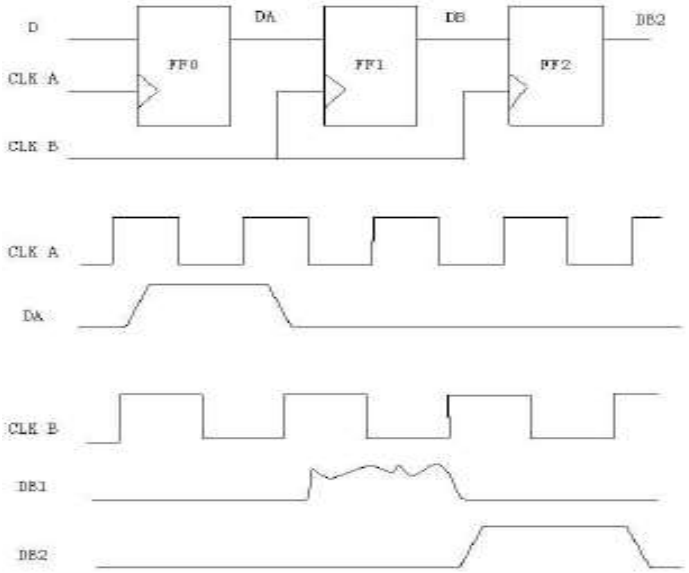
1.2 AXI HANDSHAKE MECHANISM

In AXI 4.0 specification, each channel hREADY signals for handshaking. The sour when the control information or data destination asserts READY when it can a information or data. Transfer occurs only VALID and READY is asserted. Cases of VALID/READ handshaking. Note asserts VALID, the corresponding control in must also be available at the same time. Indicate when the transfer occurs. A transfer the positive edge of clock. Therefore, the register input to sample the READY signal.



The APB bridge buffer addres,,control and data from AXI4-lite ,and drives the APB peripherals and returns data and response signal to the AXI4-lite.it decodes the address using an internal address map to select the peripherals.the bridge is designed to oprerate when the APB and AXI4-lite have independent clock frequency and phase.for every AXI channel,invalid commonds are not forwarded and an error response generated.thay is once and peripheral acess does not exists ,the APB bridge will generate DECERR as response through the response channel.(read or write).and if the target peripheral exists,but asserts PSLVERR, it will give a SLVERR response.

FIGURE 3-HANDSHAKE MECHANISM



2 .CLOCK DOMAIN CROSSING

A clock domain crossing (Cis) when a signal crosses from one clock to another. If a signal does not assert long may appear asynchronous on Metastability happens when setup/hold time window. Sync into a higher clocked domain registering the signal through a source domain, thus holding detected by the higher Synchronizing a signal travers in more cumbersome. This typical clock domain with a form of domain to the source domain, detected.

2.1 METASTABILITY

Metastability cannot be another metastable signal enabled sign. The metastability ousting the mean time between mtbf Where C1 and C2 are constant used to build the flip-flop metastable output, and fclk and synchronous clock and the asynchronous respectively.

$$MTBF = \frac{e^{C2*MET}}{C1*fclk*fdata}$$

2.2SYNCRONISER

Designers can use special metastable hardened flops for increasing the MTBF. Synchronizer flop is used following the signal DB. So, instead of the metastable signal DB being used in the function downstream. the stable signal DB2 is used in the logic downstream[8]. In the AXI4-Lite to APB bridge, we use synchronizer block designs for communicate between the AXI and APB clock domain.

FIGURE 4-TWO FLIP SYNCRONISER

3. FINITE STATE MACHINE

A finite state machine is a mathematical abstraction sometimes used to design digital logic or computer programs.It is a behavior model composed of a finite number of states, transitions between those states, and actions, similar to a flow graph in which one can inspect the way logic runs when certain conditions are met. The state transition diagram is a picture of our state machine model. Figure. 5 is the state transition diagram of our FSM.

The state machine operates through the following states:

- IDLE. This is the default state of the FSM. SETUP. When a write transfer request is asserted, the FSM moves into the SETUP state.
- SETUP. When a read transfer request is asserted, the FSM moves into the SETUP state.
- ENABLE. The enable signal, PENABLE, is asserted in the ENABLE state. READ_ACCESS. The enable signal, PENABLE, is asserted in the ENABLE state.
- HRESP. When the AXI read data channel is not ready for receiving signal RRESP, then stay in HRESP state. States HRESP and ENABLE are added, because the APB is not pipelined, wait states are added during transfers between the APB and AXI interface.

States HRESP and ENABLE are added, because the APB is not pipelined, wait states are added during transfers between the APB and AXI interface. System Verilog source code sample of the enumerated type encoded FSM is given below.

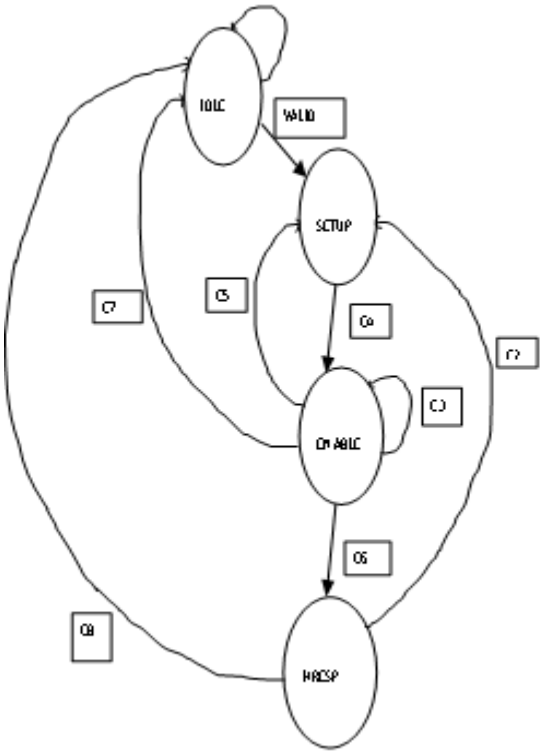


FIGURE 5-FSM STATE DIAGRAM

According AXI specification, the read the read address channel, write address channel and write data channel are completely independent. Each channel has a set of forward signals and a feedback signal for handshaking. A read and a write requests may be issued simultaneously AWVALID/WVALID and ARVALID are asserted high simultaneously) from AXI4-Lite, the AXI4-Lite to APB bridge will give

more priority to the read request than to the write request. That is, when both write and read requests are valid, the write request is initiated on APB after the read is requested on APB

4 SIMULATIONS AND IMPLEMENTATION

The timing diagram shown in Figure below. illustrates the AXI4-Lite to APB bridge operation for various read and write transfers It shows that when both read and write requests are active, read is given more priority.

FIGURE 6-TYPICAL READ AND WRITE TRANSFER

Before Static Timing Analysis (STA), it is necessary to inform the EDA tools that ACLK and PCLK are two asynchronous clock domains:

Area Report

Number of Slices	5	out of	768	0%
Number of Slice Flip Flops	3	out of	1536	0%
Number of 4 input LUTs	10	out of	1536	0%
Number of IOs	111			
Number of bonded IOBs	110	out of	140	78%
IOB Flip Flops	18			
Number of GCLKs	1	out of	4	25%

Timing report

Minimum period	5.928ns (Maximum Frequency: 168.691MHz)
Minimum input arrival time before clock	6.943ns
Maximum output required time after clock	10.702ns
Maximum combinational path delay	10.134ns

5. CONCLUSION

In this study, we provide an implementation of AXI4-Lite to APB bridge which has the following features:

- 32-bit AXI slave and APB master interfaces.
- PCLK clock domain completely independent of ACLK clock domain.
- support up to 16 APB peripherals.
- support the PREADY signal which translate to wait states on AXI.
- an error on any transfer results in SLVERR as the AXI read/write response.

6. REFERENCES

[1] ARM, "AMBA Protocol Specification 4.0", www.arm.com, 2010.
[2] Ying-Ze Liao, "System Design and Implementation of AXI Bus", National Chiao Tung University, October 2007.
[3] Clifford E. Cummings, "Coding And Scripting Techniques For FSM Designs With Synthesis-Optimized, Glitch-Free Outputs," SNUG (Synopsys Users Group Boston, MA 2000) Proceedings, September 2000.
[4] Clifford E. Cummings, "Synthesis and Scripting Techniques for Designing Multi-Asynchronous Clock Designs," SNUG 2001
[5] Chris Spear, "SystemVerilog for Verification, 2nd Edition"Springer,www.springeronline.com, 2008.
[6] Lahir, K., Raghunathan A., Lakshminarayana G., "LOTTERYBUS: anew high-performance communication architecture for system-on-chip deisgns," in Proceedings of Design Automation Conference, 2001.
[7] Sanghun Lee, Chanho Lee, Hyuk-Jae Lee, "A new multi-channel onchip-bus architecture for system-on-chips," in Proceedings of IEEE international SOC Conference, September 2004.
[8] Martino Ruggiero, Rederico Angiolini, Francesco Poletti, Davide Bertozzi, Luca 86
[9] Benini, Roberto Zafalon, "Scalability Analysis of Evolving SoCInterconnect Protocols," Int. Symposium on System-on-Chip, 2004. Lukai Cai, Daniel Gajski, "Transaction level modeling: an overview," in Proceedings of the 1st IEEE/ACM/IFIP international conference on Hardware/software codesign and system synthesis, October 2003.
[10] Min-Chi Tsai, "Smart Memory Controller Design for Video Applications," Master thesis: National Chiao Tung University, July 2006.

