Design and Implementation of Ripple Carry Adder

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***Abstract*— In this paper design of a 4-bit ripple carry adder is proposed using a novel CMOS 3T XNOR full adder cell. The number of transistors used in adder is less than conventional adder. The conventional full adder is compared with the ripple carry adder in terms of power and area. The design is implemented using Tanner schematic editor. The optimized layout of the ripple carry adder is designed using Tanner Layout Suite. A 3T XNOR gate cell is proposed which is used in 8T full adder. The proposed design remarkably reduces power consumption hence power-delay product (PDP) over various input voltages and frequencies, energy efficient applications. All simulations have been performed on 45nm standard model on Tanner EDA tool.**

***Keywords*—**

1. INTRODUCTION

Most of the VLSI applications, such as digital signal processing, image and video processing and microprocessors, extensively use arithmetic operations. Addition, subtraction, multiplication and multiply and accumulate (MAC) are examples of the most commonly used operations. The performance of the 1-bit full adder can be enhanced. Low power VLSI circuits by less transistor count have become important criteria for designing the energy efficient electronic circuits for high performance. The power-delay product or energy consumption per operation to indicate the optimal design tradeoffs is the better metric. In this paper a CMOS 3T XNOR full adder cell which offers faster operation and consumes less area and power than standard implementations of the full adder cell is presented. Generally ripple carry adders are used among all types of adders because of its compact design but it is the slowest adder. Here ,a design of ripple carry adder using full adder cell with 18 transistors. The paper is organized as follows: in section II, previous work is reviewed. Subsequently, in section III, the proposed design of ripple carry adder is presented. In section IV, the schematic and layout of the adders are presented. In section V, the simulation results are given and discussed. The comparison and evaluation for proposed and conventional designs are carried out. Finally a conclusion will be made in the last section.

2. EXISTING CIRCUIT

The structure of a general full adder has three inputs a, b, cin and two outputs sum and carry. The input signals a, b and cin will be added together logically [1], [3], [6], [7]. The output signals of the full-adder sum and carry can be expressed as in Eq. (1) and Eq. (2)

$$Cout = A.B + Cin(A + B) \text{ ------ } 1$$

$$SUM = Ci\bar{n}.(A \oplus B) + Cin(A \oplus B)$$

$$SUM = Cin \oplus (A \oplus B)$$

Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 1.Truth table for full adder

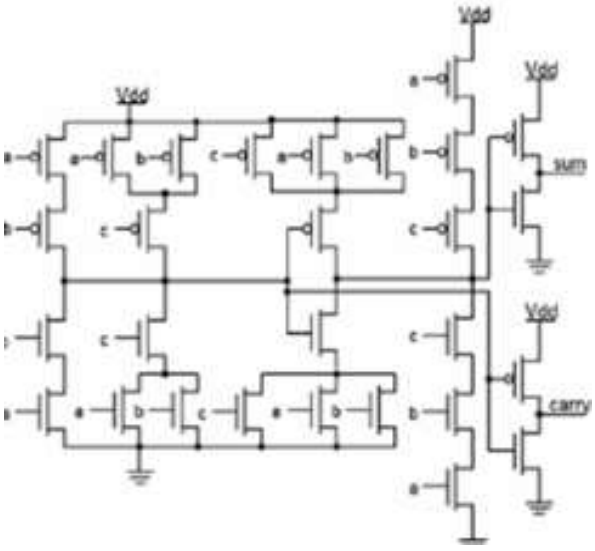

Fig 1. Conventional 28 T Full Adder

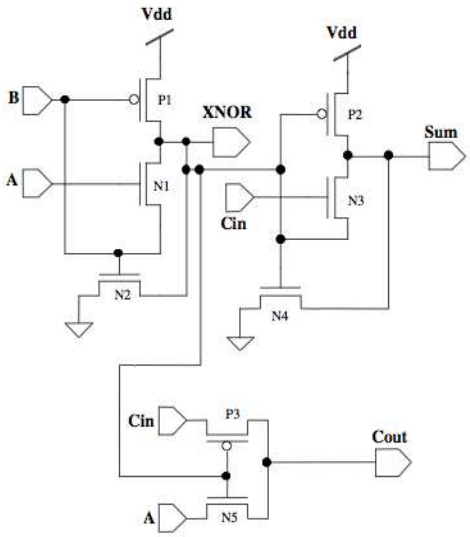

Fig 2 .Conventional 8T Full Adder

The existing full adder's ie full adder using 28T to 8T given above have its significance.

Ripple carry adder is built using multiple full adders such as the above discussed conventional full adder. In ripple carry adder each carry bit from a full adder "ripples" to the next full adder. The simple implementation of 4-bit ripple carry adder is shown below. C0 is the input carry, x0 through x3 and y0 through y3 represents two 4-bit input binary numbers.

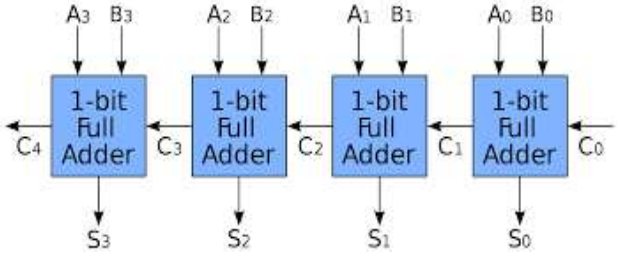

Fig 3. Ripple Carry Adder

3. PROPOSED 3T XNOR CELL

The proposed design of XNOR gate is shown in Figure 4.

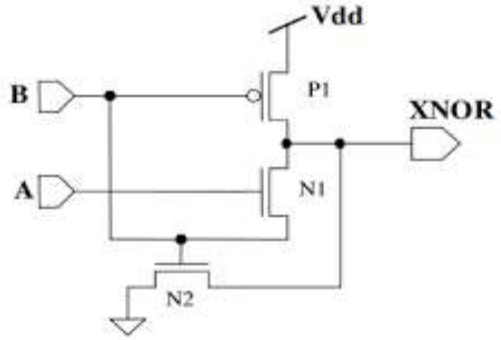

Fig 4 .Proposed 3T XNOR

There is a major degradation in output voltage that may lead to functional failure as well as increased power consumption for the remaining input vectors. For example, when ab=11, the first stage gives the degraded output. A complete logic '1' signal at the first stage and as nMOS is strong '0' device, it will pass compete '0'. This results in the degraded output at the first stage. As both nMOS M2 and M3 get enabled and try to transfer opposite signals on the first stage output result into voltage degradation. Similarly, for ab=10, transistor M1 and M2 get enabled and try to transfer opposite signals resulting into voltage degradation. This degraded output when given to the second XNOR stage, the output sum is further degraded. This leads to increase in power consumption as well as in PDP.

Operation of XNOR:

A	B	OFF	ON	OUTPUT
0	0	M2 (nMOS)	M1(Pmos)	1
0	1	M2 (nMOS)	M3(Nmos)	0
1	0		M2(Nmos),M1 pMOS	0.15
1	1		Both nMOS	1

4 .SCHEMATIC AND LAYOUT OF FULL ADDER

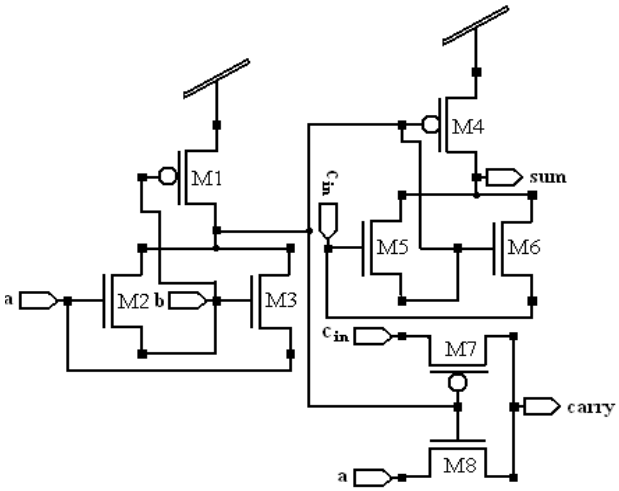

Fig 5. Proposed 8T Full Adder

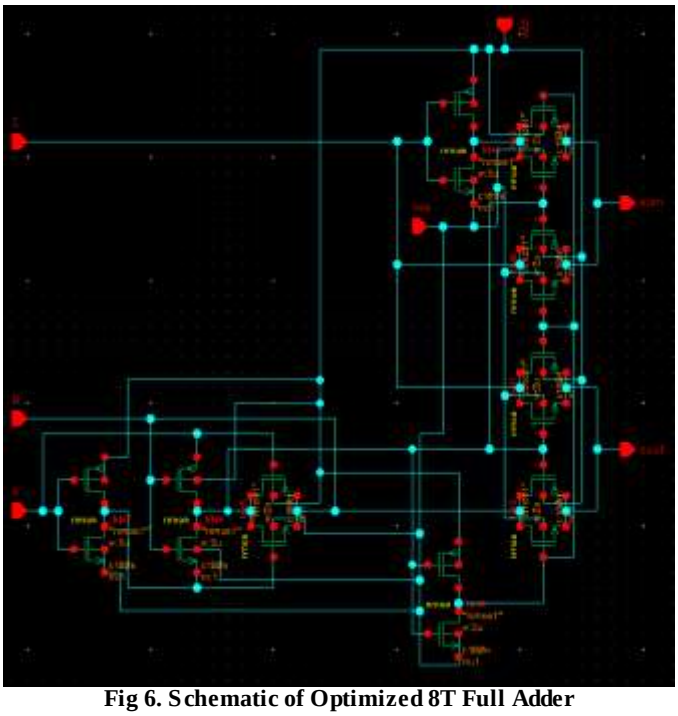

Fig 6. Schematic of Optimized 8T Full Adder

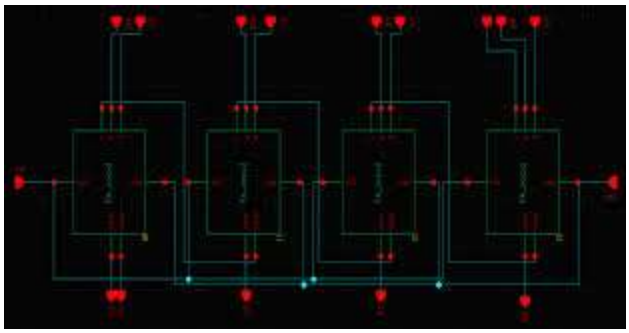

Fig 7. Schematic of Ripple Carry Adder Using Optimized 8T Full Adder

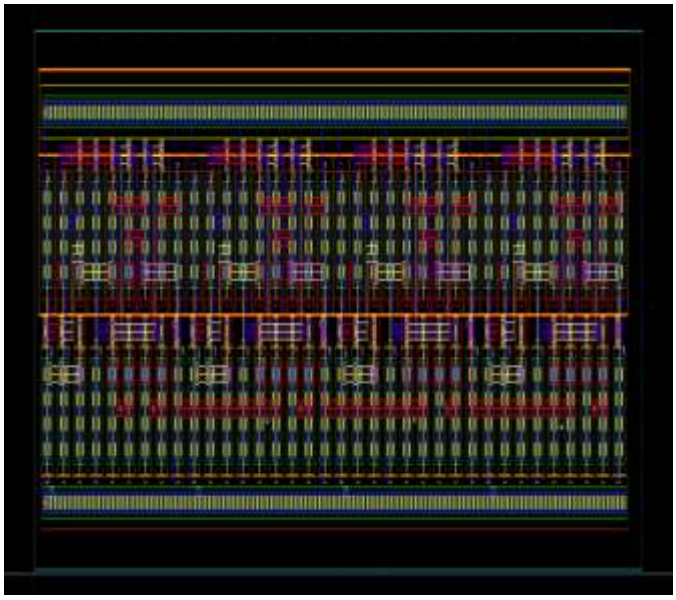

Fig 8 .Layout of Ripple Carry Adder Using Optimized Full Adder

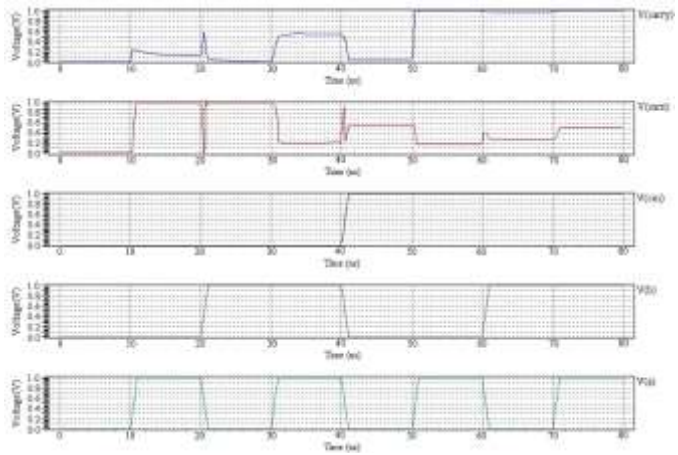

Fig 9. Input and output waveform

XNORing of the input 'a' and 'b' is the first step of output, using as selector is again XNORed with carry- in(Cin) to get sum.

Example:step I of output is 0 (cin=0):otherwise cin =1 carryout=input a.

5. COMPARISION OF ADDERS IN TERMS OF POWER

The existing different adders are compared in terms of power and transistor count ie the ripple carry adder is designed and implemented with proposed XNOR circuit shows low power consumption.

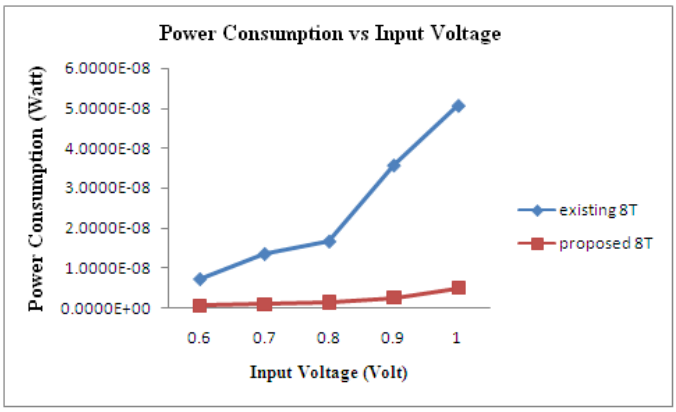

Fig 10. Power consumption vs input voltage of existing 8T and proposed 8T adder

Full adder	Power consumption
Ripple carry with 3T XOR	11.3 µw
Ripple carry adder conventional method	4.32µw
Ripple carry adder using TG	3.52 µw
Ripple carry adder using proposed XNOR	3.2 µw

6 .CONCLUSION

In this paper different ripple carry adders have been implemented, simulated, analyzed and compared. A novel full adder designed using 3T XNOR is presented in this paper that targets low transistor count and area. And it is extended to ripple carry adder whose characteristics of the adder circuit are compared against conventional complementary CMOS full adder based on the transistor count and delay. The optimized layout is drawn for the proposed full adder cell and the ripple carry adder in tanner tool .Thus we have implemented a ripple carry adder which is optimized in terms of transistor count and area and is more efficient than the conventional one.

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