Modified DMC based Enhanced Memory Reliability against MCUs

Vandna Gohar[#1], Kamal Niwaria[*2]
[#] *Department of Electronics Engineering, RKDF-IST, RGTU*
Hoshangabad Road, Bhopal, India
[1]*vandnagohar@gmail.com*
2kamalniwaria@gmail.com

***Abstract*— Nowadays, an increase in the application of semiconductor memories has made it possible to port a huge amount of data within a small space due to the advanced semiconductor memory manufacturing technology. On the other end, an increasing use of wireless application devices has increased the amount of energy radiations in the global environment. When a sufficient amount of energy waves strike with the electrons of the semiconductor surface, they might cause a change in the conducting state of the semiconductor switching elements. Also, an effect of these transient energy particles may cause an upset in the information present in the semiconductor memory. When the application of the semiconductor device is critically linked to any loss then such upsets are required to be avoided by a suitable method. Many packaging techniques are available that effectively protect the memory data from low energy radiations and transients. However, a particular packaging provides protection from an specific or a limited variations caused by the radiations. This paper focus on the FPGA based design and simulation of Decimal Matrix Code (DMC) that can correct all single-bit and sets of multiple bit errors that might occur in semiconductor memories due to high energy environmental radiations.**

***Keywords*— Decimal Addition, Binary Comparator, Error Detection and Correction, Multiple Cell Upsets, Memory Error Correction Codes, Syndrome.**

I. INTRODUCTION

Increasing applications of semiconductor memories in modern electronic application gadgets has resulted in storage of a huge data in personal gadgets. In the presence of high energy radiations that are present in environment this data might get affected causing single or multiple cell upset. Example in Fig. 1 shows an example of variation caused in the value of the data stored in memory due to environmental radiation with the help of a block diagram. With the increasing wireless applications the energy contents of the environment has also shown a growth. This has highlighted the requirement of error detection and correction of memory error detection and correction. Most of the data that is stored in memory is recoverable with the help of advanced software resources. But, in the cases where data from memory is required as secured information in which faults are intolerable then a resource is always preferred to recover the faults. In such systems the stored data Most of the methods that are available for securing or authenticating the stored data used the concept of adding redundant data to the actual data before storing the data in to the memory.

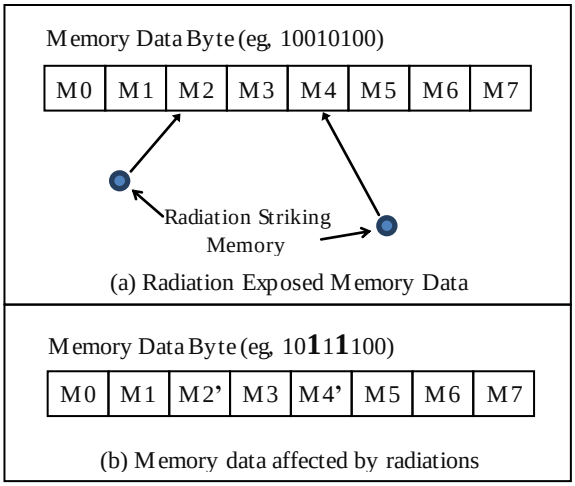

Fig.. 1 Error caused in Semiconductor Memory due to exposure to Energy Radiation

In [1] a novel per-word DMC was proposed to guarantee the dependability of memory. This is achieved by utilizing decimal algorithm to detect errors so that more than one error can be detected and corrected by the design implementation. An alternative approach to overcome the reliability issue of radiation is presented in [2] to give a comparative study of various error correction codes. In [3, 4] a hamming code based new technique for the correction of errors is implemented for a highly reliable decimal code. A mechanism derived From Orthogonal Latin Square Codes for single, double and triple-adjacent error detection and correction using hamming code is proposed in [5]. In [6] a CAM data protection scheme using DMC is proposed. For error correction [7, 8] presents the implementation of decimal matrix code and parity matrix. A memory data synthesis results against multiple bit error is shown in [7, 8]. In 2-D arranged memory data Carry Save Adder (CSA) based decimal error detection and correction technique is implemented in [9]. A quality protection level against large MCUs in memory is shown in [10]. It is shown that this implementation gives an enhanced error detection technique using Hybrid Matrix Code (HMC). An analysis showing better performance of DMC against Hamming code in implementation of decimal matrix code technique is performed in [11, 12, 13]. In [14] DMC architecture to correct

upto 5-bit errors is proposed. For memory data error correction with high reliability an implementation of DMC and HMC are performed in [15-16]. An Encoder Reuse Technique (ERT) based architecture implementation of DMC is presented in [17-18]. These designs reduce the area of the proposed design with respect to the presented conventional design architecture.

The rest of this paper is arranged as follows: Section-II presents the conventional and the proposed design of DMC Encoder and Decoder. The simulation and synthesis based results and comparative result analysis of the conventional and the proposed designs are given in section-III. Finally the conclusion based on the proposed work is discussed in section-IV.

II. DMC Proposed Design

The algorithm based block diagram of the conventional DMC encoder is shown in Fig. 2. This diagram represents the encoder output generation for a 32-bit data.

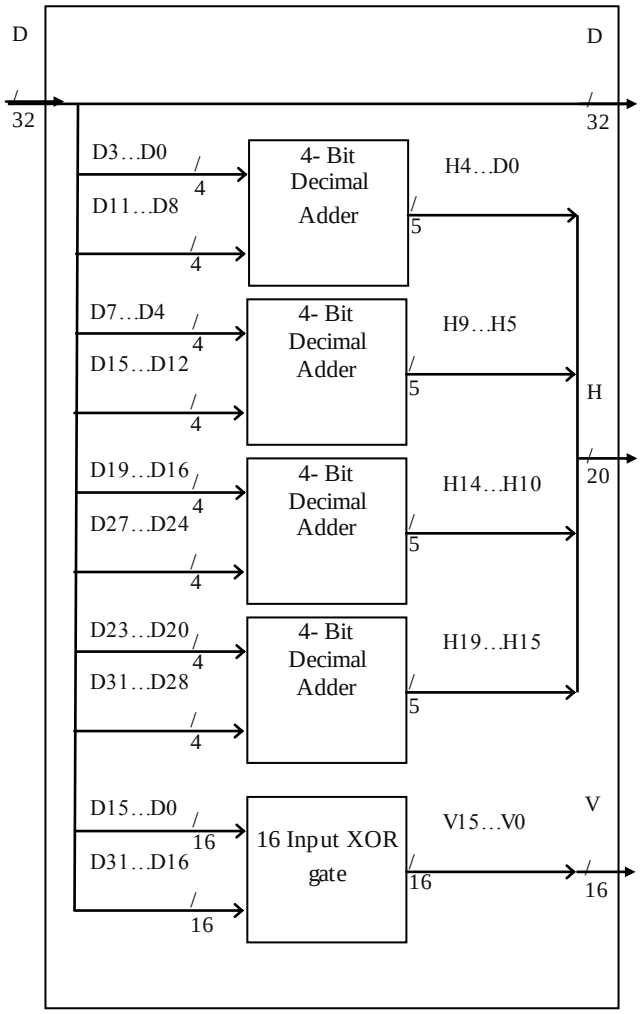

Fig.. 2 DMC Encoder Conventional Block Diagram

The corresponding decoder for the DMC design is represented and shown in Fig. 3.

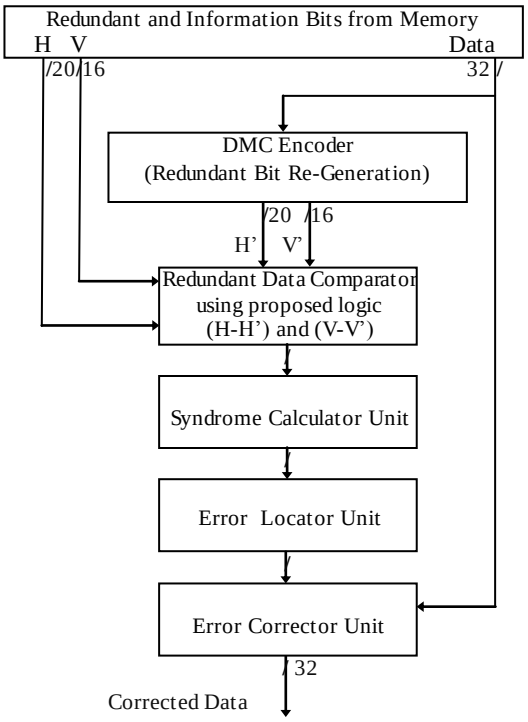

Fig.. 3 DMC Decoder Conventional Block Diagram

The conventional design of error syndrome generation unit utilizes decimal subtractor logic to generate the syndrome data. Fig. 4 shows the diagram of the conventional 5-bit subtractor logic.

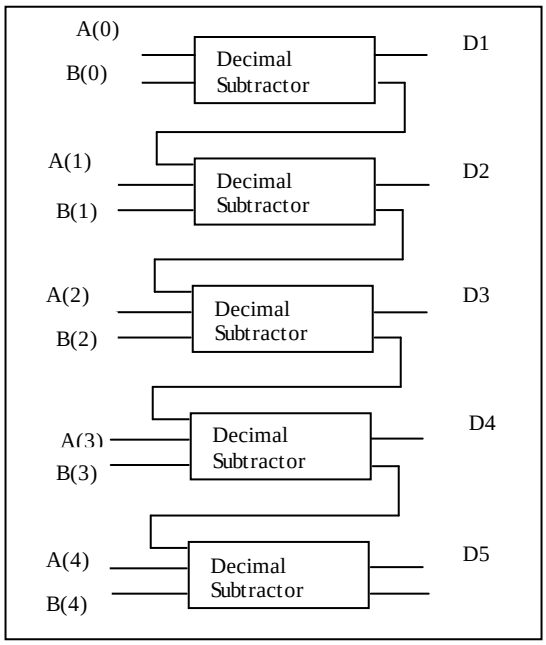

Fig.. 4 Conventional Subtractor design to calculate Syndrome

In the proposed work the syndrome bits are generated by using the bit-wise comparison logic that involves XOR-Gate.

The implemented logic equations for the generation of horizontal and vertical syndrome bits are shown as follows:

$$V_{syn} = V \text{ xor } V'$$
$$H_{syn} = H \text{ xor } H'$$

The Syndrome creation logic in the proposed work is shown in Fig. 5. For generating vertical syndrome 16 XOR gates and for generating horizontal syndrome 20 XOR gates are used.

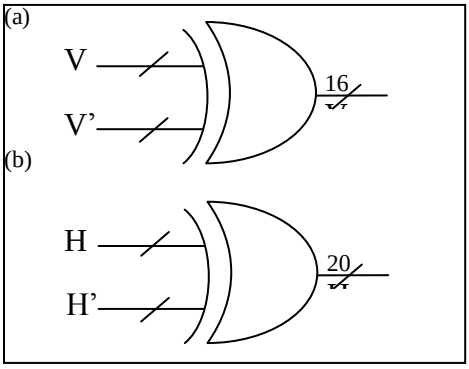

Fig. 5 Syndrome generation using proposed XOR-comparator (a) Vertical Syndrome, (b) Horizontal Syndrome

The horizontal and vertical syndrome bits, corresponding to each symbol, are grouped together. The grouped bits are shown in Fig. 6. All the grouped bits are ANDed to generate a single bit against syndrome bits of each symbol. These bits are used to locate the error from the data arranged in matrix. In the present work, 8 such bits are generated using horizontal and vertical syndrome bits. The concept of location of error symbol using these 8-bits by AND operation of bit combination in matrix architecture is shown in Fig. 7.

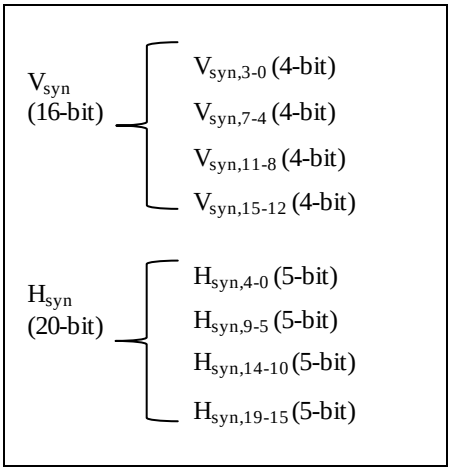

Fig. 6 Grouping of Syndrome Bit for Error Location

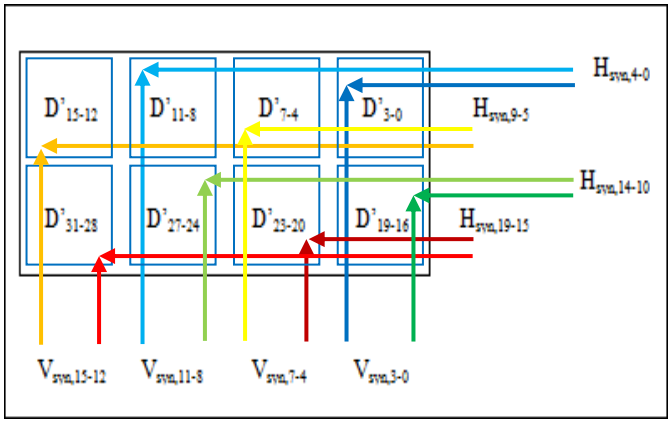

Fig. 7 Error location in the data using syndrome bits

There are total eight possible combinations of error locations. Each combination represents error in each of the data symbol in the memory. If the error identification in a symbol is not found, i.e., the AND operation of the error location bits is logic-'0', then the data in the memory is transferred to the output register without any bit change. The error identification will be followed by the inversion of error-bits using the vertical syndrome bits. The bit inversion is performed by using XOR operation which is shown in Table I. Bit inversion is performed only on those data symbol bits in which error is identified.

TABLE I
BIT INVERSION FOR ERROR CORRECTION IN SYMBOL USING XOR

Corrected Data		*Memory Data*		*Syndrome Data*
Sym-0_out	=	Sym-0	xor	$V_{syn,3-0}$
Sym-1_out	=	Sym-1	xor	$V_{syn,7-4}$
Sym-2_out	=	Sym-2	xor	$V_{syn,11-8}$
Sym-3_out	=	Sym-3	xor	$V_{syn,15-12}$
Sym-4_out	=	Sym-4	xor	$V_{syn,3-0}$
Sym-5_out	=	Sym-5	xor	$V_{syn,7-4}$
Sym-6_out	=	Sym-6	xor	$V_{syn,11-8}$
Sym-7_out	=	Sym-7	xor	$V_{syn,15-12}$

The corrected data is transferred to the output register for processing. Thus the soft errors in semiconductor memories get corrected by storing redundant bits with the data. The implementation of DMC is simple as compared to other error detection and correction techniques for semiconductor memory data. This technique also has a very less error decoding time. The main drawback of DMC technique is a high ratio of redundant bit to data bit.

III. SIMULATION AND SYNTHESIS RESULTS

The design and simulation in the proposed work is performed on Xilinx ISE Tool. Design description is performed on VHDL. The simulation of the designs is performed using Xilinx ISim by writing VHDL Testbench. The RTL schematic of the decoder design is shown in Fig. 8.

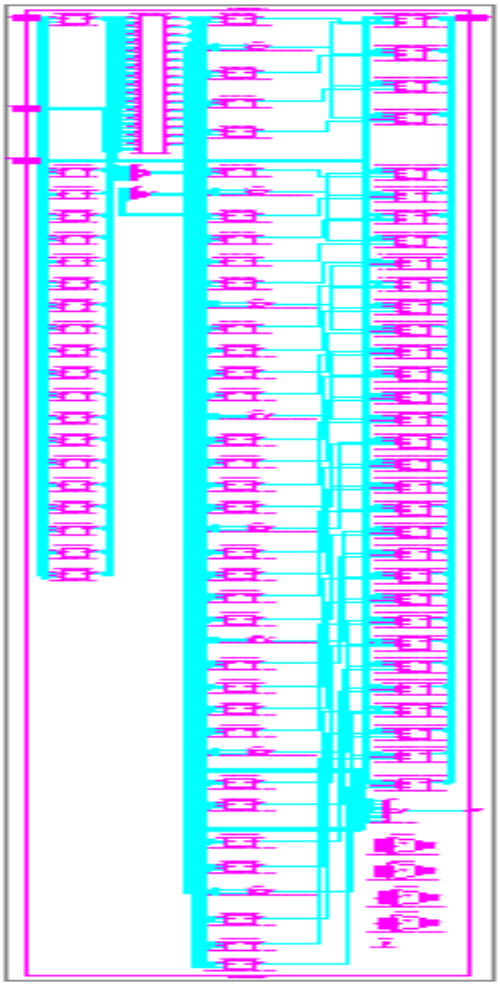

Fig. 8 RTL schematic of proposed decoder

The conventional design of 5-bit subtractor design (without carry-bit generation) is used in the conventional implementation of syndrome calculator in DMC decoder. Table II presents a comparison of the different gate count in conventional design and the proposed XOR based design of 5-bit comparator. The same is represented by a graph in Fig. 9.

TABLE III
BIT INVERSION FOR ERROR CORRECTION IN SYMBOL USING XOR

Gate Count in 5-bit comparator	*Ref[1]*	*Proposed Work*
XOR Gate	10	5
AND Gate	10	0
OR Gate	5	0
NOT Gate	10	0
Total Gate	35	5

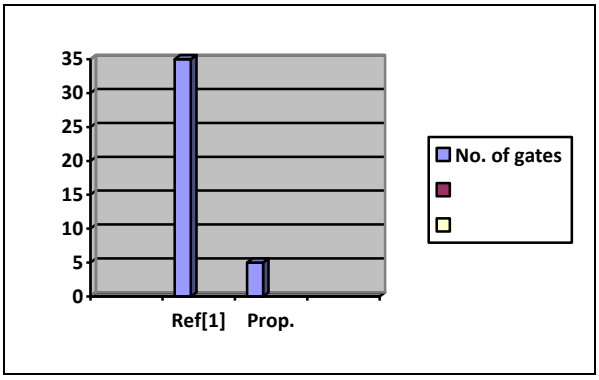

Fig. 9 Error location in the data using syndrome bits

The gate based comparative study shows that the proposed design requires less hardware resources and less area as compared to conventional design. Hardware utilization summary of the proposed designs of DMC based 32-bit encoder and decoder designs is shown in Table III.

TABLE IIIII
FPGA BASED HARDWARE UTILIZATION SUMMARY OF PROPOSED DESIGN

Spartan-3E XC3S500E-4PQ208	*Total*	*32-bit DMC Encoder*		*32-bit DMC Decoder*	
		Used	*%*	*Used*	*%*
Slices	4656	26	0	70	0
LUTs 4-Inputs	9312	48	0	123	0
Bonded IOBs	158	100	63	101	63

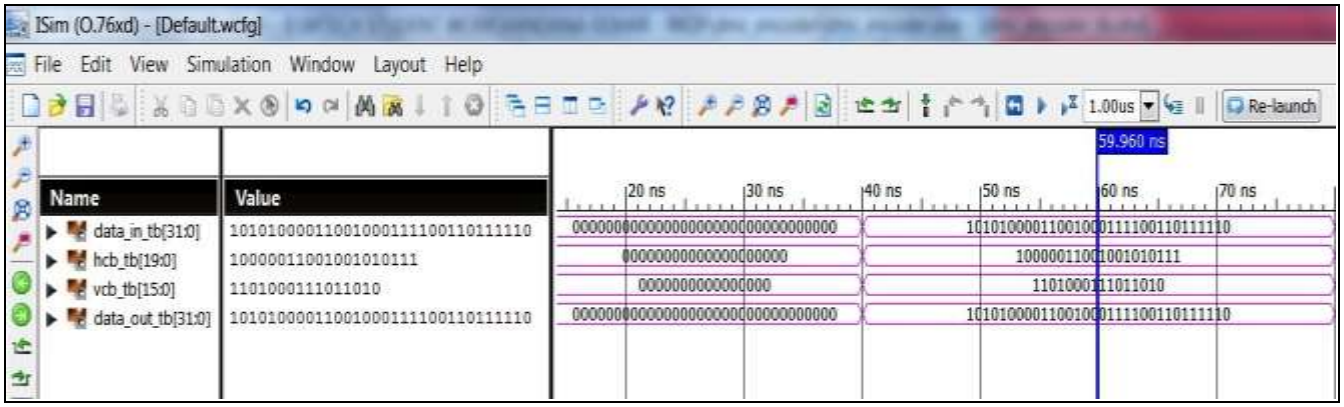

Fig. 10 Simulation Waveform of Proposed Encoder

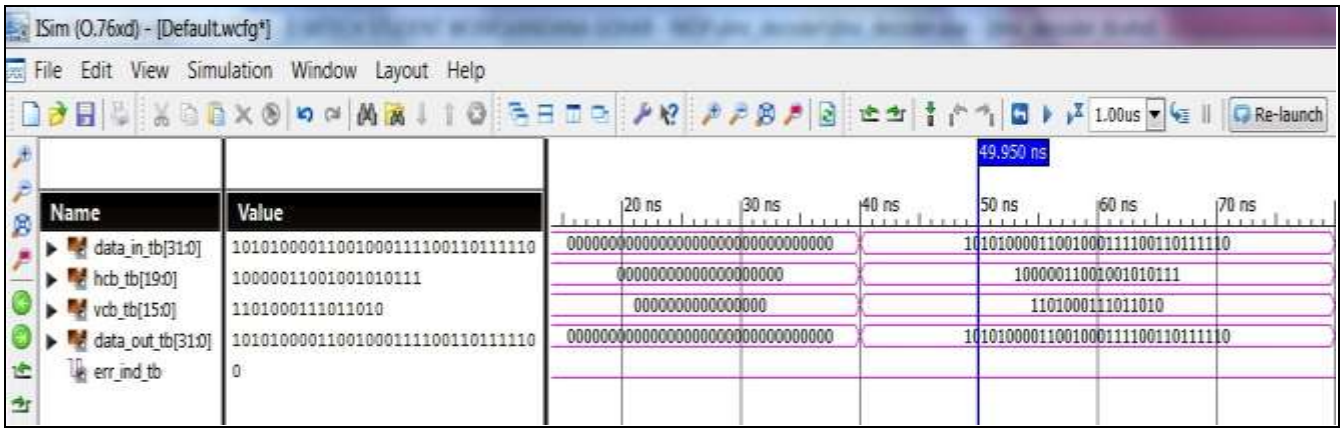

Fig. 11 Simulation Waveform of Proposed Decoder (without error in the data bits)

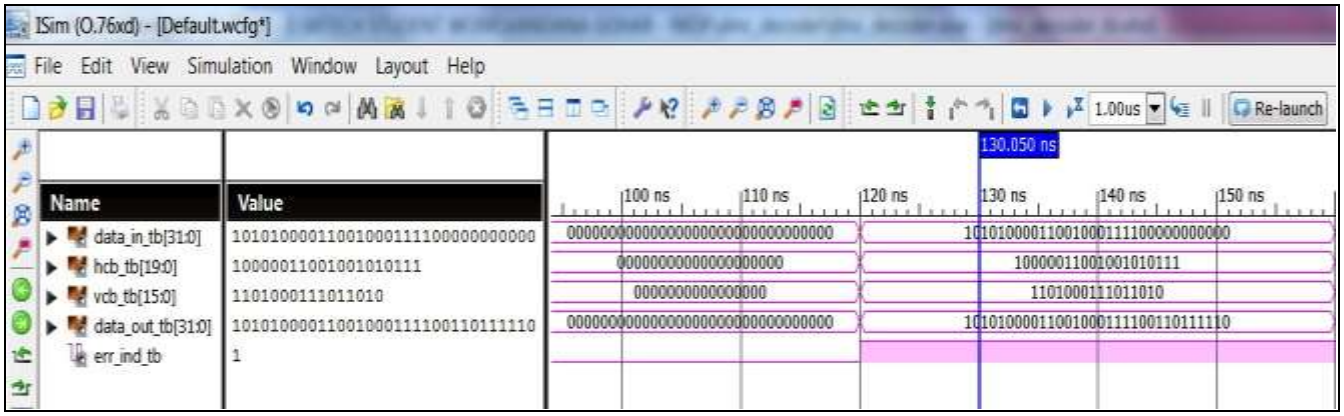

Fig. 12 Simulation Waveform of Proposed Decoder (with error detection and correction in the data bits)

The designs are simulated for a 32-bit data. The simulation waveform of proposed encoder is shown in Fig. 10. The output of the encoder are stored in memory. When the data is read from memory then it is given to decoder for data error detection. Fig. 11 shows the waveform of decoder simulation when there is no error in the stored data. Fig. 12 shows the decoder simulation waveform with error detection and correction in the stored data.

IV. CONCLUSIONS

The work performed in this work for the simulation of DMC encoder and decoder design is performed using XOR based comparator for Syndrome calculation. The use of logic reduced design in syndrome calculation leads to an optimized design implementation of DMC decoder. The replacement of the decimal subtractor by XOR based comparator is proposed in this work that shows the result in reduction in the area overhead of the decoder with respect to the conventional design.

ACKNOWLEDGMENT

The authors want to convey thank to Mr. Piyush Jain (Director, ITDT Center, Bhopal, India) for sharing his ideas in writing this paper.

REFERENCES

[1] Jing Guo, Liyi Xiao, Zhigang Mao and Qiang Zhao, "Enhanced Memory Reliability Against Multiple Cell Upsets Using Decimal Matrix Code", IEEE Transactions on Very Large Scale Integration Systems, Vol.22 No.1, pp.127-135, January 2014.

[2] David S, and Gayathree K., "A Comparative Study of Various Error Correction Codes", International Journal of Computer Science and Mobile Computing (IJCSMC), Vol.3 Issue 8, pp.196-200, August 2014.

[3] S. Kamalakannan, S. Karthikeyan and K. Sathyamoorthy, "Implementation of Error Correction Technique based on Decimal Matrix Code", International Journal of Advanced Research Trends in Engineering and Technology (IJARTET), Vol.2 Issue 4, pp.1-6, April 2015.

[4] K. Madhuri and V. Thrimurthulu, "Implementation of Decimal Matrix Code for correcting Cell Upsets in Static Random Access Memories", International Journal of Electrical, Electronics and Data Communication (IJEEDC), Vol.2 Issue 10, pp.72-76, October 2014.

[5] Sanilkumar N. S. and Aby Thomas, "Efficient Error Correcting Mechanism for Memories used in Radiated Environment", International Journal of Engineering Research and General Science (IJERGS), Vol.3 Issue 5, pp. 624-631, September-October 2015.

[6] Kavitha A. and Ramasathu L., "Fault Secure Memory using Modified Decimal Matrix Code", International Journal of Computer Science and Engineering Communications (IJCSEC), Vol.3 Issue 2, pp.829-834, 2015.

[7] Tintu B. Varghese and Ambika Sekhar, "Implementation of Decimal Matrix Code for Enhancing Memory Reliability", SSRG International Journal of Communication and Media Science (SSRJ-IJCMS), Vol.2 Issue 4, pp.1-5, July-August 2015.

[8] Neethu V. and Anju S. L., "A New Methodology for Error Detection and Correction to Realize Fault Tolerant Memory", International Journal of Science and Research (IJSR), pp.1689-1694, 2013.

[9] K. Janani and R. Ponni, "FPGA based protection of Soft Errors using Multiple Error Correction Codes", IJESC, January 2015.

[10] Maria Antony S. and Sunitha K., "Hybrid Matrix Codes for Enhanced Memory Reliability against Multiple Cell Upsets", International Journal for Scientific Research and Development (IJSRD), Vol.3 Issue 1, pp.114-117, January 2015.

[11] Sandeep M. D. and Rajashekhargouda C. Patil, "An approach to Reduce Number of Redundant Bits used to Overcome Cell Upsets in Memory using Decimal Matrix Code", ACEEE International Conference on Recent Trends in Signal Processing, Image Processing and VLSI (ICRTSIV), 2014.

[12] M. Sivasankaran and G. Renganayaki, "Improving Memory Reliability against Multiple Cell Upsets using Hamming based Matrix Code", International Journal of Innovative Science and Applied Engineering Research (IJISAER), Vol.13 Issue 44 Ver. 1, pp.38-43, March 2015.

[13] V. Vithya and P. Sakthivel, "Reducing Redundant Bits and Enhanced Memory Reliability using Decimal Matrix Code", International Journal of Electrical and Electronics Research (IJEER), Vol.3 Issue 3, pp.48-54, July-September 2015.

[14] E. Abinaya, D. Somasundareswari and S. Mathan Prasad, "Implementation of a Decimal Matrix Code for Correcting Multiple Cell Upsets in SRAM based FPGA Memories", International Journal of Advanced Research Trends in Engineering Technology (IJARTET), Vol.2 Special Issue 8, pp.87-93, 2015.

[15] Gayathree K. David S. and Moortheeswari M., "Reliability Enhancement using Parity Algorithm", International Journal of Innovative Science, Engineering and Technology (IJISET), Vol.2 Issue 4, pp.1176-1180, April 2015.

[16] Tarun Srivastava and Vipin Gupta, "Improved Performance of Memory Reliability against Multiple Cell Upsets using Hybrid Matrix Code", IJSET, 2015.

[17] E. Lavanya and J. Dhanapathi, "Detection of Multiple Cell Upsets in Memory for Enhanced Protection", International Journal of Innovative Trends and Emerging Technologies (IJITET), Vol.1 Special Issue 2, pp.129-132, March 2015.

[18] Gayathree K. and David S., "Analysing the Power Overhead of Decimal Matrix Code with Different Adder Architecture", International Journal of Research in Engineering and Advanced Technology (IJREAT), Vol.3 Issue 2, pp.126-132, April-May 2015.

