Design and analysis of varios adders using m.g.d.i. Technique

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Abstract: **Adders are significant component in digital systems because of their widespread use in other basic digital operations such as subtraction, multiplication and division. Hence, improving performance of the digital adder would extensively advance the execution of binary operations inside a circuit compromised of such blocks. In the present work, 8-bit adder topology like ripple carry adder(RCA), carry save adder(CSaA), carry look ahead adder(CLA) & carry increment adder(CIA) has been designed using the MGDI(Modified Gate Diffusion Input) technique. This technique gives better results in terms of power, delay and area when compared to the conventional CMOS technique. The simulation has been done at 65nm technology using DSCH tool and the layout has been designed using Microwind.**

I. INTRODUCTION

In past technology, the main concentrations of the VLSI designer were performance of the device, area required, cost and reliability of the complete system. Power dissipation was secondary issue. But in today's technology, the power dissipation is given equal weightage along with area and speed considerations. So many factors have been contributed to this trend. But the main driving factor is the remarkable success and growth of personal computing devices such as multimedia products, portable desktops and wireless communication systems like personal communicators which needs high- speed computation and complex functionality with low power consumption. In such applications, low power consumption is a critical design issue.

Power dissipation in CMOS circuits is caused by three main sources: 1) the charging and discharging of capacitive loads due to change in input logic levels. 2) the short-circuit current arises because of the direct current path between the supply rails during output transitions and 3) the leakage current which is determined by the fabrication technology, Addition is an indispensable operation for any digital system, DSP or control system. Therefore a fast and accurate operation of a digital system is greatly influenced by the performance of the resident adders.

In this paper, we designed four different low power, fast processing 8-bit adders using MGDI technique that has advantages of minimum transistors required, more speed and low power dissipation as compared to conventional CMOS techniques. The organization of this paper is as follows: Section II, explains the 4 adder topologies. Section III, explains MGDI technique and its performance analysis for basic digital gates. Section IV, presents the implementation the different adders using MGDI in DSCH 3.5 and MICROWIND Tool. At the end, the discussion and conclusion is presented in section V & VI.

II (a) IMPLEMENTATION OF RIPPLE CARRY ADDER (RCA):

The ripple carry adder is constructed by cascading full adders (FA) blocks in series. The carry out of one stage is fed directly to the carry-in of the next stage. Even though this is a simple adder and can be used to add unrestricted bit length numbers, it is however not very efficient when large bit numbers are used. One of the most serious drawbacks of this adder is that the delay increases linearly with the bit length. The advantages of the RCA are lower power consumption as well as compact layout giving smaller chip area. The design schematic of RCA is shown in Figure 1.

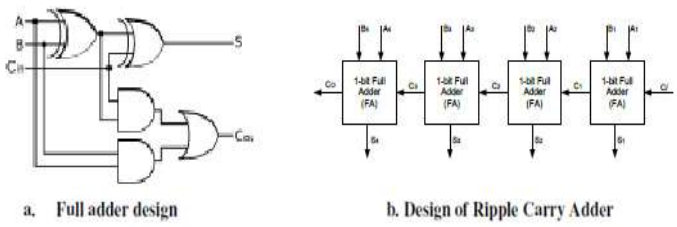


Figure1: Block diagram of Ripple Carry Adder (RCA)

II (b) IMPLEMENTATION OF CARRY SAVE ADDER (CSaA):

The Carry-Save Unit consists of n full adders, each of which computes a single sum and carries bit based solely on the corresponding bits of the three input numbers. The entire sum can then be computed by shifting the carry sequence left by one place and appending a 0 to the front (most significant bit) of the partial sum sequence and adding this sequence with RCA produces the resulting n + 1-bit value. This process can be continued indefinitely, adding an input for each stage of full adders, without any intermediate carry propagation.The design schematic of Carry Save Adder is shown in Figure2.

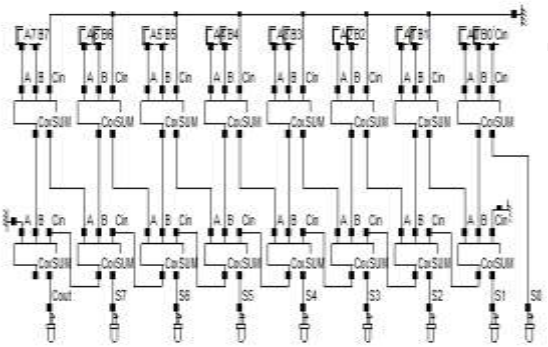


Figure2: Schematic of Carry Save Adder (CSaA)

II (c) IMPLEMENTATION OF CARRY LOOK AHEAD ADDER (CLA):

Carry look-ahead adder is designed to overcome the latency introduced by the rippling effect of the carry bits. The propagation delay occurred in the parallel adders can be eliminated by carry look ahead adder. The carry look ahead adder is based on the principle of predicting the carry bits. This adder reduces the carry delay by reducing the number of gates through which a carry signal must propagate.

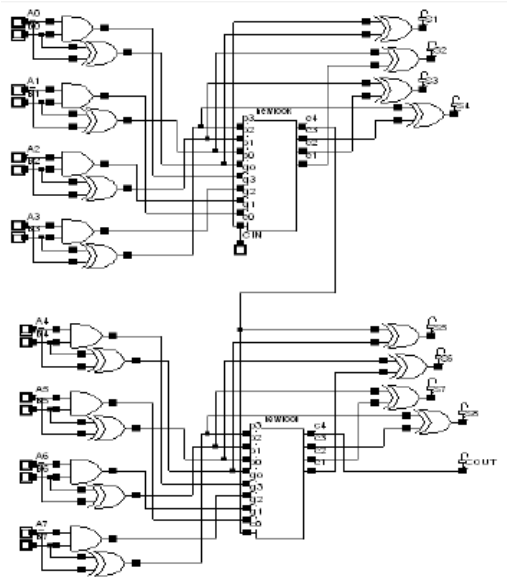


Figure3: Schematic of Carry Look Ahead Adder (CLA)

II (d) IMPLEMENTATION OF CARRY INCREMENT ADDER (CIA):

An 8-bit increment adder includes two RCA (Ripple carry adder) of four bit each. The first ripple carry adder adds a desired number of first 4-bit inputs generating a plurality of partitioned sum and partitioned carry. Now the carry out of the first block RCA is given to CIN of the conditional increment block. Thus the first four bit sum is directly taken from the ripple carry output. The second RCA block regardless of the first RCA output will carry out the addition operation and will give out results which are fed to the conditional increment block.

The input CIN to the second RCA block is given always low value. The conditional increment block consists of half adders Hence the output sum of the second RCA is taken through the carry increment block. The design schematic of Carry Increment Adder is shown in Figure4.

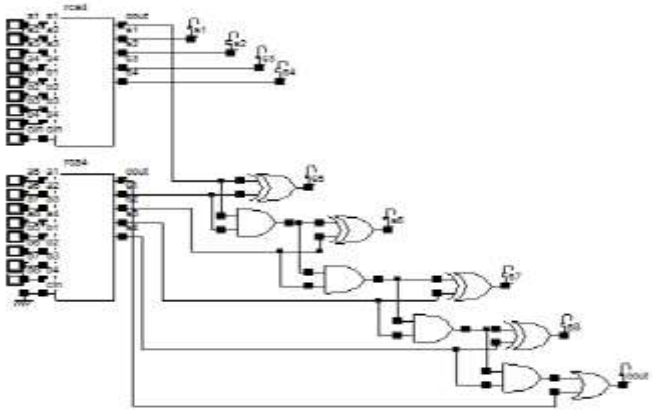


Figure4: Schematic of Carry Increment Adder (CIA)

III. MGDI LOGIC DESIGN TECHNIQUE

First the GDI basic cell was introduced by Arkadiy Morgenshtein in 2002 [5]. The basic GDI cell (figure 2) contains one nMOS and one pMOS transistors with four terminals: G, P, N and D. G is the common gate input of nMOS and pMOS transistors, P is the input to the outer diffusion node of pMOS, N is the input to the outer diffusion node of nMOS, and output D is the common output diffusion node of both transistors. The GDI primitive cells are designed in twin-well CMOS or silicon on insulator (SOI) technologies.

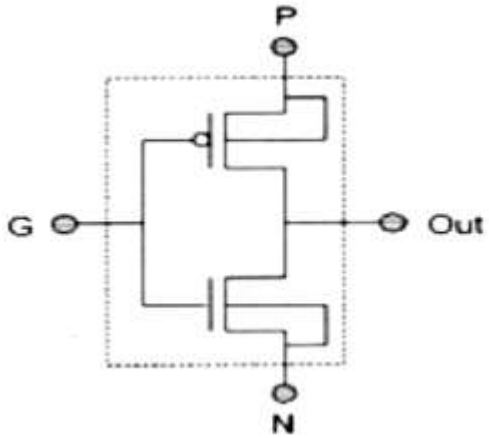


Figure5. Basic GDI cell

With few improvements in GDI technique, we have used MGDI cell for all basic gates with minimum power dissipation. Figure 3 shows the design of MGDI basic gates for inverter, 2 input AND, OR, NAND, NOR, and 3 transistor XOR gates. The operation of OR gate is described here. For OR gate, the source of pMOS is connected with input "B" and the source of nMOS is connected with input "A". The gate terminal G is connected with "A". When both the inputs are at low level then pMOS will operates in linear whereas nMOS is cut-off. When A is at high and B is at low level then pMOS is in linear region and nMOS is in linear region thereby producing the output as 1. Similarly for A at low level and B is at high level then pMOS is in linear and nMOS is also in linear region again producing the output as 1 Similarly when A and B both are at high level , then pMOS and nMOS are again in linear region thereby producing the output as 1.

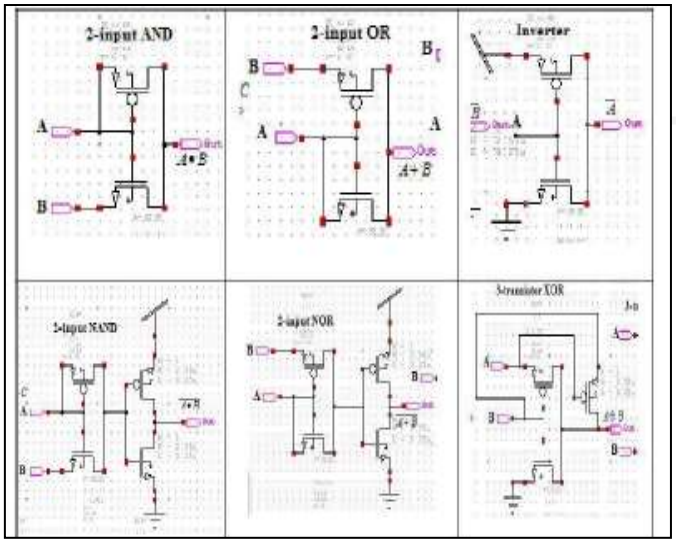


Figure6. Basic digital gates using MGDI technique

The comparative performance analysis [8] of MGDI, and CMOS logic is presented in Table 1. The comparative performance is done with respect to switching delay, transistor count and average power consumed by MGDI, and CMOS logic.

The Comparative Table No.1 shows that the MGDI performance is better when compared to CMOS logic. CMOS technique uses double number of transistor compare to MGDI to realize any digital gates. The transistors used to design XOR and XNOR has only three transistors in MGDI whereas CMOS logic uses eight transistors.

TABLE1.

S.No.	Primitive Cell	Switching Delay (ns)		Power Dissipation (mW)		Area (µm)		Transistors Used	
		CMOS	MGDI	CMOS	MGDI	CMOS	MGDI	CMOS	MGDI
1	2-INPUT AND GATE	0.04	0.025	0.079	0.0435	39.7	13.2	6	2
2	2 - INPUT OR GATE	0.05	0.025	0.078	0.016	42.6	13.2	6	2
3	INVERTER	0.025	0.025	0.077	0.077	12	12	2	2
4	2 - INPUT NAND GATE	0.025	0.035	0.089	0.0427	23.5	27.6	4	4
5	2 - INPUT NOR GATE	0.035	0.035	0.086	0.06625	25.5	27.6	4	4
6	2 - INPUT XOR GATE	0.055	0.025	0.059	0.0508	102.7	18.3	12	3
8	2:1 MULTIPLEXER	0.04	0.025	0.076	0.038	45.5	14.3	6	2

IV. IMPLEMENTATION OF ADDERS USING MGDI CELL

First Basic gates, Half Adder, Full Adder, 4-bit Ripple Carry Adder and 4-bit carry look ahead adder are designed using MGDI cell in MICROWIND & DSCH tools with 0.65µm technology with 1v supply voltage. The W/L ratio of both nMOS and pMOS transistors are taken as .3,0.5/0.07µmThe simulation of the adders has been done by considering the worst case scenario where one of the input is all set to 11111111 and Cin = 1 and the maximum delay has been considered for all analysis.The power dissipation of adder components are also measured for these input patterns and its average power has been reported.

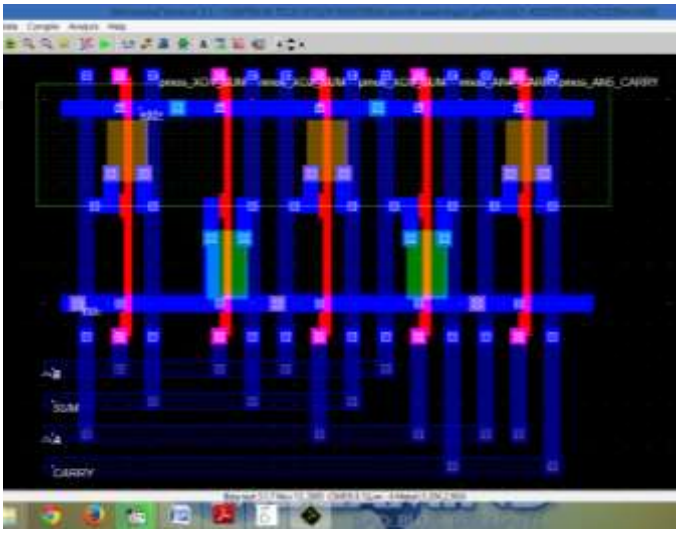


Figure 7: Layout of MGDI Half Adder

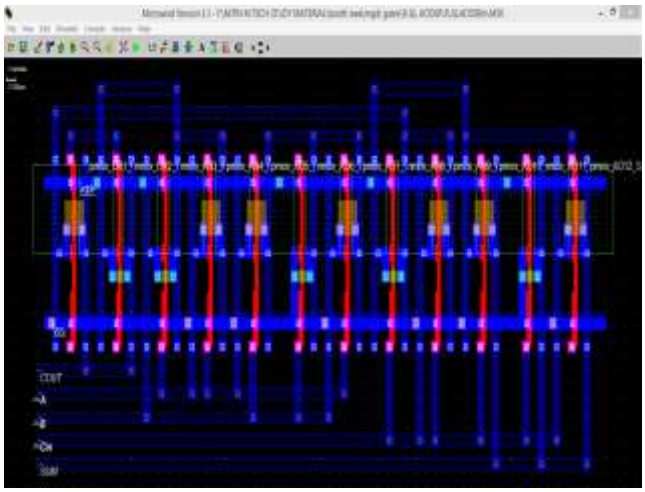
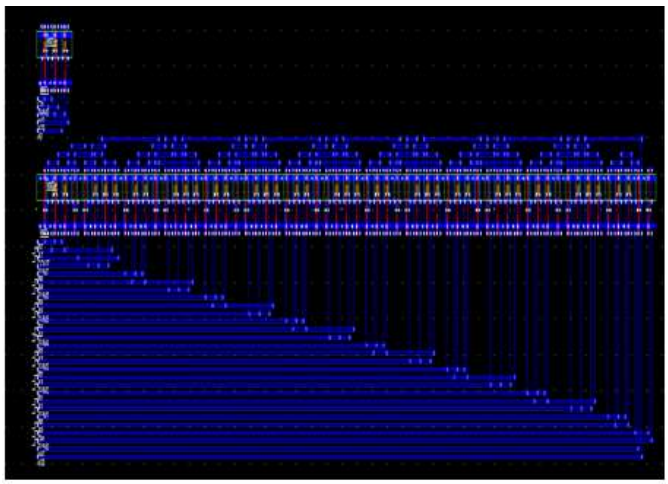


Figure 9: Layout of MGDI Ripple Carry Adder



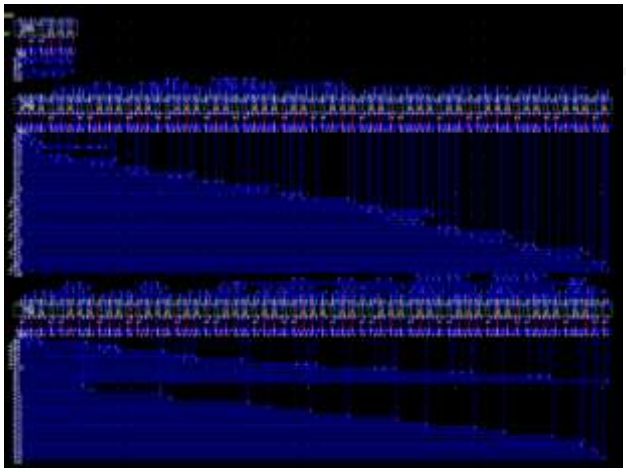


Figure 10: Layout of MGDI Carry Save Adder

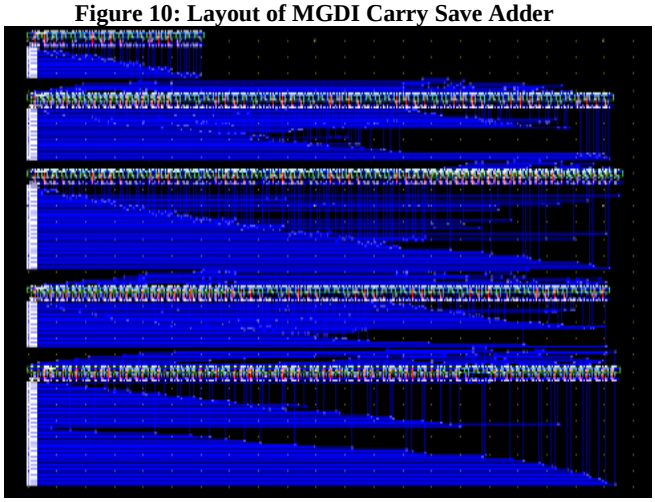


Figure 11: Layout of MGDI Carry Look Ahead Adder

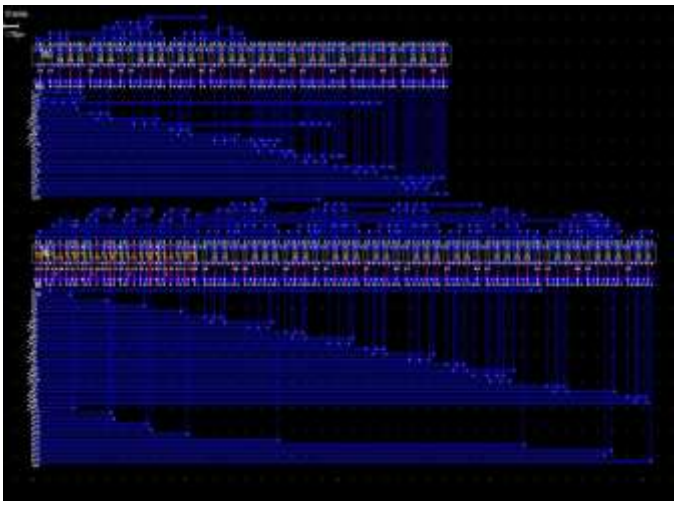


Figure 12: Layout of MGDI Carry Increment Adder

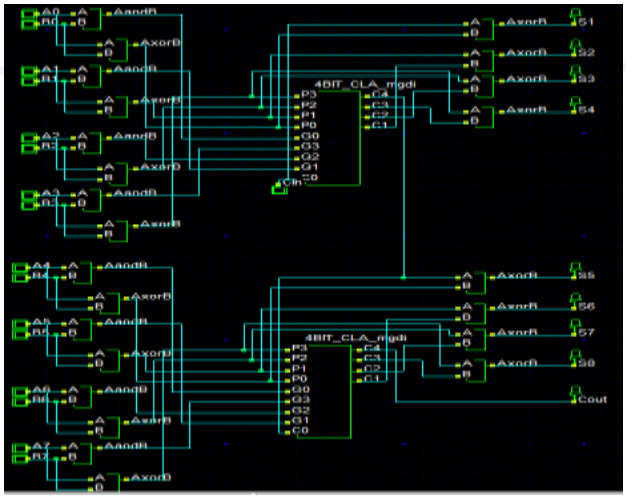


Figure 13: Schematic of MGDI Carry Look Ahead Adder

Figure 13, shows the schematic of Carry Look Ahead Adder and similarly, the schmatics of other three adders were designed and simulated using the DSCH.

V. SIMULATION RESULTS

The simulation results of the four different adders using the MGDI and CMOS techniques is shown in the tables below:

Table2. Analysis of Ripple Carry Adder

S.NO.	PARAMETERS	CMOS TECH.	MGDI TECH.
1	SWITCHING DELAY (ns)	0.355	0.14
2	VERILOG FILE SIZE (Lines)	290	119
3	NO. OF SYMBOLS USED	258	98
4	COMPILED CELLS	224	64
5	ROUTED WIRES	84	9
6	NO. OF NMOS TRANS. USED	112	24
7	NO. OF PMOS TRANS. USED	112	40
8	ELECTRICAL NODES COMPILED	154	52
9	AREA (μm^2)	31373	1495.3
10	TRANSISTORS USED	224	64

Table3. Analysis of Carry Save Adder

S.NO.	PARAMETERS	CMOS TECH.	MGDI TECH.
1	SWITCHING DELAY (ns)	0.42	0.175
2	VERILOG FILE SIZE (Lines)	528	186
3	NO. OF SYMBOLS USED	493	173
4	COMPILED CELLS	448	128
5	ROUTED WIRES	44	13
6	NO. OF NMOS TRANS. USED	224	48
7	NO. OF PMOS TRANS. USED	224	80
8	ELECTRICAL NODES COMPILED	311	94
9	AREA (μm^2)	6749.9	2836.3
10	TRANSISTORS USED	448	128

Table4. Analysis of Carry Look Ahead Adder

S.NO.	PARAMETERS	CMOS TECH.	MGDI TECH.
1	SWITCHING DELAY (ns)	0.47	0.245
2	VERILOG FILE SIZE (Lines)	673	275
3	NO. OF SYMBOLS USED	618	242
4	COMPILED CELLS	590	214
5	ROUTED WIRES	35	49
6	NO. OF NMOS TRANS. USED	449	264
7	NO. OF PMOS TRANS. USED	449	280
8	ELECTRICAL NODES COMPILED	713	471
9	AREA (μm^2)	116292	6943
10	TRANSISTORS USED	898	544

Table5. Analysis of Increment Adder

S.NO.	PARAMETERS	CMOS TECH.	MGDI TECH.
1	SWITCHING DELAY (ns)	0.395	0.145
2	VERILOG FILE SIZE (Lines)	390	151
3	NO. OF SYMBOLS USED	348	124
4	COMPILED CELLS	319	95
5	ROUTED WIRES	37	106
6	NO. OF NMOS TRANS. USED	178	60
7	NO. OF PMOS TRANS. USED	178	80
8	ELECTRICAL NODES COMPILED	259	107
9	AREA (μm^2)	5245.5	2301.3
10	TRANSISTORS USED	256	140

VI CONCLUSION

This paper has presented the architecture design, logic design and circuit implementation of 4 different adder topologie. The objective for Area, delay and power in adders was carried out for 8-bit addition using CMOS and MGDI techniques and Comparison with CMOS Technique is shown.The adders with MGDI technique gives less delay and less power dissipation with higher-speed of operation as compared to CMOS Technique.

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