The Keeper Design for Dynamic Logic Circuits Using Different Techniques

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Abstract—**The increasing variability in device leakage has made the design of keepers for wide OR structures a challenging task. The conventional feedback keepers (CONV) can no longer improve the performance of wide dynamic gates for the future technologies. In this paper, we propose an adaptive keeper technique called rate sensing keeper (RSK) that enables faster switching and tracks the variation across different process corners. The problems of contention current and process tracking have been two different paradigms in the design of dynamic logic circuits. The existing keeper techniques address one of them while sacrificing the other. However the proposed Rate Sensing Keeper technique provides reduced contention and better process tracking for a given noise robustness with less overhead in area, power and delay. The technique also allows for a larger pulldown width that can be used in complex register files. The design has been implemented using UMC 130nm Mixed Mode/RF CMOS Process in cadence Spectre RF Simulator.We show that the RSK technique gives superior performance compared to the other alternatives such as Conditional Keeper (CKP) and current mirror-based keeper (LCR).**

Index Terms—**Bias, keeper, process variation, rate sensing, wide OR.**

I. INTRODUCTION

IDE OR structures are typically used in the read path of register files, L1 caches, match lines of TCAMs, flash memories and PLAs. In most of the applications the worst case requirement would be to sense the difference between the leakage state where all the pulldown legs are leaky and the ON state where only one of the legs is ON. The increase in the variability and magnitude of the leakage current has become a major bottleneck in realizing such wide OR gates. Especially, in case of dynamic logic gates, the robustness of the dynamic node has to be guaranteed across different process corners without significant loss in the performance. For this purpose the dynamic gates use a feedback keeper to support the leakage at the dynamic node during the evaluation phase. However, the feedback keeper produces a large contention current during evaluation phase. Moreover the keeper being pMOS, it does not track the leakage currents in the pulldown nMOS logic for the fast-nMOS slow-pMOS (fNsP) and slow-nMOS fast-pMOS

(sNfP) corners. This results in performance degradation, higher short-circuit power dissipation and limits the number of pull down legs.Introduction

The need for high performance in the microprocessors has resulted in a number of logic families that trade off power and robustness for speed. Dynamic logic is one such logic family which offers the least logical effort for a given logic function. The advantage of dynamic logic is that it has less number of transistors and offers less capacitive load to the driving gate. This makes the dynamic logic an ideal choice for designing high performance functional units in a microprocessor where speed is the major design metric. This chapter gives a brief overview of dynamic gates and different keeper techniques that are used to achieve robustness.

II. DYNAMIC LOGIC GATE

The dynamic gates basically consist of NMOS logic transistors connected to a floating dynamic node and hence the name dynamic logic. The dynamic node is connected to VDD using a precharge PMOS transistor. The widely used form of dynamic gate is called as the Domino Logic which has an inverter at the output. The inverter ensures that the input to each domino gate is a monotonically rising signal.

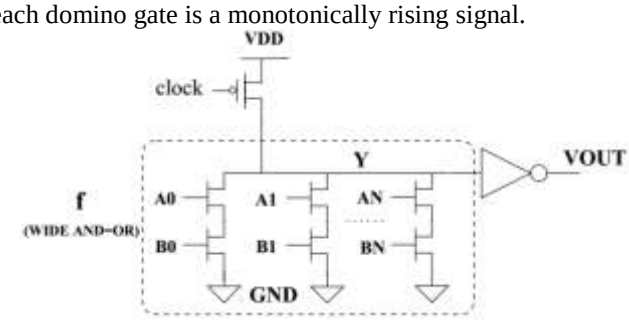

Figure 1: A wide AND-OR domino gate

Figure 1 represents a wide AND-OR domino logic dynamic gate with the precharge transistor and clock signal. The dynamic logic works on two clock phases. When the clock is low the voltage node Y gets charged to the supply voltage VDD through the pre-charge transistor. This phase of operation is called as the pre-charge cycle. By the end of the pre-charge cycle the data inputs (A0. . . AN and B0. . . BN) to the logic circuit will be ready at the input of the NMOS transistors. Now the CLK signal goes high turning the pre-charge transistor off. This phase of operation is called evaluation cycle. Now there are two possible scenarios.

Case 1: If there is no conducting path from the node Y to the GND i.e., when A0. . . AN=0 or B0. . . BN=0 or A0. . . AN, B0. . . BN = 0 then each of the parallel pull down leg remains OFF causing the node Y to remain at VDD. However in practical cases even when the gate input (A0. . . AN, B0. . . BN) of a transistor is zero there is a small leakage current through the transistor. This region of operation of the transistor is called the sub-threshold region. Because of this even when the pull down stack is off during the evaluation phase there is a small leakage current flowing through each of the parallel pull-down legs which causes the Y node to eventually go to zero after a certain period of time. Hence the logic value will be corrupted and will result in erroneous input to the subsequent stages. Also in practice the input voltage will not be perfectly zero at the gate inputs. They will have an additional noise voltage due to various non-idealities in the

chip. This will further add to the leakage of the dynamic node in the circuit.

Case 2: However if any one of the pull down legs are ON i.e. Ai = 1 and Bi =1 for any i = 1. . . N then there is a conducting path from Y to the GND resulting in the discharge of Y node. This will result in the node VOUT to go to VDD and the subsequent stages will get the correct input.

III. KEEPER DESIGN

Now of the above two cases described in the previous section, discharging due to case 1 is not desired while that due to case 2 is desired. To circumvent this, a keeper PMOS transistor (M1) is introduced between the Y and VDD nodes. The functioning of this keeper should be such that it should minimize or compensate for the discharging in scenario 1 without affecting the discharging due to case 2. Suppose if the discharging current in scenario 1 is Ileak and that during case 2 is Ion, an ideal keeper should provide the current Ileak during case 1 and zero current during case 2. If the keeper does not supply the required current during case 1 then the Y node voltage will be less than VDD, which in turn will corrupt the node VOUT. Also if the keeper supplies some current during case 2 then it will contend with the pull down logic and might slow down the discharge process. The ability of the keeper to keep the Y node close to VDD during case 1 determines its noise robustness. The amount of current that the keeper produces during scenario 2 determines its contention with the pull-down logic. Thus any keeper design should try to achieve a good tradeoff between speed and robustness.

The following section will give a brief overview of the various keeper techniques that exist in literature.

IV. EXISTING KEEPER TECHNIQUES

The dynamic gates designed in the present day technology demand very stringent keeper design to achieve high performance and robustness. The keeper is expected to have minimum contention, good noise robustness, good process tracking, less power and area overhead and should support wide fan-in gates. However it is difficult to achieve all the required characteristics in the same keeper technique. The existing keeper techniques try to trade off one characteristics to gain in the other. This section gives a brief description of the three major keeper techniques that are used in the design of dynamic gates.

1. Conventional Keeper

The conventional keeper is shown in Figure 2. It consists of a weak PMOS keeper which is controlled by a feedback inverter. At the start of the evaluation phase, the keeper is on. If one of the pulldown legs turn on, a large contention current flows through the keeper that slows down the falling transition. As the dynamic node comes down, the keeper PMOS goes from linear to saturation resulting in an increasing contention current until the output rises sufficiently to turn the keeper off. The noise robustness of the gate can be improved by increasing the keeper size. However keeper upsizing has a severe impact on the power and delay. In case of wider fan-in gates if the keeper is sized for the worst case leakage it can turn out that this contention current exceeds the ON current of a single NMOS transistor and prevent the node from switching. Also excess short circuit power is wasted in the keeper and the inverter due to the larger contention current. The conventional keeper cannot be used beyond 20 pull down legs because the keeper required to maintain the robustness is too huge that during evaluation the logic fails to switch due to the larger contention current. Thus upsizing the keeper is certainly not the right way for achieving robustness. Also the process variations in the NMOS leakage is not tracked by the PMOS keeper.

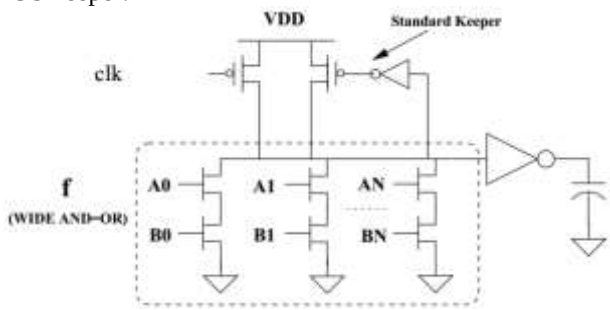

Figure 2: A wide AND-OR domino gate with conventional keeper

2. Conditional Keeper

The input data to the wide dynamic gates are ready before or close to the start of the evaluation phase. In such a case, the maximum time window for any potential output transition is only a fraction of the total evaluation time. The conventional keeper turns on unconditionally at the start of the evaluation phase, degrading the performance of the gate. However in the conditional keeper technique [7], the keeper is weak during the output transition window and strong for the rest of the evaluation time, if the dynamic node should remain high. The weak keeper during the transition window results in reduced contention and a faster output transition, while the strong keeper during the rest of the evaluation time results in a good robustness to leakage and noise. Figure 3 shows the circuit implementation with two keepers: a fixed weak keeper, PK1, and a conditional strong keeper, PK2. At the start of the evaluation phase, PK1 is the only active keeper. After a delay time,

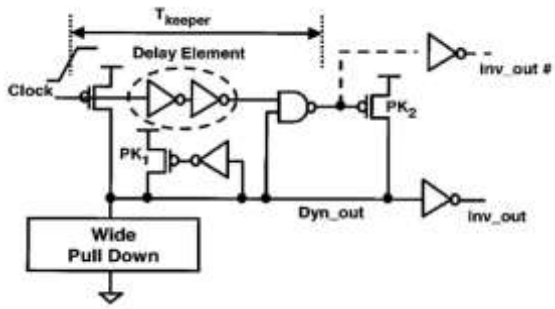

Figure 3: A wide AND-OR domino gate with a conditional keeper [14]

Tkeeper = Tdelayelement + TNAND, the keeper PK2 is activated, i.e., the output of the NAND gate goes low, only if the dynamic output should remain high. A chain of inverters can act as a delay element. By varying the size and the number of stages of the inverters, the Tkeeper can be varied. The size of the two keepers are chosen such that W(PK1) + W(PK2) =

W(PK0), where PK0 is the size of a conventional keeper. By reducing the contention current during the evaluation phase, the conditional keeper enables a high speed domino gate. However this comes at the cost of a significant amount of power dissipated in the inverter chain and nand gate. Also the delay chain does not track the variability in the NMOS pull down logic.

3. Current Mirror Keeper

The previous two keeper techniques did not have any process tracking. However in this current mirror method a replica of the pulldown logic is used to generate the reference leakage current which in turn is mirrored into the dynamic node to compensate for the leakage. Figure 4 shows the current mirror based keeper with the associated logic [8]. The replica NMOS has a width equal to that of the pulldown logic. The gate of the replica transistor is connected to VSS through a diode connected PMOS at the top.

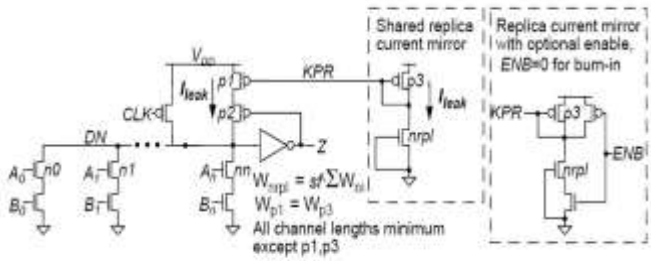

Figure 4: A wide AND-OR domino gate with a replica current keeper [12]

The PMOS mirror voltage is then used to control the keeper (P1) current. The mirror voltage varies based on the process corners. Thus this technique can track the process variations in the chip. Another advantage of this design is that the same replica circuit can be used to mirror the current to several other dynamic gates of same equivalent width.

The main limitation of this design is that since the keeper (P1) is in linear region, the amount of contention current during evaluation is large since the PMOS goes from linear to saturation. Also the concept of mirroring is meaningful only when the two transistors are in saturation. Thus this design is highly sensitive to mismatch between the two PMOS transistors. Also in the original design the replica width was increased ten times to compensate for any mismatch in the current mirrors which in turn is an additional overhead in terms of area, static power in the reference and also larger contention current. Another major issue with the current mirror keeper is that the replica transistor with its gate terminal connected to the source (GND), does not account for the noise voltage at the input of the domino gate. The design methodology proposed in [8] takes into account only the mismatch between the current mirror transistors. However the leakage contribution due to the noise voltage at the Read Select inputs (A0..A1) is an important factor that decides the keeper size and in turn the performance of the domino gate. The UGDN value of a domino gate with the replica current keeper can be adjusted by increasing the size of the reference transistor and the mirror transistors. The keeper transistor (P1) width required for a typical UGDN of 100mV is equal to the width of the pull down transistor which is again a huge area overhead per gate. The size of the gating keeper transistor (P2) width is chosen such that it supports the required leakage current to achieve the desired UGDN (Unity Gain DC Noise) level. The mirror voltage that is distributed to the various domino gates is susceptible to noise coupling and the design does not include any margins for it.

The mirror voltage VKPR in Figure 4 varies for different process corners thereby modulating the keeper strength. For a fixed size of the current setting transistor P3, the value of VKPR is close to VDD for slow NMOS corner than for the fast NMOS corner. The dynamic node of the domino gate is at VDD (in all process corners) which results in maximum DIBL in the pull down transistors. Thus the replica transistor does not track the leakage due to the DIBL. To keep the values of VKPR close to VDD irrespective of the process corners, the size of the mirror setting and the mirroring transistor has to be increased which results in area and power overhead. It can be seen that there are two conflicting design requirements in current mirror keeper. One the value of VKPR should as close to VDD as possible to track the DIBL effect. This requires a larger keeper and mirror transistor. However a larger keeper transistor will result in excess contention current and large area overhead, which degrades the performance of the domino gate. Thus the performance of the replica mirror domino gate is no better than the conventional keeper, because the keeper is essentially of the same type except for the current mirror. However the advantage of current mirror keeper is that it tracks the process variations in the NMOS logic and mirrors only the required current into the dynamic node. Due to this adaptive threshold tracking this keeper design can be used for large number of pull down legs.

Keeper Design Methodology

The domino gate in Figure 5 with the rate sensing keeper circuit can be modeled as a sense amplifier with one arm containing the dynamic logic and the other arm the reference rate transistor as shown in Figure 7.

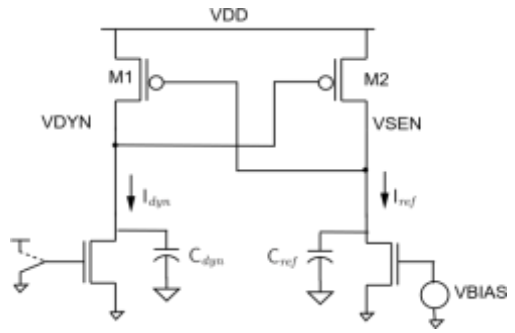

Figure 7: Sense amplifier model of the rate sensing keeper

It is essentially the difference in the voltage rates in both the arms that causes the nodes to switch in the appropriate direction. Let the current through pull down NMOS be I_{dyn} and the reference current be I_{ref}. Let the capacitances in the two nodes be C_{dyn} and C_{ref} respectively. This includes both the device and an approximate estimation of the interconnect capacitance. Thus the condition for the keeper is,

$KeeperON: I_{dyn}(I_{leak}) < I_{ref}$

$$KeeperOFF: I_{dyn}(I_{on}) > I_{ref}$$

The design of the keeper involves choosing appropriate sizing for the transistors and the right bias voltage. There are several parameters that can be controlled to achieve a given speed and robustness target. The primary requirement of the keeper is that;

1. It should track the process corner, with its rate varying exponentially with the threshold.
2. The keeper should replenish sufficient current to compensate the leakage at the dynamic node.
3. The reference rate should be between the leakage rate and pulldown rate of the dynamic node in any given process corner.

During the leakage state of the pull down logic, the keeper will be turned on completely. If the allowed noise level at the output is $V_{onnoise}$ then from the transfer characteristic of the output inverter, the voltage at the dynamic node can be found as $V_{dynnoise}$ which will be less than VDD. Thus the PMOS keeper will be in linear region of operation. The linear region current of the keeper must equal the pulldown leakage current for the given noise margin.

$$I_{dynleak} = \mu_p C_{ox} \frac{W_{keep}}{L} [(V_{sgp} - V_{thp})V_{sdp} - \frac{V_{sdp}^2}{2}$$

$$I_{dynleak} = I_{off}.W_{pd}$$

Where, $\mu_p C_{ox}$ is a device parameter that can be calculated, L is the channel length that is normally kept to be the minimum possible in the technology, $V_{sgp} = VDD$, $V_{sdp} = VDD - V_{dynnoise}, I_{off},$ the leakage per μm and W_{pd}, the total width of the NMOS pull down network. Using Equations 4.3 and 4.4 the width of the keeper can be found. The next step is to determine the required reference rate from the rates of the dynamic node. If $I_{dynleak}$ and I_{dynon} are the dynamic currents during leakage and pull down respectively and C_{dyn} is the dynamic node capacitance then;

$$R_{dynleak} = \frac{I_{dynleak}}{C_{dyn}}$$

$$R_{dynon} = \frac{I_{dynon}}{C_{dyn}}$$

$$R_{ref} = a.R_{dynon} + b.R_{dynoff}$$

Where R_{ref} is the required reference rate. 'a' and 'b' are positive constants that decide the robustness and speed of the circuit. Larger the value of 'a' more robust is the circuit and larger thevalue of 'b' higher is the speed. The scheme used here is the optimal point between robustness and speed. However the reference rate can be chosen as to have a higher speed or a better noise robustness by choosing the rate closer to $R_{dynleak}$ or R_{dynon} respectively. The value of C_{dyn} can be calculated by knowing the junction capacitance of the NMOS devices and the total pull down width. Though the capacitance value will keep changing as the node pulls down, an approximate value of the capacitance at VDD can be taken without significant error, as the regenerative action takes place when the dynamic node is closer to VDD. Equation can then be used for calculating the required peak current at the reference node.

$$I_{ref} = R_{ref}.\ C_{ref}$$

Where C_{ref} is the capacitance at the reference node. Though the width of the reference rate transistor is not known, an approximate value can be used because the dominating capacitances at the node are due to the keeper and other transistors. The value of the bias voltage VBIAS should be chosen close to the threshold voltage of the reference transistor. This will ensure an exponential variation of the reference rate with respect to various process corners. The size of the reference rate transistor can be found using Equation.

$$I_{ref} = \mu_p C_{ox} \frac{W_{ref}}{L} V_T^2 (1-\eta) exp \frac{(V_{gs} - V_{tn})}{\eta V_T}$$

Where; μ_p, C_{ox}, η, L & V_{tn} are device parameters, V_T is the thermal voltage, V_{gs} is the bias voltage, VBIAS and I_{ref} is the required reference current obtained from Equation above. The width of the reference rate transistor can be obtained from last Equation. The above design procedure has to be done for the fNsP corner in which the leakage is high and the keeper is weak. The values of other transistors M2, M3, M5 and M6 can be chosen to be of minimum size and can be varied according to the given design specification.

V. CONCLUSION

In this paper we proposed an adaptive keeper technique called RSK The present work proposes a keeper design methodology that significantly improves the performance of the dynamic gates with less overhead in area, power and delay. The proposed design also achieves a better tracking of the delay across various process corners thereby improving the yield of the designs that uses the dynamic gates. The technique essentially utilizes the difference in the rate of discharge between the two states of the dynamic node namely leakage state and ON state. It uses a rate controller to generate a reference rate that is compared with the dynamic node rate. This is achieved by controlling the dimensions and bias voltage of a reference transistor whose threshold variations tracks the NMOS device variations. Since the technique has reduced contention current it allows for more number of pull down legs to be used in the domino logic. This is a boon for several superscalar processors that demand complex register files and memories.

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