# Designing of Sequential Circuits using Reversible Logic Gates

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*Abstract*— Reversible logic has become one of the most promising research areas in the past few decades and has found its application in several technologies; such as low power CMOS , nanotechnology and optical computing. The main purpose of designing reversible logic is to decrease quantum cost, depth of the circuits and the number of garbage outputs. Flip flop is the building block of the sequential circuits. Since the output of a sequential circuit depends not only on the present inputs but also on the past input conditions, the construction of sequentical element using reversible logic gates is quite complex than that of combinational circuits. This paper represents the design and simulation result of reversible D flip flop, Ring counter, Johnson counter and LFSR.

*Keywords*— Reversible logic, reversible gate, power dissipation, flip flop, garbage.

#### I. INTRODUCTION

**Reversible logic gates-** Reversible logic supports the process of running the system both forward and backward. This means that reversible computations can generate inputs from outputs and can stop and go back to any point in the computation history. A circuit is said to be reversible if the input vector can be uniquely recovered from the output vector and there is a one-to-one correspondence between its input and output assignments, i.e. not only the outputs can be uniquely determined from the inputs, but also the inputs can be recovered from the outputs Energy dissipation can be reduced or even eliminated if computation becomes Information-lossless.

A reversible logic gate is an n-input n-output logic device with one-to-one mapping. Also in the synthesis of reversible circuits direct fan out is not allowed as one-to-many concept is not reversible. However fan-out in reversible circuits is achieved using additional gates. A reversible circuit should be designed using minimum number of reversible logic gates. From the point of view of reversible circuit design, there are many parameters for determining the complexity and performance of circuits.

<u>*Flip Flop*</u> - A flip flop can store one bit of information. Flip flop changes their content only either at rising or falling edge of clock signal.

Here as D flip flop is designed using reversible logic, which is used to construct other sequential circuits like ring counter, Johnson counter, linear feedback shift register (LFSR).

#### II. LITERATURE REVIEW

In this section, detailed literature review is done that aims to review the critical points of current works. Here the information collected about researches and innovations carried out on the related technologies have been done. This section will highlight the recent trends and innovations in the concerned technology.

Gordon. E. Moore [1] in 1965 predicted that the numbers of components on the chip will double every 18 months. Initially he predicted only for 10 years but due to growth in the integrated circuit technology his prediction is valid till today. His work is widely recognised as the Moore's law. The effect of Moore's law was studied carefully and researches have come to the conclusion that as the number of components in the chip increases the power dissipation will also increase tremendously. It is also predicted that the amount of power dissipated will be equal to the heat dissipated by the rocket nozzle. Hence power minimization has become an important factor for today's VLSI engineers.

Landauer [2] determined that the amount of energy dissipated for the loss of each bit of information is at least KTln2. During any computation the intermediate bits used to compute the final result are lost, this loss of bits is one of the main reasons for the power dissipation.

C.H.Bennett [3] in 1973 discovered that the power dissipation in any device can be made zero or negligible if the computation is done using reversible model. The theory is proved with turning machine which is a symbolic model for computation developed by turning. Bennett also showed that the computations that are performed on irreversible or classical machine can be performed with same efficiency on the reversible machine. Based on the above concept the research on the reversibility was started in 1980's. Edwardv Fredkin and Tommaso Toffoli [4] introduced new reversible gates known as Fredkin and Toffoli reversible gates based on the concept of reversibility. These gates have zero power dissipation and are used as universal gates in the reversible circuits. These gates have three outputs and three inputs, hence they are known as 3\*3 reversible gates.

In the year 1994 shor [5] did a remarkable research work in creating an algorithm using reversibility for factorizing large number with better efficiency when compared to the classical computing theory. After this the work on reversible computing has been started by more people in different fields such as nanotechnology, quantum computers and CMOS VLSI.

Peres [6] introduced a new gate known as Peres gate. Peres gate is also a 3\*3 gate but it is not a universal gate like the Fredkin and Toffoli gate. Even though this gate is not universal gate it is widely used in much application because it has less quantum cost with respect to the universal gate. The quantum cost of the Peres gate is 4.

H Thalpliyal and N Ranganathan [7] invented a reversible gate known as TR gate. The main purpose of introducing this reversible TR gate was to decrease the garbage output in a reversible circuit.

H Thalpliyal and N Ranganathan [8] introduced the reversible logic to sequential circuits. Implementation of the sequential circuit such as D-latch, T latch, JK latch and SR latch using Fredkin and Feynman gate has been done. After this work more research has been done on sequential circuits using reversible gates.

Using the combination of Fredkin and Feynman gate a new gate known as Sayem gate was proposed by Sujata S. Chiwande Prashanth R. Yelekar [9] sayem gate is a 4\*4 reversible gate and is used in designing sequential reversible circuits.

M.L. Chuang and C.Y. Wang [10] proposed that the numbers of gates, the number of garbage output were reduced in implementing the Latches and when the results will be compared [9] with 25% improvement was achieved.

## III. METHODOLOGY

## BASIC REVERSIBLE LOGIC GATES

## 1. Fredkin Gate

Fredkin gate is a (3\*3) conservative reversible gate originally introduced by Petri. It is called (3\*3) gate because it has three input and three output

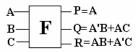


Figure.1 Fredkin Gate

## 2. Feynman Gate

Feynman gate is a 2\*2 one-through reversible gate shown in Fig.2. It is called 2\*2 gate because it has 2 input and 2 output. One-through gate means that one input variable is also the output.

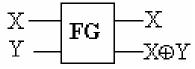


Figure.2 Feynman Gate

#### **REVERSIBLE LOGIC DESIGN**

## 1. D Flip Flop.

A flip flop is bistable electronic device used to store 1 bit memory. D Flip Flop is designed here using fredkin gate and Feynman gate.

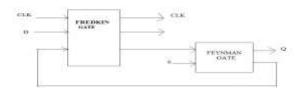


Figure.3 Reversible D flipflop

#### 2. Ring Counter

This is the simplest shift register counter.Here the ring counter is being constructed using above D flip flop.The output of D flip flop is connected to the input of another D flip flop.Then the output of last flip flop is connected to the input of first flip flop.

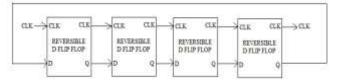


Figure.4 Reversible Ring counter

#### 3. Johnson counter

This is also known as twisted ring counter. It is also designed using reversible D flip flop same as reversible ring counter but the output of last flip flop is passed through not gate then its output is connected to the input of first D flip flop.

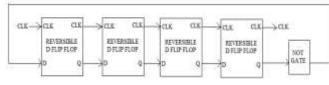


Figure.5 Reversible Johnson counter

#### 4.Linear feedback shift register

LFSR is a shift register whose input bit is a linear function of its previous state. The most commonly used linear function of single bits is XOR. Thus an LFSR is most ften a shift register whose input bit is driven by the xor of some bits of the overall shift register value. So here we used Feynman gate in place of XOR gate.

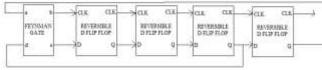


Figure.6 Reversible LFSR

#### IV SIMULATION RESULTS

## A. REVERDIBLE D FLIP FLOP

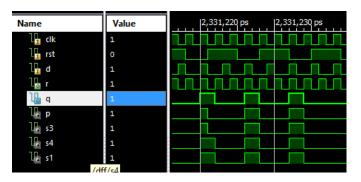


Figure.7. Simulation waveform of Reversible D flipflop B. REVERSIBLE RING COUNTER

Name	Value	1,195,645 ps	1,195,650 ps	1,195,635 ps	1,195,660 pc
in ck	1				
ieset	0				
n 📲 q13:01	1000	0000	1000 0100	0010 0001 ( 1000	1 0100 0010
<ul> <li>tempEx08</li> </ul>	1000	0000	1000 0100	0010 0001 1000	1 0100 0010
reset_d	0				
to input	Ø				_
light int	1				
14 12	1				
14 13	1				
14 14	1				

Figure.8. Simulation waveform of Reversible Ring Counter

#### C. REVERSIBLE JOHNSON COUNTER

Name	Value		1,343,590 pc	1,343,595 ps	1,343,600 ps
1∎ ek 1∎ reset	0 1				
jahnson[3:0]	0000	0000.	1000 1100 1	1110 (1111 ) 0111	0011 0001
▶ 📑 temp[3:0]	0000	0000	1000 1100 (1	1110 (1111 ) 0111	0011 0001
Wir wir	1				
14 rt	0				PT 1 2 1
12:	0				
lin es	9				
1 r4	.0				

Figure.9. Simulation waveform of Reversible Johnson Counter

# D. REVERSIBLE LFSR

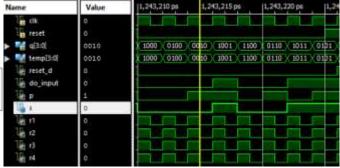


Figure.10. Simulation waveform of LFSR

## IV. CONCLUSIONS

We have designed efficiently D flip flop, Ring counter, Johnson counter and Liinear feedback shift register using reversible logic gates such as fredkin gate and Feynman gate. By using this circuits we can built other sequential circuits. As LFSR is building block of Built in self register we can design it further in a future.

#### ACKNOWLEDGMENT

We would like to express our sincere thanks to the anonymous reviewers for their critical suggestions which helped in improving the manuscript.

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