Process Variation: Performance Degradation Analysis Each New Technology

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***Abstract*— Scaling is the primary engine for growth of VLSI industry in last few decades. The scaling improves all device parameters simultaneously which results in improved devices and systems. The scaling new has reached to sub-nanometer regime where other undesirable effects are coming into pictures. Process variations is deviation in devices parameter from their original value and becoming so severe that further scaling is not possible. The designs which are implemented without considering process variations fails to provide correct output. The modern devices not only demand high performance, energy efficient operation but also demand operation should be done accurately. The process variation making the device behaviour deterministic to probabilistic. Therefore, critical analysis is required for performing some signal processing accurately. This paper critically analyses different types of process variations. Further the process variations effect on the logic is also analysed.**

***Keywords*— Very Large Scale Integration, Fabrication, Process Variations, Technology scaling.**

I. INTRODUCTION

Over the past four decades CMOS technology scaling [1] has been the primary engine that powered the ascent of semiconductor industry and provided a path toward both denser and faster integration an engineering achievement unmatched in human history. There are several research works that deal with the impact of technology scaling in various aspects of VLSI design where process variation has been found more of a concern and has received an increased amount of attention in recent years. Researches studies on process variation exposed that process variations are expected to get worsen in future technologies, and the effect of these variations looks like inherent unreliability in the circuits.

The conventional design approach considers that electrical and physical properties of the transistors are deterministic which results in predictive behaviour of the design. This assumption fails as the technology moves towards sub-65nm design. The device behaviour below 65nm changes from deterministic to random. This fluctuation in the device characteristics is due to variation in process parameters such as change in length, width, oxide thickness, number of dopant in source and drain diffusion etc. These deviations in device characteristic due to process are called process variation [2].

The process variation is due to the manufacturing process including sub-wave length lithography, small variations in chemical mechanical policing etc. The process variation was unnoticeable until 0.35µm technology whereas at present the design without considering the effect of process variation fails to provide design output [3]. Different process variations are modelled in terms of variation in threshold voltage and as technology scales, the shift in threshold and spread of threshold variation increases. Therefore, the process variation is shown by a distribution graph showing variations in threshold and which in turn deviation in the delay and leakage parameters of the whole circuit. For the present ICs, the major factor for yield loss is only due to process variations [4]. The effect of process variation is so severe in the modern designs that design behaviour has changed from deterministic to probabilistic [5]. Therefore, a critical analysis of the process variation of different technology is required.

In order to critically analysis the process variation, in this work an exhaustive literature review is done on the different sources of process variations and its classification based on its effect with time. Further, different modelling and severity of the process variations are analysed. Finally, the paper presents a critical analysis of the process variation effect on the performance of the logic. Severity analysis presented in this paper is based on the simulation where logic is implemented and simulated on EDA tool.

II. LITERATURE REVIEW

The device scaling has reached the VLSI chips to provide performance five order of magnitude higher than those of three decades earlier. At the same time now some new phenomenon such as process variation have raised and severely affecting the reliability of the device such that further scaling is not possible. Die size, chip yields and design productivity have so far limited transistor integration; as technology scales further the focus has shifted to process variation. This section discusses different types of process variation.

2.1 Process Variation

Device scaling has been the prime source to improve the performance of the VLSI designs. But, at smaller technology nodes, especially below 90nm, as device feature sizes approach fundamental dimensions, variation gets a larger percentage of device features and process variation becomes eminently important. If process variation causes the performance of a particular metric, such as leakage and/or delay to rise above or fall below the desired specification given for that device, it significantly reduces the yield [6]. Process variation is a natural phenomenon of variation in the attributes of devices, such as channel length (L), width (W) and gate-oxide thickness (Tox). It refers to the deviation between desired (prior fabrication) and obtained device parameters after fabrication.

2.2 Sources of Process Variation

There is some process and in that process sources of variations are listed below [6].

- **Wafer:** exhibits variations due to topography and reflectivity
- **Reticle:** exhibits variations due to CD error, proximity effects and defects
- **Stepper:** exhibits variations due to lens heating, improper focus, improper dose and lens aberrations
- **Etch:** exhibits variations due to power pressure and flow rate.
- **Resist:** exhibits variations due to thickness, refractive index.
- **Develop:** exhibits variations due to time pressure rinse.
- **Environment:** exhibits variations due to humidity and pressure.

2.3 Classification of Process Variation

The process variation can be divided into two major categories from circuit design perspective namely: 1) Inter-die variation (die-to-die) and 2) Intra-die variation (within die) variations as shown in Fig. 1. The inter-die variation is results in the deviation of device characteristic but are in symmetrical in nature i.e. all the devices on the same die will have same deviation, whereas intra-die variation shows random deviation in device parameters.

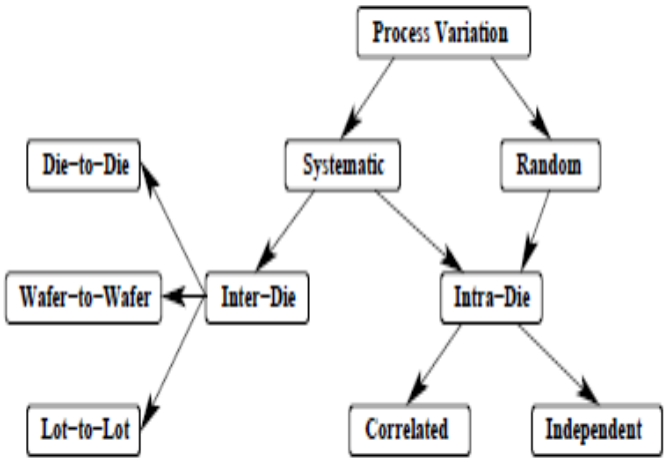

Fig. 1 Process variations: inter-die and intra-die

The aforementioned process causes variation in the device length, width, oxide thickness, dopant atom concentration etc. as shown in Fig. 2. All these affect changes the devices behavior from deterministic to probabilistic.

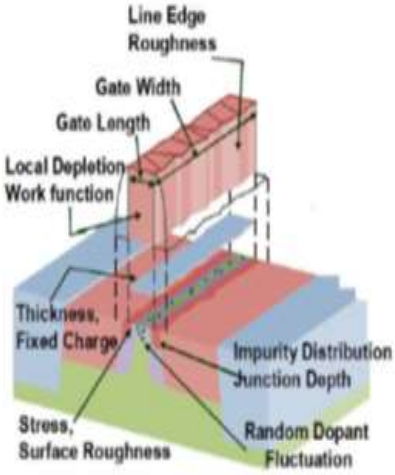

Fig. 2: Source of process variation

2.3.1 Inter-die process variations

The inter-die variation [7] shows the variation in the device parameters place on the different die or different wafer or lot, which ideally should be identical values as shown in Fig. 3. This deviation in device parameters is occurred due to sub-wavelength lithography process and exhibits symmetric variation in nature i.e. it affects all the devices on different dies with similar amount. From mathematical point of view, inter-die variation shifts the device parameters mean value to some other location e.g. device threshold of all the devices shifts to higher or lower value. It is observed that beyond 45nm technology, the inter-die variation was more significant over intra-die i.e. yield loss is more due to inter-die than intra-die.

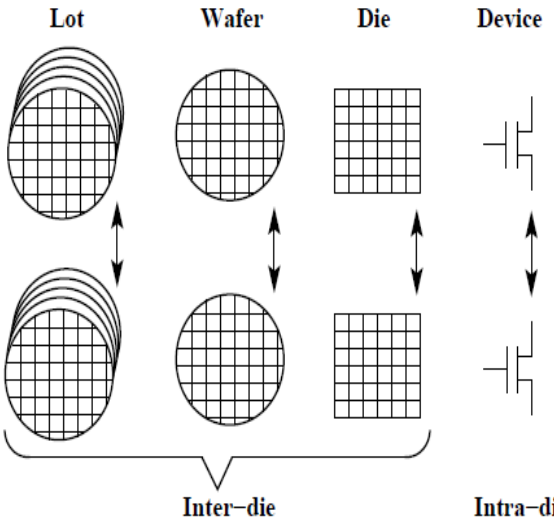

Fig. 3: Process variations at different phase of fabrication

2.3.2 Intra-die process variation

The major drawback of the intra-die variation is its random (unpredictable) nature of the variations. This random behavior occurs due to random nature of dopant atoms producing random dopant fluctuation (RDF), line edge/width roughness LER/LWR and T_{OX}. Further, the deviation increases with how close/dense the circuit is implemented i.e. these variations significantly depends on the layout of

the design and exhibits spatial correlation. Therefore, it necessary to address the intra-die variation within logic and memory to work in the desired manner. At scaled technology where there is high process variations accurate modeling approach is needed to predict correctly the circuit behavior to reduce the design cost and help improving the circuit yields.

In the intra-die variation two major sources of process variations are the random dopant fluctuations and line edge roughness. In the following subsection we will discuss each of this issue in detail.

2.3.2.1. Random Dopant Fluctuations

This process variation occurs due to random motion of the dopant atom while forming the source and drain diffusion as shown in Fig. 4 [8]. During the process of ion implantation for forming two diffusions, dopant atoms are bombarded on the p-type substrate. In this process the location of the dopant atom depends of the kinetic energy of the atom, time of diffusion and environment temperature. Small deviation in the temperature and other parameter will change the concentration of dopant atoms [8].

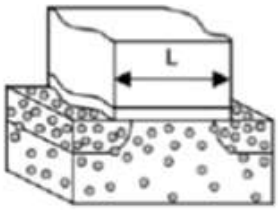

Fig. 4: Illustration of random dopant fluctuation.

In the order technologies where the dimension of the device was in micron, the number of dopant atoms was in order of three, therefore, there small deviation in the number of dopant and its location will not change the property of device. At the scaled device dimension number of dopant atoms has reduced significantly in the range of 50-60. Therefore, any deviation or dislocation will change the characteristics of the device significantly. It is very difficult to control the device parameter at this stage due to limited number of atoms.

2.3.2.2 Line-edge and width roughness (LER and LWR)

The line-edge roughness [9] is process variation occurred due to imperfect etching process as shown in Fig. 5. It refers to the deviation in the poly width that forms the gate of the device. This deviation in the device width results in the shorter or larger transistors channel length. This may cause the mismatch in the device channel length of two transistors on the same chip. This intra-die variation changes the device behavior from deterministic to stochastic.

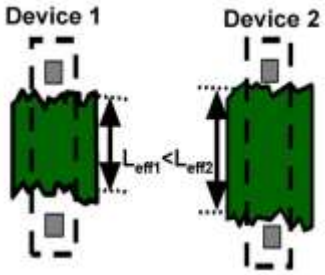

Fig. 5: Channel length variation

The high-k material may reduce the severity of the intra-die process variation as it reduces the gate-leakage. It therefore allows to further scale the device oxide thickness without increase in the leakage. But the high-k material has its own limitation of such as strain, dual band-edge work-function process integration; thermal instability etc. reduces the reliability of the device.

2.3.3 Temporal Variations

In addition to the above mentioned process variation, another kind of variation is the temporal variation the come within the device with its age i.e. its severity increases with device usage. In this PV device degrade with time and do not retain its original specifications e.g. the defect generated within the SiO_2 increases over the time and degrades the characteristics of the device. Following subsection details different types of temporal variations and their severity will be analyzed.

2.3.3.1 Negative Bias Temperature Instability

The Negative bias temperature instability is the major source of temporal variation occurred in the PMOS device when biased negatively for a long time. The stress due to negative biasing causes defect generation at the Si-SiO_2 interface and increase with time. These defect increases the threshold of PMOS which increases the delay of the device as shown in Fig. 6.

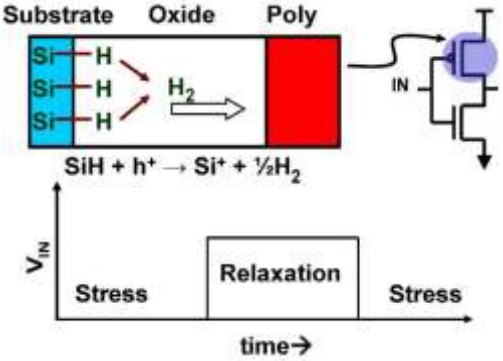

Fig. 6: NBTI induced degradation process

The NBTI [6] have special property recovery property i.e. the created dangling bonds due stress recovers when the stress is removed partially. Since the recovery mechanism is partial, there is some defects still remain in the oxide layer which degrade the characteristic of the MOS device. As shown in Figure 3.6, when inverter is negatively biased Si-H bond breaks and created Si^+, when the stress is removed, some Si^+ again make Si-H bond while H^+ makes H_2.

2.3.3.2 Positive Bias Temperature Instability

Similar to the NBTI, the PMOS device exhibits positive bias temperature instability (PBTI) [6] in NMOS devices. In the older technologies, the effect of NBTI was more severe as compared to PBTI and was ignored. But in the sub-nanometer designs due to the usage of high-k material, PBTI is also severe as NBTI. Therefore, significant research work has also started to address the effect of PBTI in addition to the NBTI.

2.3.3.3 Hot Carrier Injection (HCI)

The HCI can induce defect at Si-SiO2 interface or in the bulk and degrades the device performance similar to the NBTI. The high electric field in the device due to reduced device dimension make the charge carrier's kinetic energy very high. This carrier gets heated and result in impact ionization as shown in Fig. 7.

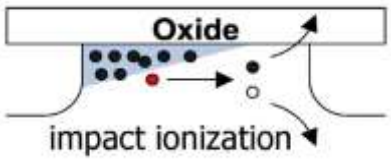

Fig. 7: Illustration of hot carrier injection.

These heated carriers generated due the impact ionization move in to the oxide layer and degrades the device characteristics. Further the effect of HCI is more significant in NMOS as compared to PMOS as the electrons have higher mobility over the holes. Moreover, the effect of HCI is more when the NMOS device is switched from low-to-high.

2.3.3.4 Time Dependent Dielectric Breakdown (TDDB)

It is also a serious issue of device reliability. The TDDB may occur due to high electric field and very small oxide thick where small deviation in the oxide thickness will significantly change the electric field. This large electric filed may create pin-holes i.e. small leakage current will flow across this hole as shown in Fig. 8.

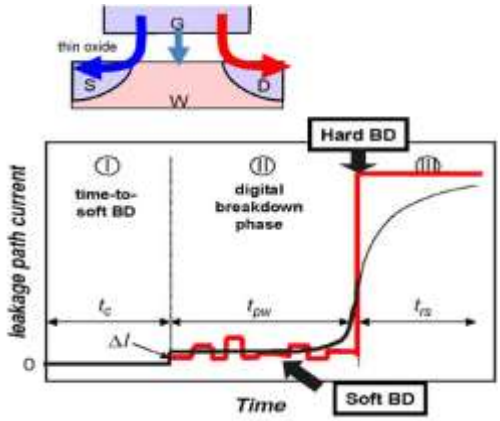

Fig. 8: Illustration of time dependent dielectric breaks down.

The TDDB also known as oxide failure occurs mainly due to variation in oxide thickness which creates a short path between channel and the gate. From this path small leakage current flow which may later cause sudden energy burst.

III. PRAPOSED WORK

The section provides detailed discussion on the proposed work on process variations severity analysis. It starts with the design, implementation and then evaluation of degradation of performance of the logic due to process variation.

3.1 Analysis of process effect on performance

The methodology followed to evaluate the severity of the process variations at different technology is given by the flow chart in Fig. 8.

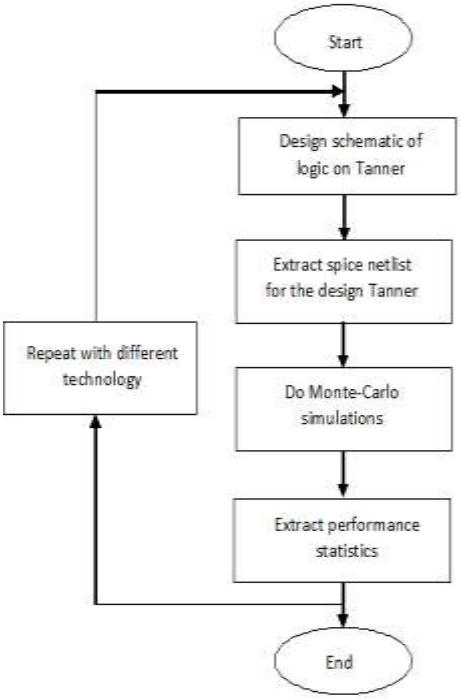

Fig. 8: Proposed flow chart to compute PV statistic on logic performance.

In order to evaluate the process variation severity on the path delay of the logic, a single threshold inverter is considered as shown in Fig. 9. The threshold of these MSOFETs within this inverter is varied due to process variation. To measure the delay, a transient pulse is applied at the input and corresponding transition at the output are observed. Due to the variations in the threshold voltage, different delay is obtained and corresponding statistic (mean, median and standard deviations) are computed.

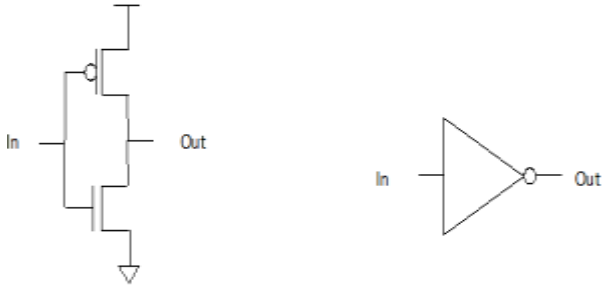

Fig. 9 Schematic diagram and symbol of inverter

Further using this inverter, inverter chain consists of 100 inverters and 500 inverters as shown in Fig. 10 are also considered to compute the net effect on the logic delay. Although, the procedure to compute the variation statistic is similar to the single inverter, consideration of large chain of inverter cancel out the random intra-die variations while provide more accurate inter-die variations. This inverter chain accurately models the general path of the logic.

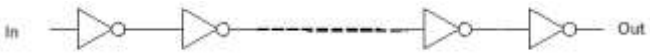

Fig. 10: Inverter chain (100 inverter) diagram.

The simulation results in the next section illustrates the severity of the process variation on different inverter chain at different technology.

IV. EXPERIMENTAL RESULT & ANALYSIS

To evaluate the performance deviations due to PV, inverter chains are designed on Tanner. Spice netlists are extracted and simulated with Monte-Carlo simulation [10]. The designs are implemented with different size based on the technology considered e.g. in 90nm technology L_{MIN} considered is 90nm while in 32nm design L_{MIN} can be taken is 32nm. The technology files considered are the 90nm, 65nm, 45nm, and 32nm. It is observed that at 90nm, 65nm, 45nm, and 32nm technologies, the change in threshold variations due to process variations are 10%, 20%, 40%, 70% respectively. Finally, these spice netlists are simulated and performance metrics are extracted.

5.1 Implementation of design on Tanner:

The schematic of the single inverter designed on the Tanner is shown in Fig. 11. It consists of two transistor sized properly based on the kind of technology considered while simulation.

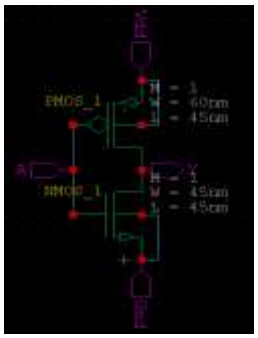

Fig. 11: Schematic of inverter on Tanner.

The functionality of the implemented designs is also verified by simulation. Further, a symbol for the inverter is created to use this inverter for making inverter chain. The schematic of the 100 inverter chain is shown in Fig. 12. The inverter chain utilizes the same inverter designed on the Tanner. The primary input to this inverter is the A while the output is Y.

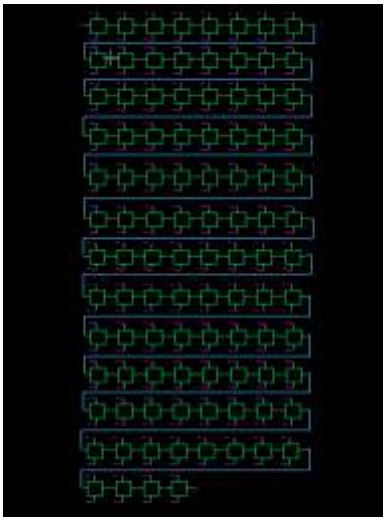

Fig. 12: Schematic of inverter chain (100 inverters).

Further, an inverter-chain consists of 500 inverters is also designed to evaluate the effect of process variation on the longer path. The spice netlists for these designs are extracted and simulated with the specified technology files. The simulation results for different technology are given in the next section.

5.2 Simulation Results and Analysis

In order to compute the performance deviation due to process variation, different threshold variations are considered at different technology [6]. The statistic of the threshold variation as illustrated in Table 1 for pMOS transistor reflect that the variance increases with increasing scaling i.e. at latest technology (32nm) node deviations are much more over the 90nm.

Table 1: Threshold variation statistic (mv) for pMOS at different technology.

Metrics	Technology			
	90nm	**65nm**	**45nm**	**32nm**
Mean	-338.0816	-362.8707	-229.5111	-278.4249
Median	-339.9022	-367.0919	-232.8989	-287.4947
Variance	0.1113068	0.5983488	0.3854291	2.7624
Sigma	10.5502	24.4611	19.6323	52.5586

Similarly, to the PMOS device statistics for the nMOS considered. With this statistics of the devices, the designs (single stage inverter, inverter chain of 100 inverters and 500 inverters) are simulated. The simulation results are shown in the next subsections.

5.2.1 Simulation results for single inverter

The delay distribution metrics for single stage inverter (SSI) simulated with different technology node is given in Table 2. The simulation results show that mean of delay is reducing

with each technology which is due to outcome of the scaling. But, with this reduced delay, deviation in the delay with respect to the mean value is increasing with each technology which is very severe and degrades the yield of the designs. As the variation from the mean value reduces, some of the IC may fails due to exhibiting longer critical path. From the simulation results show that this deviation increase by more than **6X** in at 32nm over 90nm technology.

Table 2: Delay statistic of SSI at various technologies.

Delay (ps)	Technology			
	90nm	**65nm**	**45nm**	**32nm**
Mean	23.7	23.6	44.4	2.4.7
Sigma	3.39	6.13	10.8	20.7

Finally, the delay distribution as shown as in Fig. 13 reflects a comparative increase in the standard deviation in the scaled technologies.

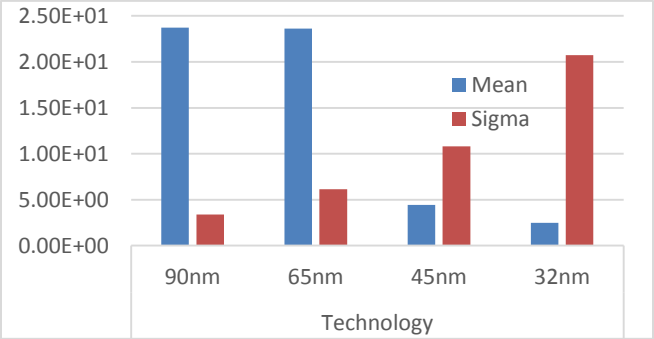

Fig. 13 Delay variation of SSI at various technology.

In order to more accurately check the effect on the path delay in the logic, inverter chain is considered.

5.2.2 Simulation results for inverter chain

The simulation result of the delay metric variation is computed for inverter chain at different technology and illustrated in Table 3. It can be seen from the Table that delay is getting reduced with each technology but at the same time spread of delay distribution increases with technology. Therefore, it can be seen that inter-die variation causes delay variation increases with each scaled technology and reaches to an intolerable limit.

Table 3: Delay statistic of 100 inverter chain.

	Technology node			
metrics	**90nm**	**65nm**	**45nm**	**32nm**
Mean	4.34E-09	3.95E-09	2.70E-09	1.01E-09
Sigma	5.75E-11	9.88E-11	2.43E-10	6.35E-10

Fig. 14 shows comparative analysis of delay variation at different technology nodes.

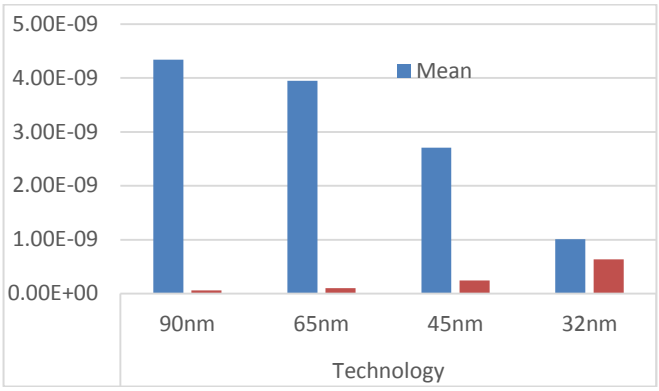

Fig. 14 Delay statistics of an inverter chain (100 inverters) at different technology.

Similar to the inverter chain of 100 inverters, 500 inverter chains is also designed and simulated. These simulation results show that process severity increases rapidly with each new technology.

V. CONCLUSION

This thesis analysed the effect of process severity with technology scaling by considering inverter chain and simulated under process variations at different technology. To achieve this, different size inverter chain (100 inverters and 500 inverters) is considered and implemented on Tanner. These inverter chains are simulated under process variation with different technology files (90nm, 65nm, 45nm, 32nm). From the simulation results it can be seen that this deviation increase by more than **6X** in the designs at 32nm technology over the design at 90nm technology.

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