VLSI Design of Novel Area Efficient Accuracy Reconfigurable Adder for Error Resilient Applications

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***Abstract*— The portable devices of the modern era employing multimedia applications demands high performance arithmetic units. Adder is one of basic operation used to perform different signal processing. Significant research has been done to achieve high performance adder. Approximate adder has recently become active area of research for achieving high performance arithmetic units. Therefore, different approximate adders are developed in the literature. In this paper, presents a novel accuracy reconfigurable adder and then the performance of the proposed adder over the existing adder designs. The proposed and existing designs are implemented and simulated with benchmark input to compute the efficacy of proposed over the existing architectures. The simulation results show that proposed adder requires reduced area over the existing designs.**

***Keywords*— Digital Signal Processing (DSP), Approximate adders, Image Processing, Integrated Circuits, VLSI, Low Power Design.**

I. INTRODUCTION

The multimedia applications on the portable devices are increasing rapidly. These applications exhibit huge computations to achieve desired output [1], [2]. Therefore, significant research has been carried out to achieve high performance signal processing. Further, the growing number of functions on these devices demands VLSI architectures which processing signal very efficiently which ultimately increases the complexity of the designs [3]. The complexity of today's design is very high which result in high power and delay in the present devices and it is growing with increasing functionality on the same device. The conventional approaches to improve the performance of these design is the device scaling. The device scaling approach has reached to a level where further scaling brings severe process and other variation effects [4].

The aggressive scaling in the deep sub-nano meter regime brings the process variation to detrimental its performance. The design without considering it will fail to provide desired output. Further, addition circuit to mitigate the effect of process variation is very costly in terms of power, area and delay such that gain due scaling are less than overhead [5]. Therefore, other design methodology is required to develop designs for the modern devices. There are several applications where the approximate results are acceptable and this can be exploited to reduce the complexity of the designs.

The most fundamental and frequently used arithmetic operation is addition to performance different signal processing. Therefore, design of high performance adder may significantly improve the performance of these applications. Along with conventional ripple carry adder [6-10] several high performance adders have been developed. This adder provides improved performance at the cost of increased area/power overhead. Therefore, to improve the three metrics simultaneously approximate adders are developed for the error resilient applications.

Significant research has been carried out to achieve efficient approximate adders such as error tolerant adder (ETA-I) [11], ETA-II, ETA-IIM etc. In ETA-I operands are divided into upper and lower parts where upper part is computed accurately while the lower part approximately. In addition to the approximate adders, accuracy configurable adder (ACA) is also presented. This adder provides variable accuracy at the cost of reduced performance. Therefore, accuracy reconfigurable design can be used in wide applications due to exhibiting variable accuracy. The existing adder designs are not efficient and therefore, demanding more area efficient and performance efficient adders.

This paper presents a novel accuracy reconfigurable adder. The rest of the paper first discusses different accurate/approximate adders followed by proposed accuracy reconfigurable adder and finally compare them by implementing and computing design and quality metrics.

II. Literature Review

This section details different accurate and approximate and then presents approximate and accuracy configurable adders.

2.1 Ripple Carry Adder

It is the simplest accurate adder as shown Fig. 1 and consists of some full adders. Each of full adder (FA) have three inputs and two outputs. RCA [6] is very area efficient but exhibits poor delay metrics. Mostly, conventional circuits designed with ripple carry adder where performance is not the prime issue and area is the major factor.

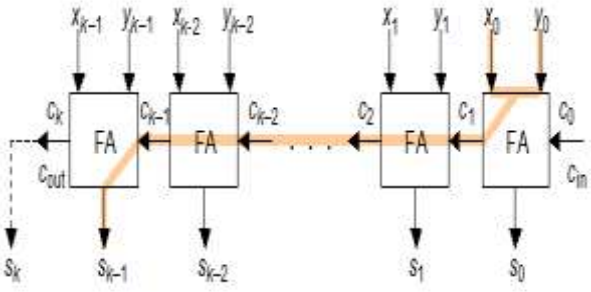

Fig. 1: RCA architecture.

2.2 Carry Select Adder

The carry-select adder (CSL) [7] is high speed adder and provides higher performance at the cost of area overhead. The architectural diagram of CSL adder is shown in Fig. 2. It divides input bits into small groups and perform addition using small RCA blocks. This small RCA blocks have two carry paths: one for logical zero and one for logical one. Thereafter, carry propagation at high RCA become selection, consequently reduces significantly delay at the cost of area overhead over conventional design.

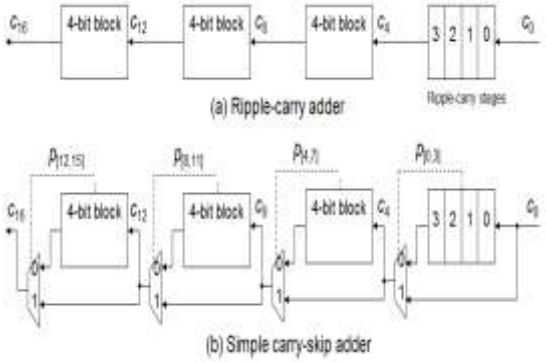

Fig. 2: CSL adder architecture.

2.3 Carry Look-ahead Adder (CLA)

The CLA [8] determines the carry in advance at MSB position to reduce the propagation delay. As it reduces the propagation time, it significantly improves the performance of the adder with little area and power overhead of the adder. The CLA computes the carry-in for the different group of sub-adders and make used of this carry-in signal to reduce the dependency. The logical block diagram of the CLA is shown in the Fig. 3. It allows independent carry generation for each bits and consists of the simple AND & OR logic.

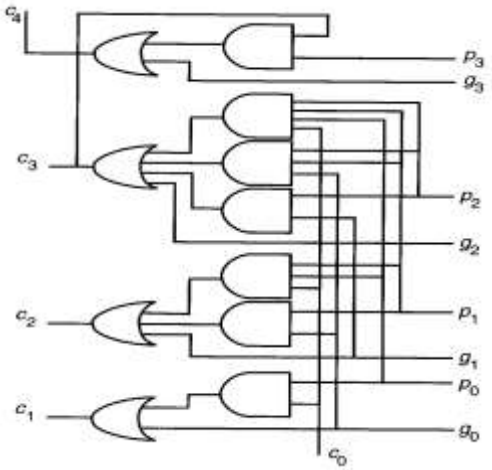

Fig. 3: Architecture of CLA.

2.3 Need of approximate adder

The accurate architectures of adder fail to provide energy efficient high performance addition. In order to improve the all the three parameters, approximate adder have been used recently. Moreover, there are applications where, 100% accuracy is not required i.e. these applications can accept output with small error. For these applications approximate adder can be designed such that there is significant improvement in design metrics with small introduced error.

3.3 Error Tolerant Adder (ETA-I)

The ETA-I [11, 12] divides operand into two parts: namely higher order accurate part whereas least significant bit makes a lower part. The addition starts from the segmentation point in the two opposite direction in parallel. For the MSBs accurate addition is done from right to left to preserve its correctness and for inaccurate part no carry signal will be generated. To reduce error in overall addition a method is utilized in the approximate part in which carry will not be generated and forward. It checks both bits of the operand from right to left direction and if both bits are not logic '1', normal addition is done without carry which can be achieved by XOR operation.

The architecture of the ETA-I is shown in the Fig. 4, which shows that ETA-I is divided in two parts: accurate and inaccurate parts. The accurate part contains some MSBs whereas the inaccurate part contains few LSBs. Since the higher order bits play more important role than the lower order bits' normal addition method is applied for accurate part to preserve its correctness and special strategy is adopted for the inaccurate part.

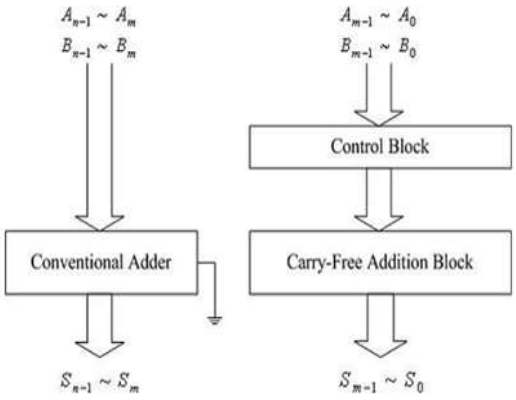

Fig. 4: Architecture diagram of ETA-I.

The working principle of the ETA-I can be better understood via an example as shown in Fig. 5. In this, we take two 16-bit input data as, X= "1011001110011010" (45978) and Y= "0110100100010011" (26899).

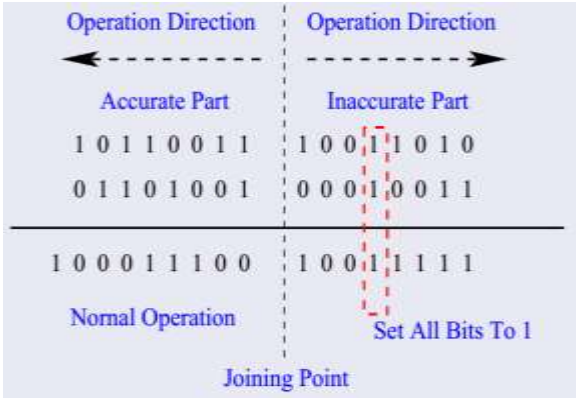

Fig. 5: Working of ETA-I.

3.4 Sloppy Adder

A sloppy adder [13] that computes approximate sum with reduced complexity as shown in Fig. 6.

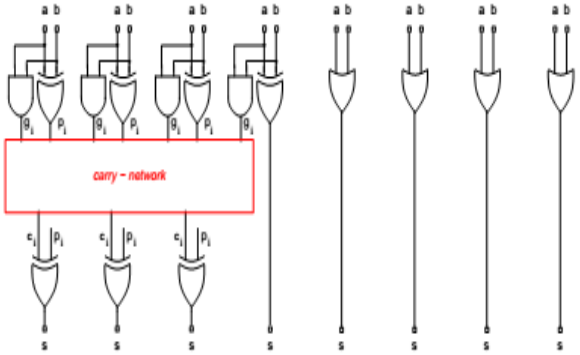

Fig. 6: 8-bit sloppy k = 4 adders

In the proposed sloppy adder, least significant bits are computed with approximate logic due to their small contribution in the overall sum while the MSBs are evaluated in accurate manner to maintain the quality. In the approximation logic, author used OR logic to compute least significant some bits.

3.4 Accuracy Configurable Adder (ACA)

To improve the wide applicability of the approximate designs, an accuracy configurable adder [14] is presented which can configure the accuracy at run-time. The ACA provides approximate sum during normal operation but can provide accurate results at the cost of performance power overhead. The approximate part of ACA utilizes sub-adders to compute the partial sum as shown in Fig 7. The overall sum is extracted by concatenating all bits of least significant sub-adders and upper half of each sub-adder except least significant one. In this adder error occurs only when there is carry transmission from one partial adder to another. The addition of error detection and correction (EDC) to this approximate adder will make it as ACA. The EDC logic for this proposed adder is very simple and can be implemented by few AND gates.

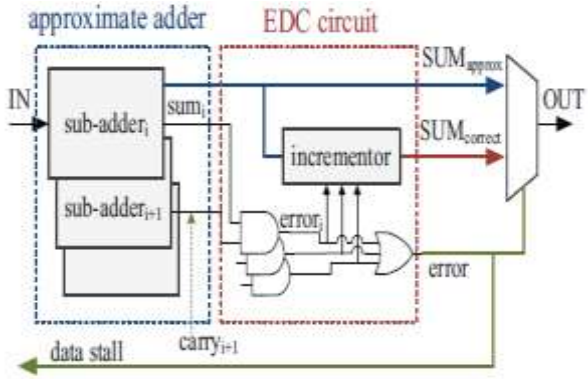

Fig. 7: ACA adder architecture

The ACA generates a carry flag when sum is incorrect. Therefore, to compute the accurate result, the error detected by the EDC will be added to the approximate part to compute the accurate sum. The approximate or accurate sum will be selected with the help of multiplexor. The prime advantage of the ACA is to provide variable accuracy output while the major drawback is its large area overhead. Therefore, if the area of the ACA if can be reduce, it will provide an adder which is good in all respects.

IV. PROPOSED ACCURACY RECONFIGURABLE ADDER ARCHITECTURE

To reduce the implementation complexity of the ACA, all the sub-adders are reduced to half size except the first full adder. The resulting proposed approximate adder architecture is shown in Fig. 8.

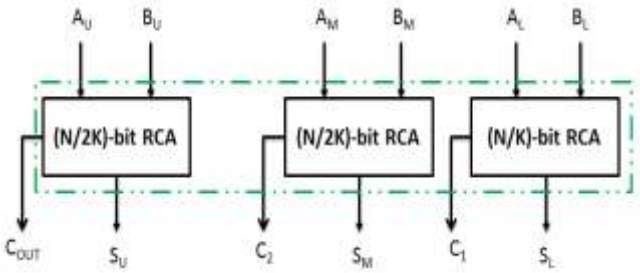

Fig. 8: Proposed approximate adder architecture

It can be seen from the block diagram that the proposed adder nearly half of the area over ACA. Further, since the remaining design is same as that of ACA, the proposed adder exhibits similar delay as that of ACA but significantly reduced power consumption due to reduced number of transistors. The proposed adder has little more error over the ACA when used in the approximate mode due to the no consideration of carry for some positions. This error can be detected and the resulting error can be added to the approximate sum which will result in accurate sum at the cost of increased delay and power.

The architecture of the proposed accuracy reconfigurable adder is shown in Fig. 9. It can be seen from the figure that additional error detection and correction logic (dotted red colour) is nothing but carry look ahead logic which detects the desired carry input. The output from this logic when added to the approximate sum produces accurate output.

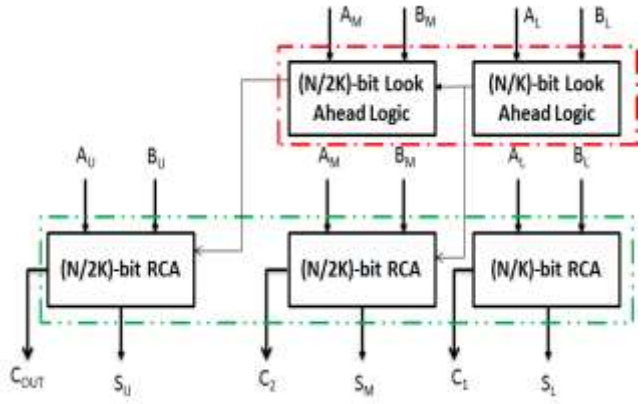

Fig. 9: Proposed accuracy reconfigurable adder

Therefore, the proposed adder can be used in both accurate and approximate mode. Since the look ahead logic requires

less number of transistor over to the same size RCA thus reduces implementation complexity over the existing accuracy configurable adder architecture. The complexities of the proposed over the existing adders are detailed in the next sub-section.

IV. EXPERIMENTAL RESULT & ANALYSIS

The quality metrics for the proposed and existing architecture are computed by implementing all designs on MATLAB and Tanner. Finally, the designs are simulated and design and quality metrics are evaluated and compared.

4.1 Design metrics on Tanner

For estimating the design metrics of proposed and all the existing adders they are implemented on the Tanner v14.1 and simulated with 45nm technology file [15]. Table 1 shows the design metric parameters for all the 8-bit conventional and approximate adders.

Table 1: Design metrics of various 8-bit adder.

Adder	#Tran	Power (mw)	Delay (ns)	PDP (nJ)
ETA-I	212	1.68	0.178	299.04
ETA-IIM	224	0.0076	0.163	1.239
ACA	336	0.0099	0.163	1.614
Prop.	224	0.0067	0.15	1.005

On comparing all the design metric of different adders through Table 3 we conclude that proposed adder requires minimum energy over ACA. Thus, we can say that proposed adder exhibits smallest delay whereas ETA-I requires minimum area over the existing adder architectures. Fig. 10 compares the area of different adder architecture where the proposed adder shows comparable area over the all existing approximate adder architectures.

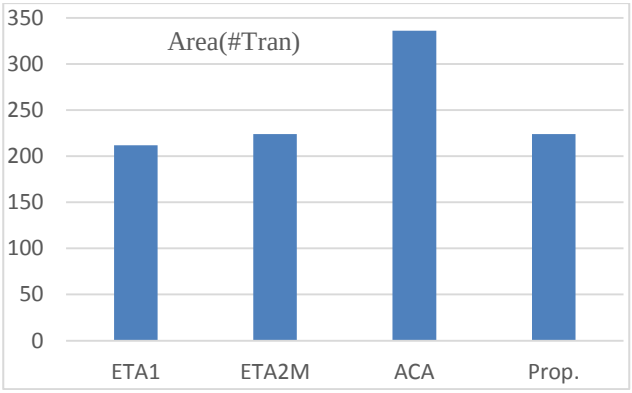

Fig. 10: Area of various 8-bit adder architectures

Similarly, Fig. 11 compares the delay of proposed adder over the different adder architecture where proposed adder exhibits smaller delay over ETA-IIM and ACA.

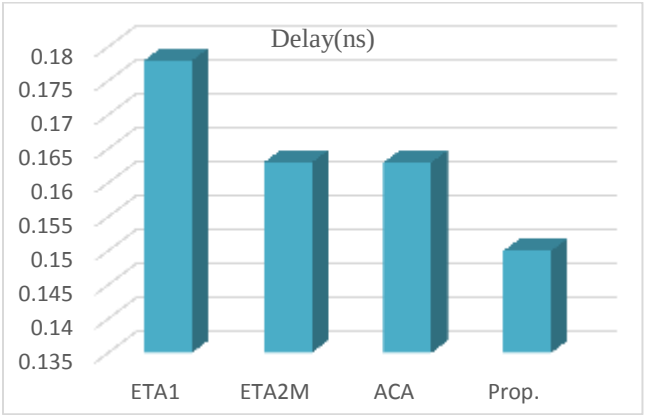

Fig. 11: Delay of 8-bit adder architectures.

Similarly, the design metrics for the 16-bit and 32-bit adders are computed as shown in Table 2 The design metrics show that proposed adder architecture requires very small area, power and delay over the existing adder architectures. The energy consumption (power delay product) is least for the proposed adder over all the existing adders.

Table 2: Design metrics of 16 and 32 bit adders

Adder		#Tran	Power (uw)	Delay (ns)	PDP (fJ)
ETA-I	**16-bit adder**	426	3.3	0.344	1.135
ETA-IIM		448	0.143	0.43	0.0615
ACA		672	0.197	0.331	0.0652
Prop.		448	0.133	0.3	0.0399
ETA-I	**32-bit adder**	854	6.31	0.678	4.2782
ETA-IIM		896	0.244	0.666	0.1461
ACA		1344	1.14	0.66	0.7592
Prop.		896	0.266	0.6	0.1596

4.1 Simulation results on MATLAB

The error metrics is shown in Table 3, which describes that 8-bit proposed adder exhibits nearly same characteristics as that of ETA-IIM and ACA under mode=0. These error metric reflect that the proposed adder can be effectively employed in the applications where ACA and the ETA-IIM can be used. Thus, proposed adder is suitable for different image and video processing applications. Similarly, the error metrics for higher bit-width adder 16-bit and 32-bit adder are extracted and compared.

Table 3: Comparison of 8-bit adder error metrics

Error Metrics	ACA			ETA-IIM	ETA-I	Prop
	m=0	m=1	m=2			
Mean	7.6	7.56	0	7.6	2.98	7.6
MSE	357.2	426.9	0	357.2	14.13	357.2
Std (σ)	18.89	20.66	0	18.89	3.76	18.89
poe	0.19	0.11	0	0.19	0	0.19
cofact	0.4	0.366	0	0.4	0.79	0.4

The error metrics of the proposed and existing adder are tabulated in Table 4. The simulation results show that ETA1 exhibits good error metrics but provides very poor design metrics. Whereas the error metrics of ETA2M is the very poor over the all existing designs.

Table 2: Error metrics of 16-bit adder.

Error Metrics	ACA			ETA-IIM	ETA-I	Prop
	m=0	m=1	m=2			
Mean	127.88	126.15	0	20448	61233	127.88
MSE	$4.79x10^5$	$5.0x10^5$	0	$2.29x10^7$	$6.32x10^8$	$4.79x10^5$
Std (σ)	692.6	707.6	0	4790	$2.5x10^4$	692.6
poe	0.057	0.03	0	0.4818	1	0.057
cofact	0.184	0.178	0	0.426	2.43	0.184

Thus, it observed from the simulation results that proposed adder provides good design metrics over all the existing adder architectures whereas the quality metrics are comparable to the accuracy configurable adder architecture. It can be observed from Table 4 that proposed adder requires least energy consumption for both 16-bit and 32-bit adder over the existing accurate and approximate adder architectures. Thus we can say proposed adder provides significant improvement in area, power, delay and PDP over all existing adders.

V. CONCLUSION

The high performance requirement by the different portable devices exhibiting multimedia applications can be achieved by designing approximate adder. This paper presents an exhaustive literature review on different kinds of approximate adder and accessed their performance in terms of area power and delay. These adders exhibit different tradeoff between these metrics.

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