Implementation of FPGA based Design for digital signal processing

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***Abstract*: Implementing hardware design in Field Programmable Gate Arrays (FPGAs) is a formidable task. There is more than one way to implement the dsp design for fft processor and digital FIR filter. Based on the design specification, careful choice of implementation method and tools can save a lot of time and work. There are toolboxes available to generate VHDL(Verilog) descriptions of the filters which reduce dramatically the time required to generate a solution. Time can be spent valuating different implementation alternatives. Proper choice of the computation algorithms can help the FPGA architecture to make it efficient in terms of speed and/or area.**

***Keywords*: Multiplier and accumulator, Booth algorithm, Booth Multiplier, Booth Wallace Multiplier, Adaptive Lattice Filter, Fir filter, Median filter, IIR filter.**

INTRODUCTION

Adaptive filters have become vastly popular in the area of digital signal processing. Adaptive direct modeling or system identification and adaptive inverse modeling or channel equalization find extensive applications in telecommunication, control system, instrumentation, power system engineering and geophysics.

Filter adds more noise to the signal; the digital filter performs noiseless mathematical operations at each intermediate step in the transform. As the digital filters have merged as a strong option for removing noise, shaping spectrum, and minimizing inter-symbol interference in communication architectures. These filters have become popular because their precise reproducibility allows design engineers to achieve performance levels that are difficult to obtain with analog filters .FIR and IIR filters are the two common filter forms.

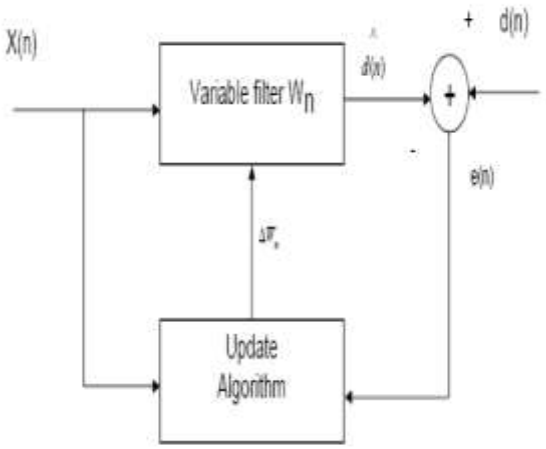
The creation and analysis of representative data can be a complex task. Most of the filter algorithms require multiplication and addition in real-time. The unit carrying out this function is called MAC (multiply accumulate). Depends on how good the MAC is, the better MAC the better performance can be obtained.

FFT architectures can be categorized as two types, the pipelined architecture and the memory based architecture. A cascade structure of FFT processor which could implement input data length alterable based on radix-16 and radix-2/4/8 mix radix algorithm. “Ping-pong” memory architecture was adopted in the design, each level need a lot of memory. Because the architecture needed more storage resources, the design need improve. After analyzing the various FFT algorithms, the paper presents a variable point FFT processor of a pipeline structure chosen the decimation –in-time FFT and 2D FFT algorithms.

In a 8 point FFT processor without pipelining it takes four clock cycles to generate the output for one set of input and in the next clock cycle the next set of input is applied for processing. Where as in pipelined FFT processor as soon as one set of input is transferred to second stage a new set of input is applied to the first stage during the same clock cycle, due to which number of clock cycles is reduced.

Adaptive Filter

An adaptive filter is a filter that adjusts its transfer function according to an optimizing algorithm. Because of the complexity of the optimizing algorithms, most adaptive filters are digital filters that perform digital signal processing and adapt their performance based on the input signal used.[1]



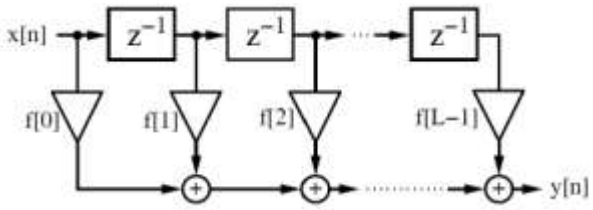
Block diagram of an Adaptive filter

Median filter

In, signal processing it is often desirable to be able to perform some kind of noise reduction on an image or signal. The median filter is a nonlinear digital filtering technique, often used to remove noise. Such noise reduction is a typical pre-processing step to improve the results of later processing (for example, edge detection on an image). Median filtering is very widely used in digital image processing because, under certain conditions, it preserves edges while removing noise [9].

FIR filter

The Lth-order LTI FIR filter is graphically interpreted in Fig.It can be seen to consist of a collection of a "tapped delay line," adders, and multipliers. One of the operands presented to each multiplier is an FIR coefficient, often referred to as a "tap weight" for obvious reasons. Historically, the FIR filter is also known by the name "transversal filter," suggesting its "tapped delay line" structure [7].

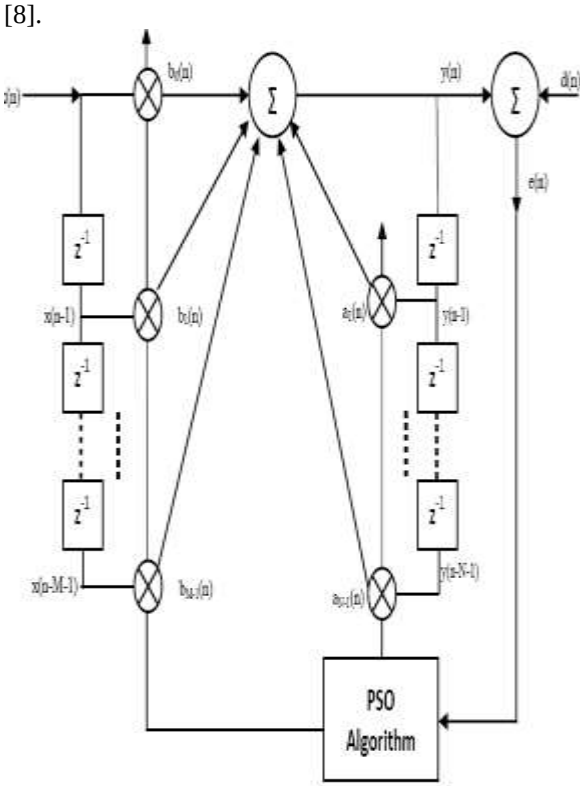


Design of FIR filter

Digital filters include infinite impulse response (IIR) digital filter and finite impulse response (FIR) digital filter. As the FIR system have a lot of good features, such as only zeros, the system stability, operation speed quickly, linear phase characteristics and design flexibility, so that FIR has been widely used in the digital audio, image processing, data transmission, biomedical and other areas. FIR filter has a variety of ways to achieve, with the processing of modem electronic technology, taking use of field programmable gate array FPGA for digital signal processing technology has made rapid development, FPGA with high integration, high speed and reliability advantages, FIR filter implementation using FPGA is becoming a trend.

IIR filter

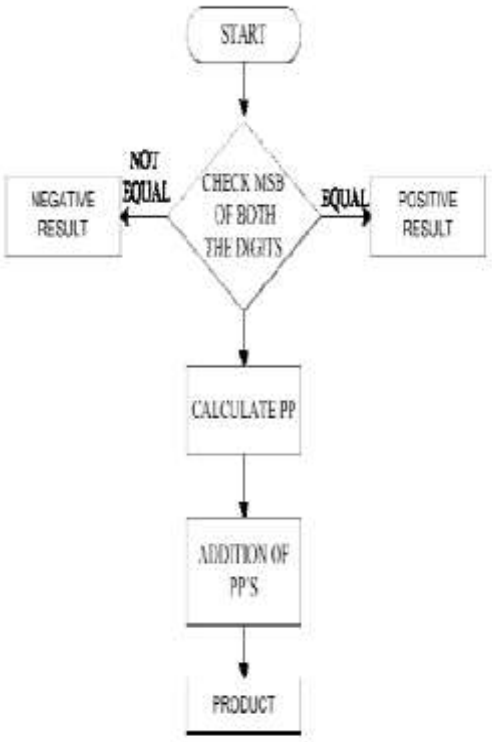
Adaptive Infinite Impulse Response (IIR) systems are used in modeling real world systems because of their reduced number of coefficients and better performance over the Finite Impulse Response (FIR) filters. Despite the fact that the digital IIR filter design is a well-researched area, major difficulties still exist in practice. This is because the error surface or the cost function of IIR filters is generally multimodal with respect to the filter coefficients. Thus, gradient-based algorithms can easily be stuck at local minima [8].



IIR filter design

MULTIPLIER AND ACCUMULATOR

A multiplier can be divided into three operational steps. The first is radix-2 Booth encoding in which partial product is generated from the multiplicand X and the multiplier Y. The second is adder array or partial product compression to add all partial products. The last is the final addition in which the process to accumulate the multiplied results is included [2].



FPGA implementation of a spectral sharpening process suitable for speech enhancement and noise reduction algorithms for digital hearing aids. [4]

Booth and Booth Wallace multiplier is used for implementing digital signal processing algorithms in hearing aids. VHDL simulation results confirm that Booth Wallace multiplier is hardware efficient and performs faster than Booth's multiplier. Booth Wallace multiplier consumes 40% less power compared to Booth multiplier.

A novel digital hearing aid using spectral sharpening filter employing booth Wallace multiplier is proposed. The results reveal that the hardware requirement for implementing hearing aid using Booth Wallace multiplier is less when compared with that of a booth multiplier [2].

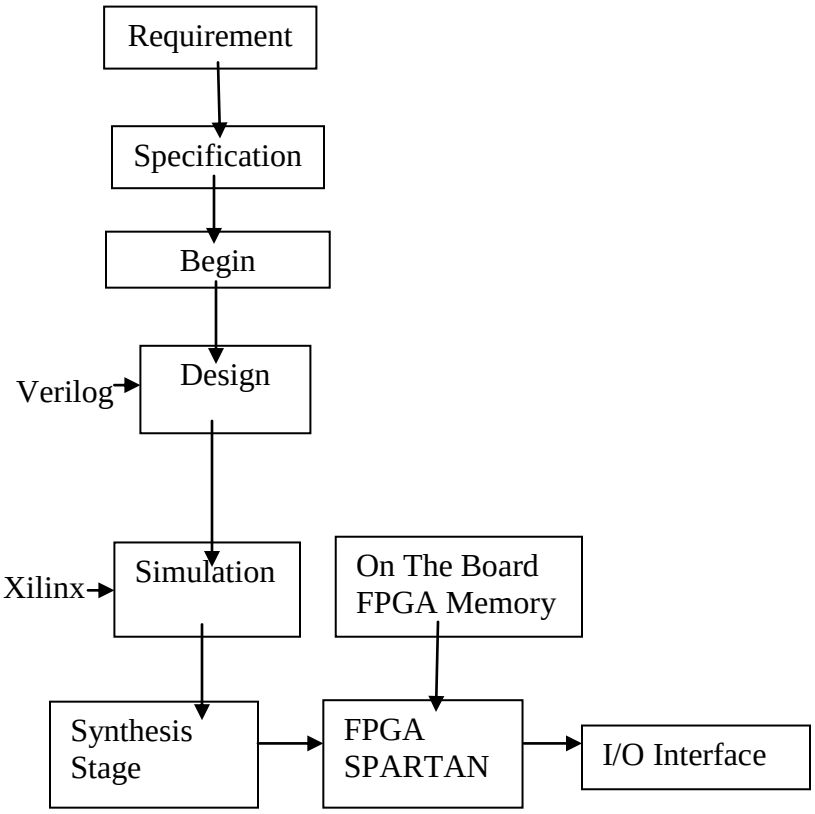
Description of Flow Chart Diagram

By gathering the requirements related to filters, MAC Units, Booth algorithm architecture, we would specify them accordingly the object so that we can begin the designing process for the Adaptive filter to making FIR, IIR & Median filters. Then after, Synthesis stage is capable of producing a wide range of resultant outputs. And finally we can check the inputs of synthesizer with the corresponding outputs of the FPGA SPARTAN.

Xilinx ISE Overview

The Integrated Software Environment (ISE™) is the Xilinx® design software suite that allows you to take your design from design entry through Xilinx device programming. The ISE Project Navigator manages and processes your design through the following steps in the ISE design flow.

RESULTS

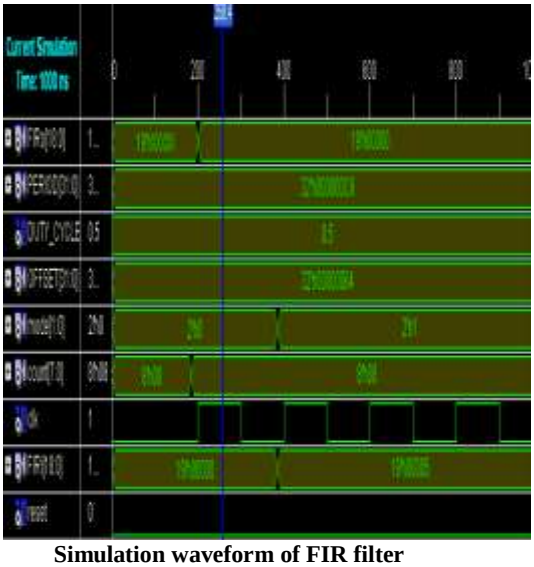


Device Utilization Summary (estimated values)		
Logic Utilization	Used	Available
Number of Slices	10	768
Number of Slice Flip Flops	16	1536
Number of 4 input LUTs	9	1536
Number of bonded IOBs	17	63
Number of GCLKs	1	8

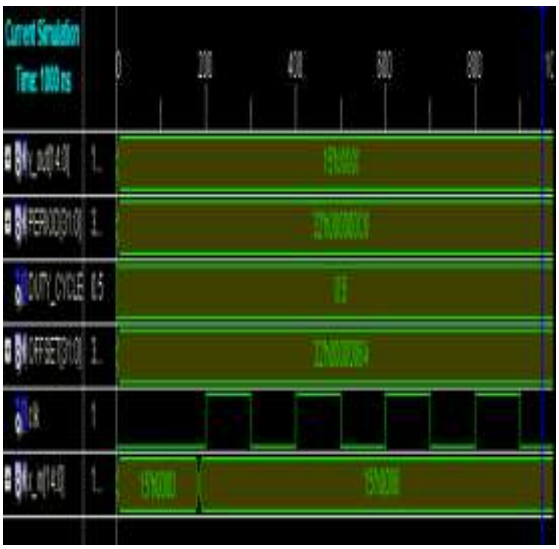
Design summary when we design FIR filter

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	17	768	2%
Number of Slice Flip Flops	30	1536	1%
Number of 4 input LUTs	27	1536	1%
Number of bonded IOBs	31	63	49%
Number of GCLKs	1	8	12%

Design summary when we design IIR filter



Simulation waveform of FIR filter



Simulation waveform of IIR filter

CONCLUSION

We have proposed and designed a verilog implementation of FPGA based digital filters which produces appreciable results because of

various benefits like low power consumption, higher efficiency, faster etc.

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