Energy Efficient DCT Architectures for Image Processing Applications: A Review

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***Abstract*— The exponential growth on the image processing applications on the portable devices demanding energy efficient signal processing. Inage compression is required to efficiently communicate and transmit huge image data over the portable mobile devices. Discrete Cosine Transform (DCT) is the most compute intensive unit in the image compression standards. The performance of the DCT significantly affects the performance of the application. Therefore, different approximate DCT architectures are developed in the literature. In this paper, an exhaustive literature review is done and then the performance of the existing DCT architectures is evaluated and compared. These existing designs are implemented and simulated with benchmark input to compute the efficacy of one over the other existing architectures. The designs are modelled on MATLAB and Tanner, simulated with benchmark inputs and then quality and design metrics are evaluated and compared.**

***Keywords*— Image Processing, Approximate Architectures, Energy Efficiency, Integrated Circuits, VLSI.**

I. Introduction

The development in the VLSI technology allowed us to implement complex functionality on the single device. This results in the several multimedia applications on the modern portable devices. The multimedia applications deal with huge data of image/video and demands energy efficient processing. The large energy consumption in these portable devices increases the failure probability which may result in device failure. For example, large data of image/video is stored in compressed form and requires image/video compression where discrete cosine transform (DCT) is prime computing block within image compression standard [1]. The high energy consumption of the DCT limits the performance of the image compression. As the portable devices exhibit limited battery size, it demands energy efficient DCT core.

The conventional approach of scaling to obtain energy-efficient design is not viable due increased process and other variation that degrades the performance of these devices significantly. Hence scaling the device dimension fails to achieve energy efficient design. Therefore, in order to design power and performance efficient VLSI architectures, an architectural or algorithmic level approach is required that can exploit the property of the application. This will result into an optimum architecture and provides improved metrics.

In the sub-nanometer designs, the process variation has become so severe that designs without considering it will fail to provide desired output. Further, addition circuit to mitigate the effect of process variation is very costly in terms of power, area and delay such that gain due scaling are less than overhead. Therefore, other design methodology is required to develop designs for the modern gadgets. There are several applications where the approximate results are acceptable such as image/video processing. The relaxation on the accuracy can be exploited to reduce the complexity of the designs [2-3].

Different efforts are given to obtain efficient DCT architecture [4-6]. The techniques such as partial computations, computation sharing, adaptive bit- width architecture, voltage over scaling etc. are some of them. An area efficient DCT architecture is proposed by Kwon et al. that reduces implementation complexity [7]. Similarly, another area and power efficient DCT architecture is presented by Park et al. in which bit-width of the high frequency computations are reduced as these computations contribute small to the overall quality [8]. Therefore, this architecture provides good design metrics with small quality degradation. The energy efficient DCT architecture can be obtained by exhibiting voltage over scaling on the non-significant coefficients which may cause timing error but will provide error of small magnitude [9]. Application of the VOS on the

Significant coefficient for further power reduction may cause large degradation in quality, if avoided. A new architecture that reduces the timing error, error which may amplify at the later stage and error of high amplitude is presented by Oranshasky et al. [10], [11]. Further, the modern VLSI designs are suffered by the process and other variations which severely degrades the performance of the DCT. A process variation aware DCT architecture is proposed by Roy et al. where design for the significant computations paths are implemented with small delay over the designs for the non-significant computation paths. Therefore, under process variations, only non-significant coefficients are affected and introduce error of small amount which does not degrade the image quality severely.

The rest of the paper first discusses different energy efficient DCT architectures and finally compares them by implementing and computing design and quality metrics.

II. Principle of DCT

This section details principle of DCT and its property followed by the DCT in matrix form, its simple architecture and 2D-DCT via 1D-DCT.

2.1 Principle of DCT

The DCT is the mathematical operation like Fourier transform and converts signal in spatial to frequency domain [1]. It is the Fourier transform where only cosine terms are considered while sine terms are omitted. DCT is nothing but a smaller version of FFT where it takes only the real part of FFT, computationally efficient over FFT, therefore, DCT is effective for image compression and, thus, much more commonly used. The mathematical expression from the 2D DCT is given below.

$$X(k_1,k_2) = \frac{2}{N} c(k_1) c(k_2) \sum_{n_1=1}^{N-1} \sum_{n_2=1}^{N-1} x_{n_1,n_2} \cos\frac{(2n_1+1)k_1\pi}{2N} \cos\frac{(2n_2+1)k_2\pi}{2N}$$

Where k1, k2 = 0, 1, N-1, c (0) = 1/p2; and c(n) = 1 for n = 0 This can be represented in a matrix form.

2.2 2D-DCT via 1D-DCT

Fig. 1 shows architecture of 2D-DCT consisting of two 1D-DCT. From the figure it can be seen that, to Obtain 2D-DCT coefficients, the transposed output from first 1D-DCT is given as input to next 1D-DCT. Therefore, only single 1D-DCT architecture has to be designed which can then be reused to compute 2D- DCT. Moreover, this approach of computing 2D-DCT requires memory to achieve transpose operation. Most of the existing DCT architecture employ this topology to achieve 2D-DCT. Thus, the most research efforts try to reduce the complexity of single 1D-DCT. This work also, tries to reduce the computational and implementation complexity of the DCT by exploiting several significant/non-significant computations.

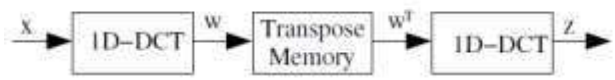

Fig. 1: 2D-DCT via 1D-DCT.

2.3 Energy compaction property of DCT

DCT is similar to FFT but can approximate a line well with fewer coefficients. Due to the higher energy compaction the value in the spatial domain can be represented by few coefficients in the DCT domain. To understand the energy compaction property of the DCT consider an example as shown in Fig. 2. It can be observed from the Figure that value of DCT coefficients becomes zero for some higher coefficients while higher coefficients in the FFT is non-zero which can be truncated. If the four coefficients of DCT and the FFT are truncated and the inverse operation is done to recover the original signal, the recovered signal from the DCT is much similar to the original over to the recovered signal from the FFT. Therefore, DCT exhibits much higher energy compaction property over the FFT and therefore used in image compression standards.

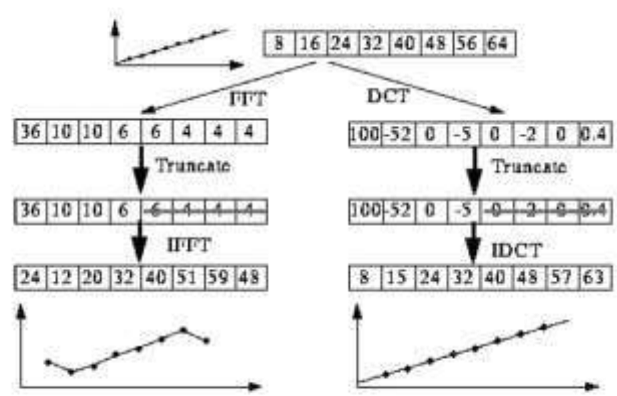

Fig. 2: Illustration of energy compaction property.

III Energy efficient DCT computation techniques This section presents different techniques to achieve energy efficient DCT architecture.

3.1 Computation Sharing Multiplication technique Kwon et al. [7] presented a computation sharing based low complexity DCT architecture. The architecture provides good quality-energy tradeoff by sharing computation multiplier in the DCT. In order to implement the hardware for the DCT architecture distributed arithmetic based computations are performed. The author modified the basic matrix of DCT such that, some constant multiplications become common between different expression and can therefore be shared. The approach can be effectively used in the other applications employing constant multiplications. For example, DCT coefficients a, b, c, d, e, f, and g with their accurate value and their proposed modified values are given in Table below.

Table 2.1: Original and modified DCT coefficients

Constant multiplie	Original values		Modified values	
	Binary	Pre-computed bank required	Modified value	Pre-computed value required
a	0011 1111	3x, 15x	0100 0000	1x
b	0011 1011	3x, 11x	0011 1100	3x
c	0011 0101	3x, 5x	0011 0100	1x, 3x
d	0010 1101	1x, 13x	0010 1100	1x, 3x
e	0010 0100	1x	0010 0100	1x
f	0001 1000	1x	0001 1000	1x
g	0000 1100	3x	0000 1100	3x

From the table it can be observed number of precomputation reduces significantly by decomposing the multiplier. The 8-bit multiplication is divided into 4-bit each, and common multiplication then shared. Moreover, to reduce the number of different multiplier required author approximated the original multiplier such that very small error provides significant reduction in the implementation complexity.

3.2 Bit-truncation technique

Park et al. [8] presented a low complexity reconfigurable DCT design that reduces power consumption. The complexity of the DCT is reduced by reducing the bit-width of the coefficient multipliers. For example, few least significant bits of the multiplier of least significant coefficient is truncated. This truncation of the LSB reduces implementation complexity with the significant improvement in the power and performance without much degradation in the output quality. Further the author presented the reconfigurable architecture such that bit-width can be varied at run-time to achieve reconfigurable DCT architecture such that quality-energy tradeoff can be achieved.

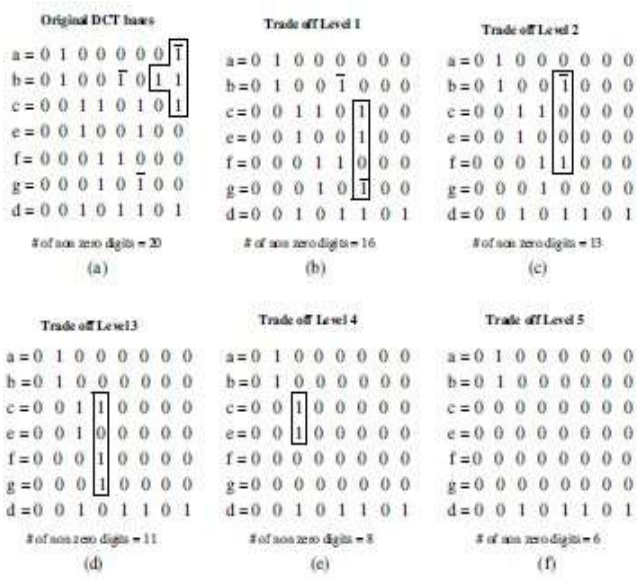

Fig. 3: Constant multiplier Approximation

From the Fig. 3, it can be observed that author tries to reduce non-zero bits in the constant multipliers. The reduction in non-zero term reduces the complexity. The number of non-zero terms in original multipliers were 20 and reduced to 6 in level 5 as shown in figure. With each new tradeoff level, the complexity reduces and power performance increases at the cost of small quality degradation.

3.3 Process aware DCT architecture

Banerjee et al. [10] Presented an architecture of process variation tolerant DCT that reduce the power consumption by applying aggressive voltage scaling. The architecture is designed to exploit the property of the DCT which says that not all the computations in DCT exhibits equal contribution to the quality. Therefore, architecture with less contribution to the quality (non-significant) are designed with longer path over the significant computing path which are designed with smaller delay. In 8-point DCT the initial coefficients are significant over the higher coefficients. Therefore, the higher frequency coefficients are designed slower.

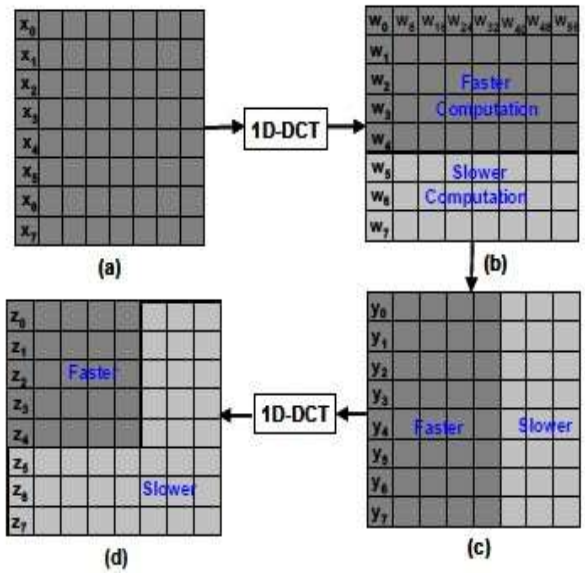

Fig. 4: Input image matrix and DCT matrices after 1st and 2nd transform.

From the Fig. 4 it can be seen that author compute first five coefficients faster over the last three non-significant coefficients. After doing 2D- DCT transformation, the resulting DCT matrix is exhibits 25 coefficients which are significant and computed faster over the rest which are non-significant. In the case of process and other variation only non-significant coefficient will show timing error which the significant coefficients computed without any timing error. Thus the design provides process variation tolerance as these variations produces very small error whereas in conventional designs significant coefficients are also shows large error and degrades the quality severely.

3.4 Timing error acceptance DCT (TEA-DCT)

An approach that early detects the timing error in the architectures due to voltage over scaling and corresponding offending technique is presented by Ku et al. [10]. The author implemented this technique in the DCT and showed a low energy inverse DCT architecture with controlled timing error. The paper presented a strategy to control the large timing error, the timing error which may get amplified at the later stage. This control logic exploits the knowledge of statistics of the operands and by rearranging the operations such that error may cancel out or diminishes but not increases.

The dynamic reordering of the reduces the possibility of timing error [11]. The author showed that numbers of error are reduced if number of addition of positive number with negative number is reduced.

This can be achieved by first adding all positive number with negative numbers and large add positive sum with negative sum. Let us consider, four numbers (-1, 1, -1, 1) have to be added and each number is represented by 16-bit. The addition of (-1, 1) plus (-1,1) will exhibits two large carry propagation over the addition of (-1, -1) plus (1, 1) which exhibits only single large carry propagation. Moreover, the carry propagation will also be of small distance over the first approach. In this way author tried to reduce the timing error.

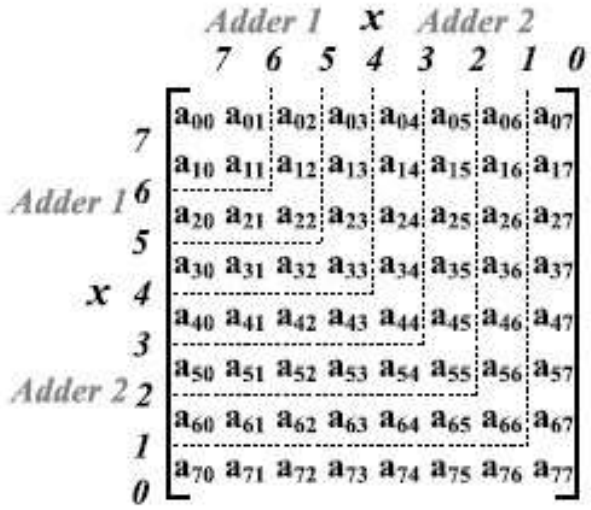

Fig. 5: Partitioning of the input matrix.

Proposed approach also partitions input matrix with different size of operator based on the significance of the coefficient. Moreover, to achieve
2D-DCT, two 1D-DCT operations are done. If error occurred in the first stage, it will get amplified in the second stage. Therefore, author showed no error on the first stage. The author achieves energy/ power efficiency by supply voltage scaling which introduces timing error. The author implemented an IDCT architecture and showed the efficacy of the proposed technique over the existing architectures.

3.5 Dynamically reconfigurable DCT architecture

An architecture of dynamically reconfigurable DCT which can be reconfigured to provide tradeoff between quality (bit-rate) and dynamic power consumption is presented by Jiang et al. [12]. In this paper author realized an optimal architecture where its performance is measured in terms of output image quality, bit-rate and dynamic power consumption. In

order to design an optimal architecture, author varied number of non-zero DCT coefficients and quality factor for quantization table. A dynamic partial reconfiguration controller is designed to achieve bit rate and dynamic power constraints. The resulting architecture as shown in Fig. 6 represent that DR controller is the key component of the reconfigurable DCT architecture.

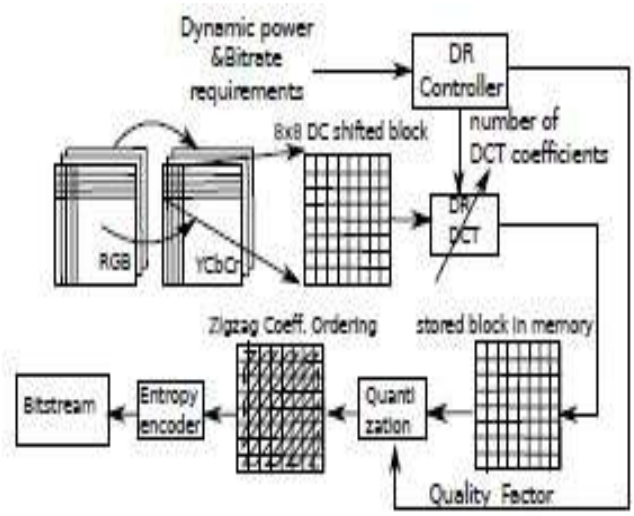

Fig. 6: Dynamic reconfigurable DCT architecture

In this DCT architecture, a constraint such as bit rate is the input used to control the complexity of the DCT. Based on the constraints, numbers of significant coefficients are computed. The 8x8 image sub-block is used to process and DCT is evaluated which is then passed to the encoder. The encoder encodes the DCT coefficients using run-length coding scheme. The design is implemented simulated with benchmark image and showed the significant improvement over the existing architectures. The proposed architecture provides reconfigurability to achieve desired quality energy tradeoff. It also exhibits significant reduced implementation complexity over the previous architectures.

IV. EXPERIMENTAL RESULT & ANALYSIS

The existing and proposed DCT architectures are implemented on Tanner and MATLAB. Tanner is used to compute design metrics whereas MATLAB is used for the computation of error metrics. To simulate the design on the Tanner, schematics of the proposed DCT is first designed on Tanner's schematic editor and net-lists of these circuits are then extracted from these schematics. These net-lists are then simulated with 45nm Predictive Technology Model file on spice simulator to achieve metrics. In the simulation area, power and delay are computed for each design.

4.1 Simulation results on Tanner

The proposed and existing DCT architectures are implemented on Tanner to evaluate the design metrics. The schematic of the proposed and existing DCT architectures are shown in Fig. 7.

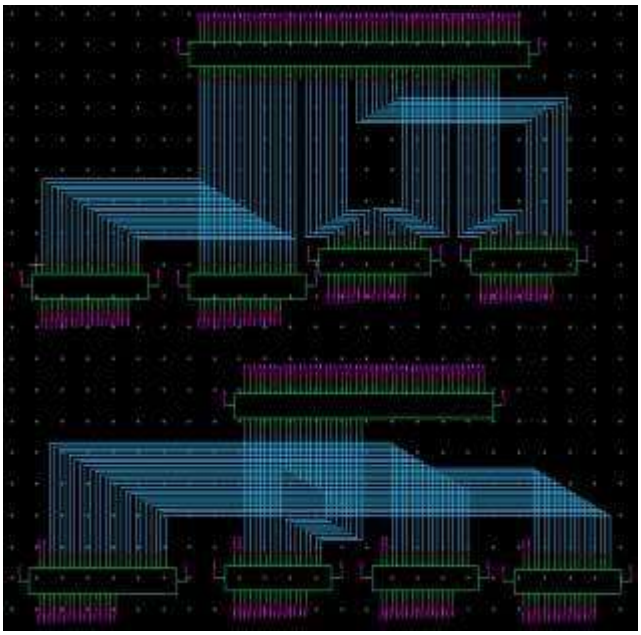

Fig. 7: Proposed energy efficient approximate DCT architecture on Tanner

The schematic of the TEA-DCT and the bit- width aware DCT (BWA-DCT) are shown in Fig. 8 and Fig. 9 respectively. It can be observed from the figure that both exhibit similar architecture except that the BWA have different bit-width operation for each coefficient whereas TEA-DCT exhibits additional logic to detect and correct the error.

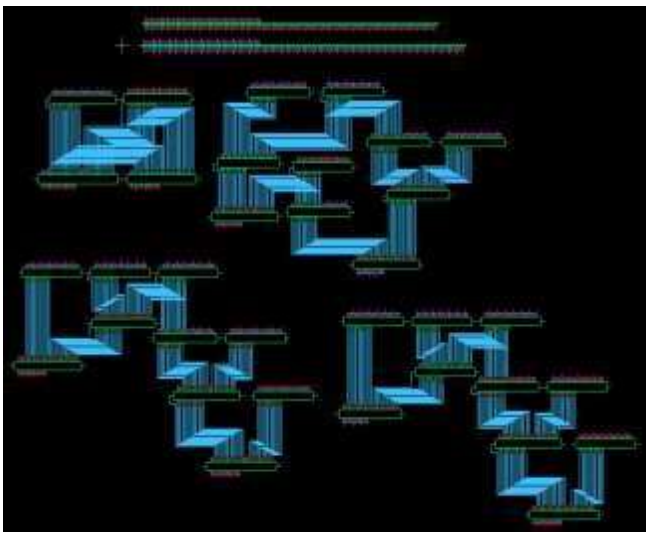

Fig. 8: Schematic of BWA-DCT on Tanner

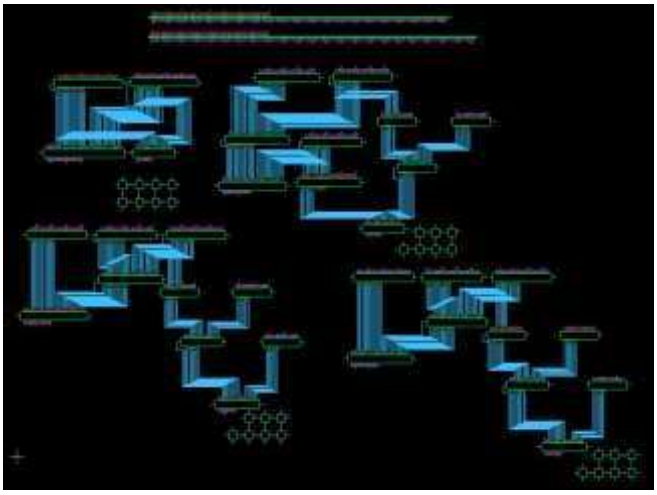

Fig. 9: Schematic of TEA-DCT on Tanner

4.1 Simulation results on MATLAB

The error metrics are evaluated by modelling the proposed and the existing adders on the MATLAB and simulating the designs with benchmark input images. The peak signal to noise ratio (PSNR) is computed and compared as shown in Table 1. The mathematical expression that computes the PSNR in
decibel is given by the equation below.

$$P\text{□□□□} = 10.\log_{10}\left(\frac{\text{□□□□}^2}{\text{□□}}\right) \quad (1)$$

Where, SigI reflects the maximum signal value which for an image is 255.

Table 1: PSNR for various DCT for varying ET.

ET	TEA-DCT	BWA-DCT	Proposed
1	28.10013	14.20352	28.08197
2	27.33193	14.03673	28.05133
3	24.99839	13.63131	27.98613
4	22.37093	13.19102	27.7231
5	19.36582	12.46905	27.29903
6	15.40877	12.2634	26.67023
7	14.10823	12.08157	26.04854
8	14.10823	11.83859	25.4486

Fig. 10 compares PSNR for the different DCT where the proposed DCT exhibits higher value of the PSNR over the existing. Fig. 11 shows the reconstructed images of different DCT architecture for varying value of error tolerance. It can be seen from the figure that proposed DCT architecture provides images of higher quality over exiting.

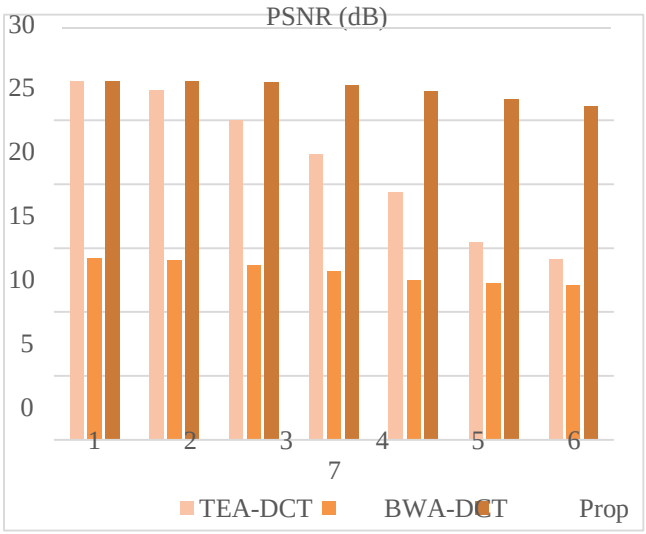

Fig. 10: PSNR of various DCT for varying ET

Fig. 11: Reconstructed benchmark image [13, 14] for varying ET using BWA-DCT (a-d), TEA-DCT (i-l), and proposed DCT (r-u) architectures.

V. CONCLUSION

The DCT is the most frequent operation in several image/video processing applications such as image compression, high performance energy efficient architecture of DCT architectures is required. This paper explored existing energy efficient DCT architectures. These architectures are evaluated and compared. It is observed that it seen that most existing design exploits the relative significant of DCT coefficients to achieve different approximation in the designs. These designs provide different tradeoff between design metrics and the quality metrics.

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