Grid Connected 13 Level Inverter for PV System Using PI Controller

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***Abstract*: Grid connected solar system uses to have converters Circuits followed by two levels: A DC/DC boosters and PWM Inverter. This combination of converters leads to decrement of Quality and efficiency of electric power, In this paper the author Propose a single phase 13- level photo voltaic (PV) inverter for Grid connected solar system with A novel pulse width-modulated (PWM) control scheme. The fast variations of solar radiation can be compensated by Digital proportional-integral controller. The inverter offers less total harmonic distortion and good power factor. The proposed system offers improved performance over five level inverters and is verified through simulation**

***Keywords:* Grid connected, photovoltaic (PV), proportional–integral (PI) current control.**

I. INTRODUCTION

The importance for sustainable energy sources has been increasing for the past two decades because of scarcities of fossil fuel and global warming. Nowadays the most admirable energy sources out all renewable energy sources are wind energy and solar energy because of advancement in power electronics techniques. Especially Solar electric energy became most popular because of advisement in manufacturing technologies and cost advantages [1] In solar energy system inverter is the main part which converts DC power obtained from solar cells in to AC power to fed in to the Grid. Nowadays Multilevel inverters are drawing attention from researchers and manufacturers due to their more benefits over conventional three level pulse width modulated inverter [PWM] inverters. They offer improved output waveforms, smaller filter size, lower EMI, lower total harmonic distortion (THD), and others [3]-[8].

The three common topologies for multilevel inverters are as follows: 1) diode clamped (neutral clamped) [9]–[11]; 2) capacitor clamped (flying capacitors) [12]–[14] and 3) cascaded H-bridge inverter [15]–[17].

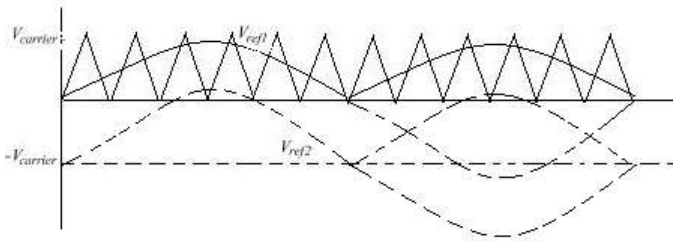

Fig.1 Carrier and Reference Signals.

In addition, several modulation and control strategies have been developed or adopted for multilevel inverters, including the following: multilevel sinusoidal (PWM), multilevel selective harmonic elimination, and space-vector modulation [3], [18].

A typical single-phase five-level inverter adopts full bridge configuration by using approximate sinusoidal modulation technique as the power circuits. The output voltage then has the following five values: zero, $+1/2V_{dc}$, V_{dc},$-1/2V_{dc}$ and $-V_{dc}$ (assuming that Vdc is the supply voltage). The harmonic components of the output voltage are determined by the carrier frequency and switching functions. Therefore, their harmonic reduction is limited to a certain degree [25].

To overcome this limitation, this paper presents a 13 level PWM inverter whose output voltage can be represented in the following 13 levels: zero, $+1/12\ V_{dc}$, $+1/6\ V_{dc}$, $+1/4\ V_{dc}$, $+1/3\ V_{dc}$, $+5/12\ V_{dc}$, $+1/2V_{dc}$, $-1/2V_{dc}$, $-5/12V_{dc}$, $-1/3V_{dc}$, $-1/4V_{dc}$, $-1/6V_{dc}$ and $-1/12V_{dc}$. As the number of output levels increases, the harmonic content can be reduced. This inverter topology uses two reference signals, instead of one reference signal, to generate PWM signals for the switches. Both the reference signals V_{ref1} and V_{ref2} are identical to each other, except for an offset value equivalent to the amplitude of the carrier signal $V_{carrier}$, as shown in Fig.1. Because the inverter is used in a PV system, a proportional–integral (PI) current control scheme is employed to keep the output current sinusoidal and to have high dynamic performance under rapidly changing atmospheric conditions and to maintain the power factor at near. unity. Simulation and experimental results are presented to validate the proposed inverter configuration.

DC-DC Boost Converter Auxiliary Circuit Full Bridge Inverter

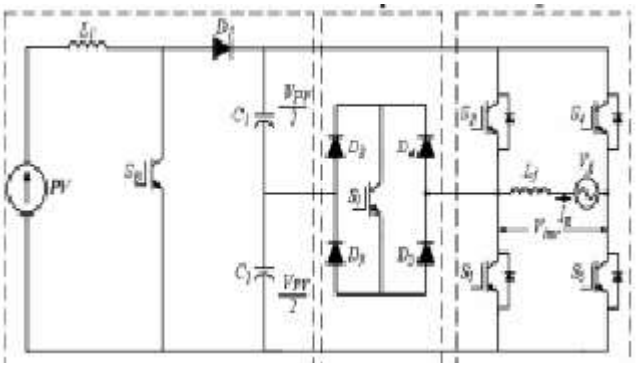

FIG.2 SINGLE PHASE INTERNAL INVERTER TOPOLOGY

DC-DC Boost Converter 13 Level Inverter

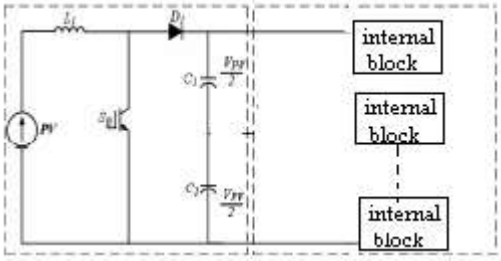

FIG.3 SINGLE-PHASE 13 LEVEL- INVERTER TOPOLOGY

2. 13-Level Inverter Topology and PWM law

The proposed single-phase 13-level inverter topology is shown in Fig. 3. The inverter adopts a full-bridge configuration with an auxiliary circuit [4]. PV arrays are connected to the inverter via a dc–dc boost converter. Because the proposed inverter is used in a grid-connected PV system, utility grid is used instead of load. The DC–DC boost converter is used to step up inverter output voltage V_{inv} to be more than *1.414* of grid voltage V_g to ensure power flow from the PV arrays into the grid [19]. A filtering inductance L_f is used to filter the current injected into the grid. The injected current must be sinusoidal with low harmonic distortion. In order to generate sinusoidal current, sinusoidal PWM is used because it is one of the most effective methods. Sinusoidal PWM is obtained by comparing a high-frequency carrier with a low-frequency sinusoid, which is the modulating or reference signal. The carrier has a constant period; therefore, the switches have constant switching frequency. The switching instant is determined from the crossing of the carrier and the modulating signal.

A. Sinusoidal PWM Law

A fundamental period in Fig. 3 consists of p pulses whose widths vary sinusoidal throughout the cycle to give the fundamental component of frequency. The basis of equivalence between the desired sinusoid and the actual pulsed waveform is taken to be volt–seconds, as shown in Fig.4, i.e., $A_{s1}=A_{p1}$ and $A_{s2} = A_{p2}$. One of these pulses, the general k_{th} pulse, is characterized in detail in Fig.5. where M is the "modulation index" and

$$M = V_m/V_s \quad (21)$$

Equation (21) can be expressed in terms of amplitude of carrier signal V_c by replacing V_s with V_c. Because, in this topology, two identical reference signals are used, $V_s=2V_c$ and $V_m = V_{ref1} = V_{ref2}$.

If M >1, higher harmonics in the phasewaveform are obtained. Therefore, M is maintained between zero and one. If the amplitude of the reference signal is increased to be higher than the amplitude of the carrier signal, i.e., M >1, this will lead to over modulation. Large values of M in sinusoidal PWM techniques lead to full over modulation [20]. Fig.4 shows the carrier and reference signals for different values of M. Equations (19) and (20) define the modulation law, which is more

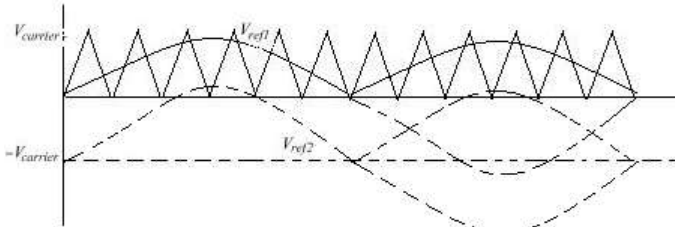

Fig. 4. Carrier and reference signals for different values of modulation index M >1

Commonly expressed in terms of δ_{1k} and δ_{2k}, by substituting from (7) and (9) to give

$$\delta_{1k} = \delta_0 [1 + M \sin(\alpha_k - \delta_0)] \quad (22)$$

$$\delta_{2k} = \delta_0 [1 + M \sin(\alpha_k + \delta_0)] \quad (23)$$

Thus, the switching angles δ_{1k} and δ_{2k} for the kth pulse can be calculated from (22) and (23) in terms of modulation index M and angles α_k and δ_0 which depend upon the fundamental frequency and frequency ratio.

B. Harmonic Spectrum of Sinusoidal PWM Waveform

The voltage harmonics produced by the sinusoidal PWM can be computed by first calculating the harmonics due to the kth pulse alone, A_{nk}, and then summating the harmonic contributions of all p pulses

$$A_{nk} = \frac{1}{2\pi} \int_{\alpha_k - 2\delta_0}^{\alpha_k + 2\delta_0} V(\theta) e^{-jn\theta} \, d\theta$$

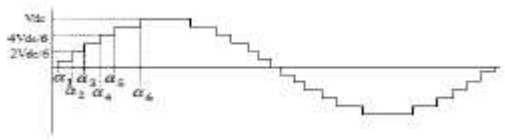

Fig.5. Ideal 13-level inverter output voltage *V*inv.

3. Operational Principle of the Proposed Inverter

Because PV arrays are used as input voltage sources, the voltage produced by the arrays is known as V_{arrays}. V_{arrays} is boosted by a DC–DC boost converter to exceed $\sqrt{2}Vg$. The voltage across the DC-bus capacitors is known as *V*pv. The operational principle of the proposed inverter is to generate 13- level output voltage, i.e., zero, +1/12 V_{dc}, +1/6 V_{dc}, +1/4 V_{dc}, +1/3 V_{dc}, +5/12 V_{dc}, +1/2 V_{dc}, -1/2V_{dc}, - 5/12V_{dc}, -1/3V_{dc}, -1/4V_{dc}, -1/6V_{dc}, and -1/12V_{dc}supply dc voltage as in Fig.5. As shown in Fig.2, an auxiliary circuit which consists of four diodes and a switch S_1 is used between the dc-bus capacitors and the full-bridge inverter. Proper switching control of the auxiliary circuit can generate half level of PV supply voltage, i.e., $+V_{pv}/2$ and $-V_{pv}/2$ [4]. Two reference signals *V*ref1 and *V*ref2 will take turns to be compared with the carrier signal at a time. If V_{ref1} exceeds the peak amplitude of the carrier signal $V_{carrier}$, V_{ref2} will be compared with the carrier signal until it reaches zero. At this point onward, V_{ref1} takes over the comparison process until it exceeds $V_{carrier}$. This will lead to a switching pattern. Switches S1–S7 will be switching at the rate of the carrier signal frequency, whereas S_4 and S_9 will operate at a frequency equivalent to the fundamental frequency.

4. Control System Implementation

The feedback controller used in this application utilizes the PI controller. As shown in Fig. 6. The current injected into the grid, also known as grid current I_g, is sensed and fed back to a comparator which compares it with the reference current I_{ref}. I_{ref} is obtained by sensing the grid voltage and converting it to reference current and multiplying it with constant *m*. This is to ensure that I_g is in phase with grid voltage V_g and always at near-unity power factor.

One of the problems in the PV generation systems is the amount of the electric power generated by solar arrays always changing with weather conditions, i.e., the intensity of the solar radiation. A maximum power point tracking (MPPT) method which has quick-response characteristics and is able to make good use of the electric power generated in any weather, is needed to solve the aforementioned problem [21]. Various MPPT control methods have been discussed in detail in [22]. Constant *m* is derived from the MPPT algorithm. The perturb-and observe algorithm is used to extract maximum power from PV arrays and deliver it to the inverter [23],[24]. The instantaneous current error is fed to a PI controller. The integral term in the PI controller improves the tracking by reducing the instantaneous error between the reference and the actual current. The resulting error signal *u* which forms V_{ref1} and V_{ref2} is compared with a triangular carrier signal, and intersections are sought to produce PWM signals for the inverter switches.

$$u(t) = K_p e(t) + K_i \int_{\tau=0}^{t} e(\tau)d\tau$$

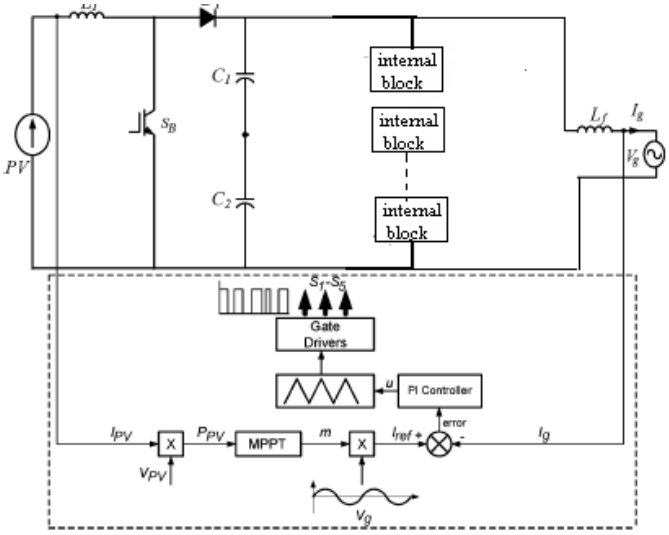

Fig. 6 . 13-level inverter with pi controller

where

$u(t)$ control signal;

$e(t)$ error signal;

t continuous-time-domain time variable;

τ calculus variable of integration;

K_p proportional-mode control gain;

K_i integral-mode control gain.

Implementing this algorithm using a DSP requires one to transform it into the discrete-time domain. Trapezoidal sum approximation is used to transform the integral term into the discrete-time domain because it is the most straightforward technique. The proportional term is directly used without approximation.

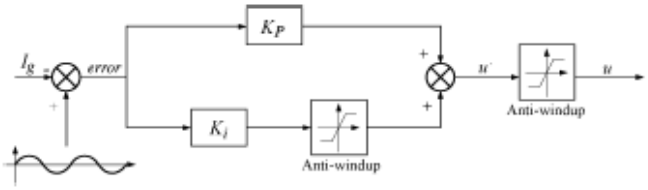

FIG.7 BLOCK DIAGRAM OF PI CONTROLLER

To eliminate the need to calculate the full summation at each time step (which would require an ever-increasing amount of computation as time goes on), the summation is expressed as a running sum

$$\text{sum}(k) = \text{sum}(k - 1) + [e(k) + e(k - 1)] \quad (33)$$

$$u(k) = K_p e(k) + K_i \text{sum}(k). \quad (34)$$

These two equations, which represent the discrete-time PI control law, are implemented in control the overall operation of the inverter.

Control signal saturation and integral-mode anti windup limiting are easily implemented.. In this work, the control signal itself takes the form of PWM outputs from the Pi controller. Therefore, the control signal is saturated at the value that corresponds to 100% duty cycle for the PWM. An undesirable side effect of saturating the controller output is the integral-mode windup. When the control output saturates, the integral-mode control term (i.e., the summation) will continue to increase but will not produce a corresponding increase in controller output (and hence will not produce any additional increase in plant response). The integral can become quite large, and it can take a long time before the controller is able to reduce it once the error signal changes sign. The effects of windup on the closed-loop output are larger transient overshoot and undershoot and longer settling times. One approach for overcoming the integral-mode windup is to simply limit in pi controller the maximum absolute value allowed for the integral, independent of the controller output saturation [25], as shown in Fig.4.

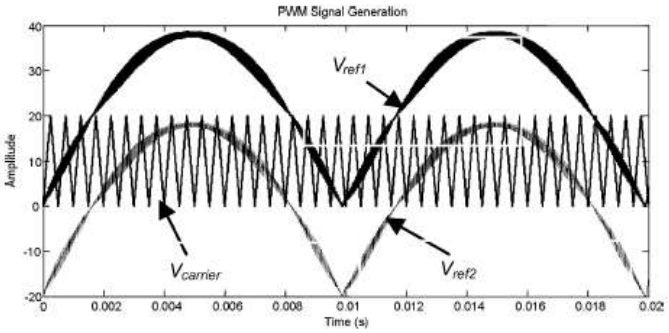

Fig.8. PWM switching strategy

5. Simulation Results

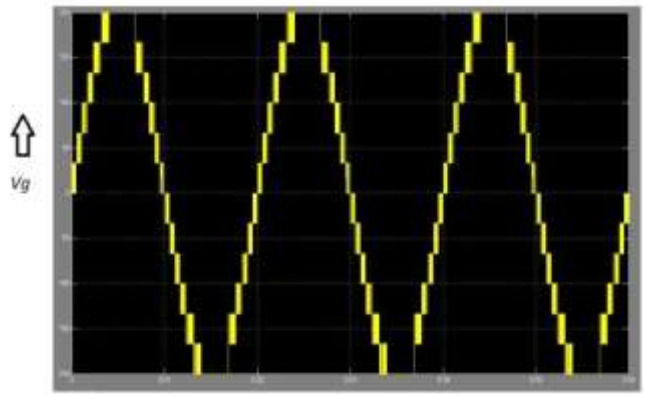

Fig.9. Inverter 13-level output voltage for M=0.2

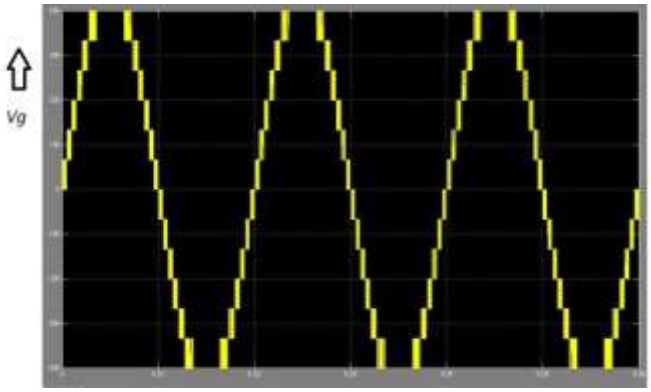

Fig.10. Inverter 13-level output voltage for M=0.8

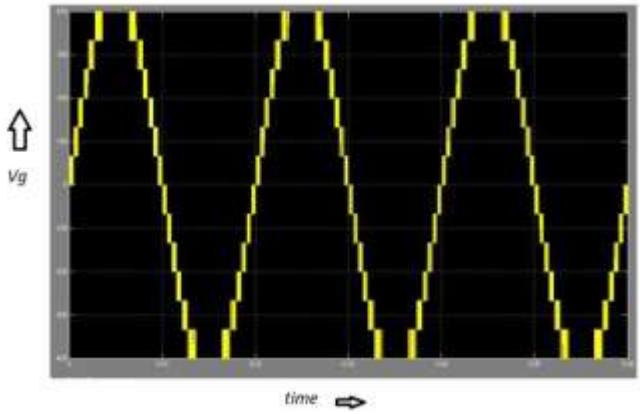

Fig.11. Inverter 13-level output voltage for M=1

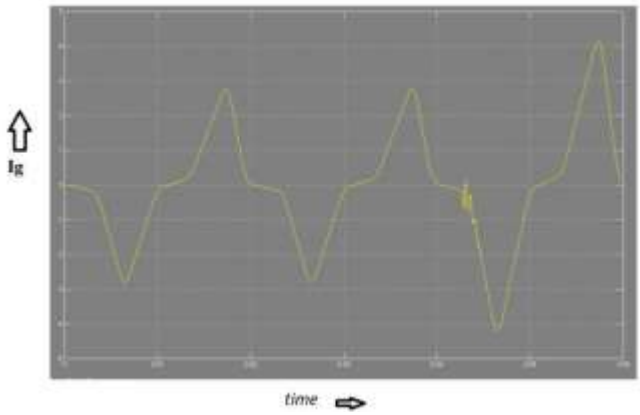

Fig.12. Inverter 13-level output current for M=0.2

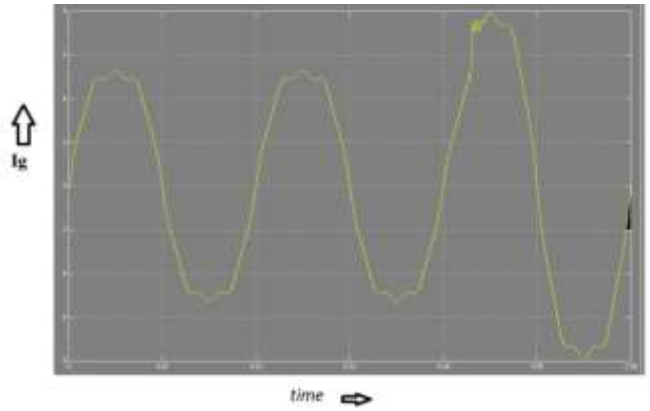

Fig.13. Inverter 13-level output current for M=0.8

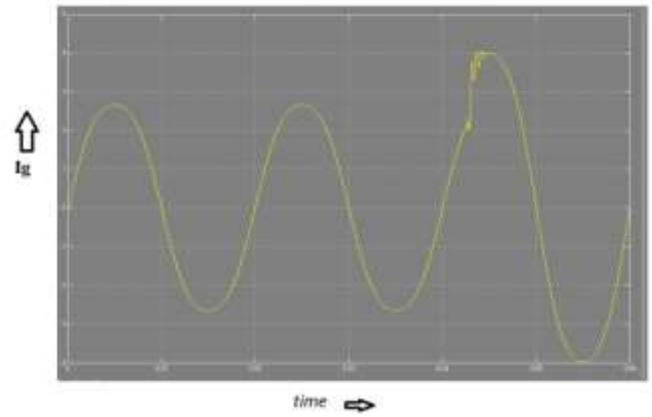

Fig.14. Inverter 13-level output current for M=1.2

A. Simulation Results

In order to verify that the proposed inverter simulations were performed by using MATLAB SIMULINK. Fig. 8 shows the PWM switching strategy used in this paper. It consists of two reference signals and a triangular carrier signal. Both the reference signals are compared with the triangular carrier signal to produce PWM switching signals for switches S_1-S_5 of inverter circuit. Note that one leg of the inverter is operating at a high switching rate equivalent to the frequency of the carrier signal, whereas the other leg is operating at the rate of fundamental frequency (i.e., 50 Hz). The switch at the auxiliary circuit S_1 also operates at the rate of the carrier signal. As mentioned earlier, the modulation index M will determine the shape of the inverter output voltage V_{inv} and the grid current I_g. Figures 9 - 14 shows V_{inv} and I_g for different values of M. The dc-bus voltage is set at 400 V ($> \sqrt{2}V_g$; in this case, V_g is 240 V) in order to inject current into the grid. Fig. 9 shows that V_{inv} is less than $\sqrt{2}V_g$ due to M being less than 0.5.

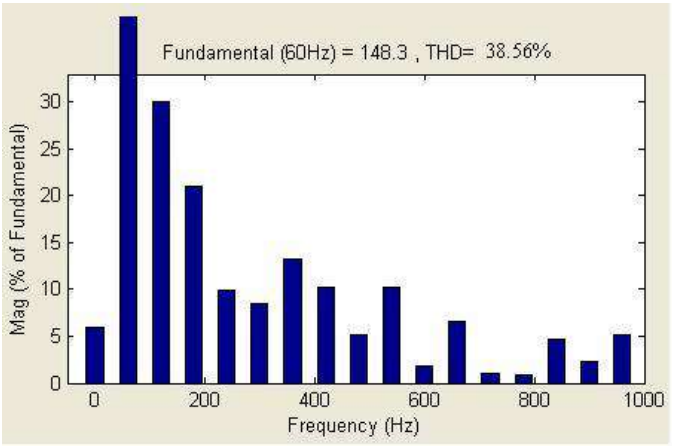

Fig.15. THD of 5-level output voltage

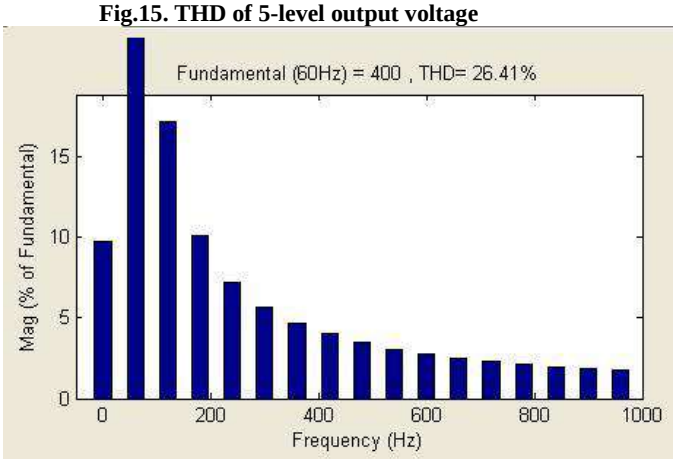

Fig.16. THD of 13-level output voltage for M=0.8

The inverter should not operate at this condition because the current will be injected from the grid into the inverter, rather than the PV system injecting the current into the grid, as shown in Fig. 12. Over modulation condition, which happens when M >1.0, is shown in Fig. 11. It has a flat top at the peak of the positive and negative cycles because both the reference signals exceed the maximum amplitude of the carrier signal. This will cause I_g to have a flat portion at the peak of the sine waveform, as shown in Fig. 14. To optimize the power transferred from PV arrays to the grid, it is recommended to operate at $0.5 < M < 1.0$. V_{inv} and I_g for optimal operating condition. As shown in fig.10,13 . I_g is almost a pure sine wave, the THD can be reduced compared with that under other values of M. To analyze the performance of the PI current control scheme, a sudden step change is applied to the simulation process. This step change is similar to real-time environment condition (for example, the sun is emerging from the clouds).

level	THD
5-level	38.56%
13-level	26.41%

6. Conclusion

This paper presented a single-phase 13 level inverter for synchronized grid pv system. It utilizes two reference signals and a carrier signals to generate PWM switching signals. The circuit topology, modulation law, and operational principle of the proposed inverter were analyzed in detail. The pi controller Is to optimize the operation of inverter. Simulation results indicate that the THD of the 13- level inverter is much lesser than that of the conventional 5- level never. Furthermore, both the grid voltage and the grid current are in phase at nearunity power factor.

References

[1]. J. M. Carrasco, L. G. Franquelo, J. T. Bialasiewicz, E. Galvan ,R. C. PortilloGuisado, M. A. M. Prats, J. I. Leon, and N.Moreno-Alfonso,"Power-electronic systems for the grid integration of renewable energy sources: A survey," *IEEE Trans. Ind. Electron.*, vol. 53, no. 4, pp. 1002–1016, Aug.
2006.

[2]. V. G. Agelidis, D. M. Baker, W. B. Lawrance, and C. V. Nayar, "A multilevel PWMinverter topology for photovoltaic applications," in *Proc.IEEE ISIE*, Guimarães, Portugal, 1997, pp. 589–594.

[3]. S. Kouro, J. Rebolledo, and J. Rodriguez, "Reduced switching frequencymodulation algorithm for high-power multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 54, no. 5, pp. 2894–2901, Oct. 2007.

[4]. S. J. Park, F. S. Kang, M. H. Lee, and C. U. Kim, "A new single-phase fivelevel PWM inverter employing a deadbeat control scheme," *IEEE Trans.Power Electron.*, vol. 18, no.
18, pp. 831–843, May 2003.

[5]. L. M. Tolbert and T. G. Habetler, "Novel multilevel inverter carrier-based PWM method," *IEEE Trans. Ind. Appl.*, vol. 35, no. 5, pp. 1098–1107, Sep./Oct. 1999.

[6]. M. Calais, L. J. Borle, and V. G. Agelidis, "Analysis of multicarrier PWM methods for a single-phase five-level inverter," in *Proc. 32nd Annu. IEEE PESC*, Jun. 17–21, 2001, vol. 3, pp. 1173–1178.

[7]. N. S. Choi, J. G. Cho, and G. H. Cho, "A general circuit topology of multilevel inverter," in *Proc. 22nd Annu. IEEE PESC*, Jun. 24–27, 1991, pp. 96–103.

[8]. G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, and G. Sciutto, "A new multilevel PWMmethod: A theoretical analysis," *IEEE Trans. Power Electron.*, vol. 7, no. 3, pp. 497–505, Jul. 1992.

[9]. A. Nabae and H. Akagi, "A new neutral-point clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523, Sep./Oct. 1981.

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