# Design & Implementation of Efficient Transreceiver System of OFDM on FPGA

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***Abstract*— This overall paper will focus on Orthogonal Frequency Division Multiplexing (OFDM) research, simulation, and efficient implementation & analysis of OFDM [2]. OFDM is especially suitable for high speed communication due to its resistance to ISI. This paper is mainly focused on the design and implementation of transmitter & receiver system for FPGA. As communication systems increase their information transfer speed, the time for each transmission necessarily becomes shorter. Since the delay time caused by multipath remains constant, ISI becomes a limitation in high-data-rate communication. OFDM avoids this problem by sending many low speed transmissions simultaneously.[3]The detailed simulation of the OFDM system with 16 QAM will be implemented .The transmitter and receiver will be implemented using FPGA .All Modules are designed using VHDL programming language**.

***Keywords*— Orthogonal Frequency Division Multiplexing (OFDM), Field Programmable Gate Array (FPGA), Hardware Description Language (HDL), Modulator, Demodulator, Fast Fourier Transform (FFT), and Signal to Noise Ratio (SNR).**

## I. INTRODUCTION

In this paper we have designed and implemented OFDM Transmitter & receiver system for FPGA. In this section a more detailed explanation of the basic blocks in the OFDM system will be provided. The theory behind all the blocks will be briefly explained and in particular, focusing in the FFT algorithm. [1]

Then, the configuration of the main blocks of the modulator and demodulator involving the FFT/IFFT blocks will be presented, explaining not only the internal configuration of the blocks but also the input and output that must be achieved. [3]

### *A. OFDM Transreceiver System Model*

The OFDM system model consist of the whole Transreceiver system according to which our project is going to work .It consist of The OFDM transmitter and Receiver .Four main criterion were used to access the performance of the OFDM system are as follows :-

(i) Tolerance to multipath delay spread
(ii) peak power clipping and
(iii) channel noise and synchronization errors.[4]

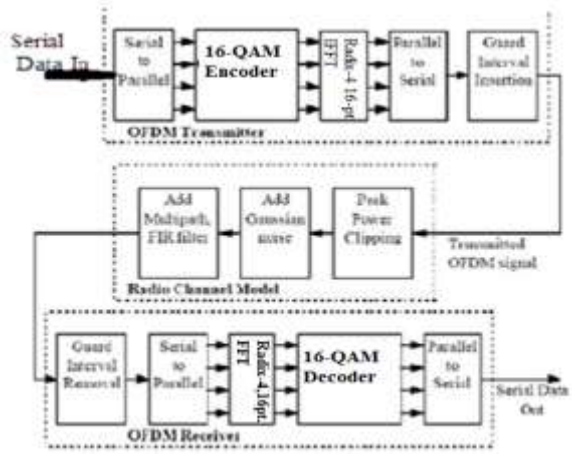



**Fig.1 Transreceiver System Model**

## II. SYSTEM ARCHITECTURE

### *A. OFDM Transmitter*

The model considered for the implementation of the OFDM transmitter is the shown in the Fig. 2 and basically consist of the following blocks:

- Serial to parallel converter.
- The FFT block.
- M-QAM decoder.
- Parallel to serial converter.[14]

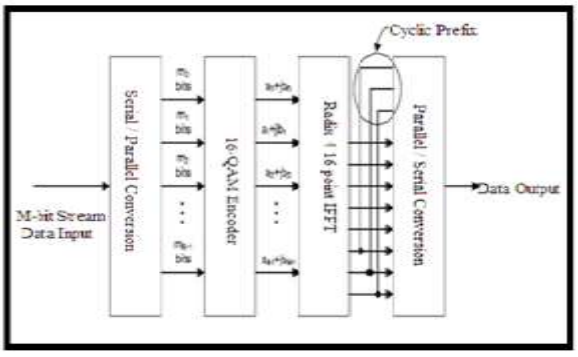



**Fig. 2 OFDM transmitter**

### *B. OFDM Receiver*

The blocks of the OFDM Receiver are shown in the Fig. 3 and those blocks are:

- Serial to parallel converter.

- The FFT block.
- M-QAM decoder.
- Parallel to serial converter.[6]

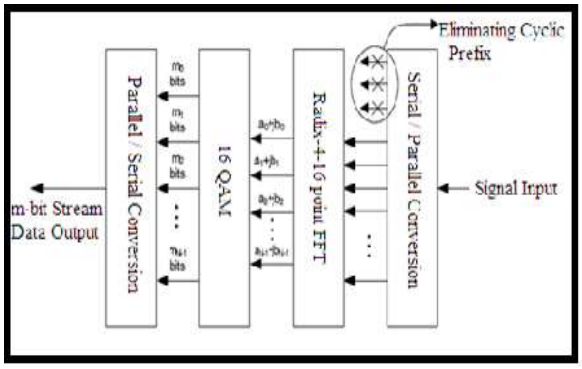



**Fig.3 OFDM receiver**

## III. DESIGN OF OFDM SYSTEM

### *A. S/P & P/S converters:-*

The aim of the serial to parallel converter is to receive the data that is going to be transmitted. The serial to parallel converter receive the M serial bits to be transmitted, and those bits will be divided into N sub-blocks of $m_n$ bits each sub-block called symbols. The amount of bit of each channel can be different Those N sub-blocks will be mapped by the constellation modulator using Gray codification, this way $a_n + jb_n$ values are obtained in the constellation of the modulator. The serial to parallel converter at the receiver has the function to receive the data that is going to be demodulated, with the same structure as it was at the transmitter. [13]

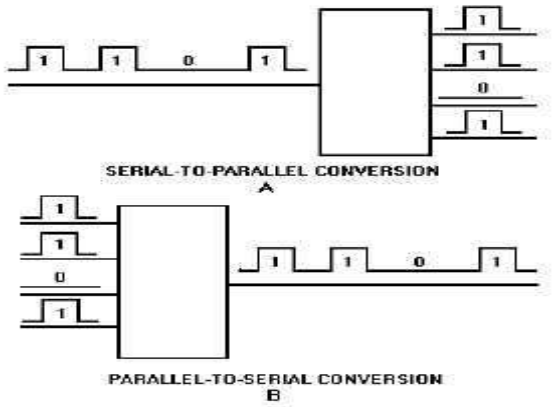



**Fig.4 S/P & P/S converters**

### *B. Constellation mapper (encoder) :-*

A constellation mapper takes a serial bit stream as its input and segments the stream into N-bit symbols, which are mapped to coordinates in the signal constellation. The coordinates of each point in a two-dimensional signal constellation represents the baseband in-phase and quadrature (I-Q) components that modulate the orthogonal IF carrier signals. Because the constellation mapper defines the shape and dimension of the signal constellation, it defines the modulation scheme that is implemented. [4].In this project 16-QAM is implemented and it is explained as above.

The types of modulations are BPSK, 4-QAM, 16-QAM, 32-QAM and 64-QAM. Depending on the modulation the amount of N bits changes: 1 bit for BPSK, 2 bits for the 4-QAM, 4 bits for 16-QAM, 5 bits for the 32-QAM and 6 bits for the 64-QAM. The modulations taken into account for this project are 16-QAM.

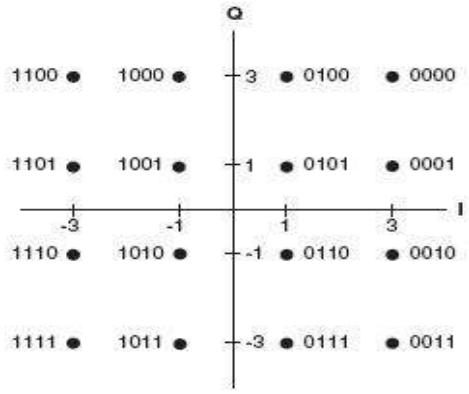



**Fig. 5 QAM constellation**

The next table shows the possible values the I,Q components can take at each modulation scheme:

**TABLE I**
**IQ values depending on the modulation**

| Modulation | I | Q |
|---|---|---|
| ***BPSK*** | {1,-1} | 0 |
| ***4-QAM*** | {1,-1} | {1,-1} |
| ***16-QAM*** | {1,3,-1-3} | {1,3,-1-3} |
| ***32-QAM*** | {1,3,5,-1-3,-5} | {1,3,5,-1-3,-5} |

### *C. Project Implemented IFFT/FFT Module:-*

For this project the IFFT/FFT module implemented is **'16-Point Radix-4 IFFT/FFT'**. It is designed as follows.

#### *1) Radix-4 FFT Algorithm :-*

Fig.6 shows an example of Radix-4 decimation in time (DIT) the method used for N=16-points FFT algorithm. As shown in FFT flow-graph inputs are in normal order while the outputs are in digit-reversed order. At input side the samples are taken from time domain which are processed with radix-4 FFT and get equivalent components in frequency domain. The numbers over flow lines indicates the twiddle factor to be multiplied with the samples [5]. The basic butterfly structure of radix-4 which have four inputs and four outputs; inputs are as

$X_0 = P_0 + W_1 P_1 + W_2 P_2 + W_3 P_3$
$X_1 = P_0 - jW_1 P_1 - W_2 P_2 + jW_3 P_3$
$X_2 = P_0 - W_1 P_1 + W_2 P_2 - W_3 P_3$
$X_3 = P_0 + jW_1 P_1 - W_2 P_2 - jW_3 P_3$

The above equations give the details of **Radix-4 FFT/IFFT.**

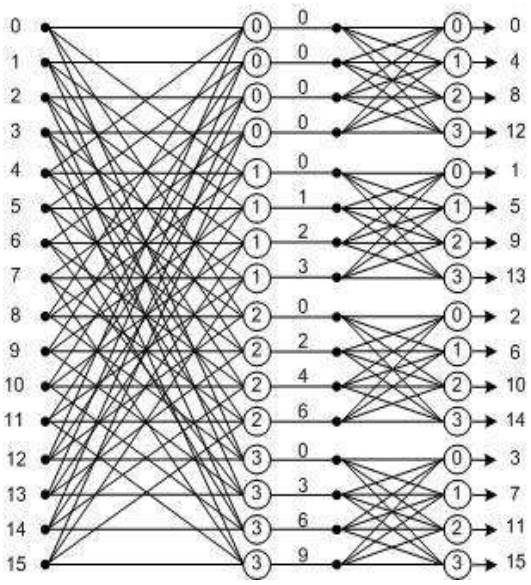


**Fig..6 16-point radix-4 DIT algorithm with input in normal order and output in digit-reversed order [8]**

## IV. RESULT AND DISCUSSION

### *A. Introduction*

Now in this point the results obtained by testing the complete implemented OFDM system will be shown. The testing can be divided into two parts, a simulation part where all testing is done on the PC and a hardware part where testing is done in the hardware. Also different systems will be analyzed on the basis of the relation between BER and SNR .The graphs will be plotted by using MATLAB coding then the better system will be designed with help of VHDL language and implemented on FPGA First we will show the results obtained from the simulation part. All these simulations, as we said in the previous chapter, have been implemented using ModelSim 6.3f. Then, in the hardware part, the different equipment used for the testing of the OFDM system will be briefly introduced, and in addition, we will show the data obtained when using the FPGA device. [3].

### *B. Analysis of system on the basis of BER and SNR by MATLAB*

The block diagram of the OFDM system using MATLAB Simulink Tools is obtained .The MATLAB coding for the relation between BER and SNR of this system is done. Also the graph between BER and SNR is plotted .The figure 7 and figure 8 shows the actual graphs in this project for BPSK and 16QAM which shows the comparative relationship between BER and SNR .From this we get the following :-

(i) The more complex modulation scheme, the larger value of BER will be evaluated

(ii)The SNR is inversely proportional to BER [4]

The figurers explain the comparative relationship between these two modulation techniques .Out of these 16-QAM is looking better. For this comparison the coding of OFDM is done in MATLAB .And the graphs are obtained between BPSK and 16-QAM .After comparison between them the efficient modulation scheme is being selected.

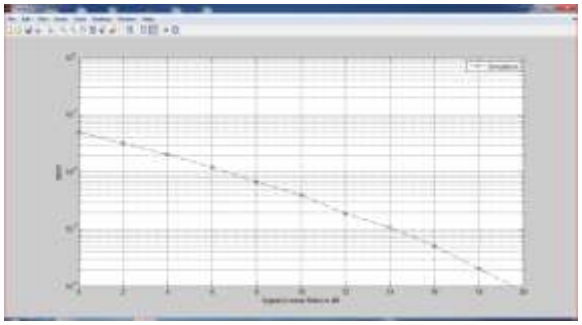


**Fig.7 The relationship between BER and SNR for BPSK system**

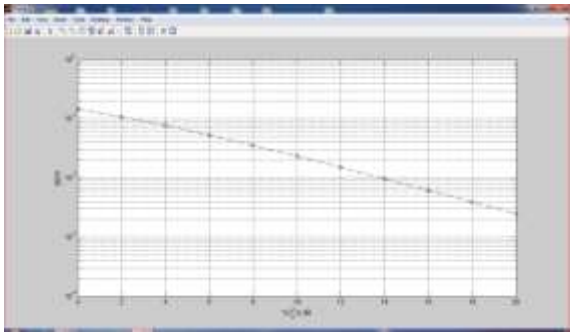


**Fig.8 Relationship between BER and SNR for QAM system**

From above figures it can be observed that the performance of 16QAM on the basis of relationship between BER and SNR is better than BPSK .So we will use 16QAM for our OFDM system.

### *C. Simulation phase*

#### *1) Output of Transmitter block*

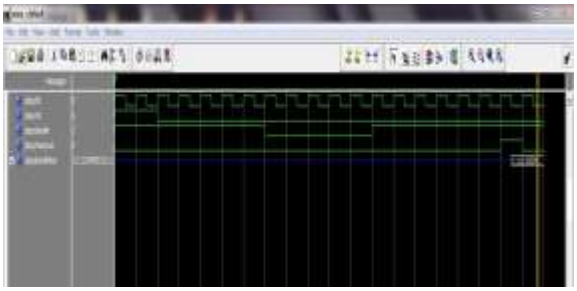


**Fig.9 Simulation result of S/P Converter**

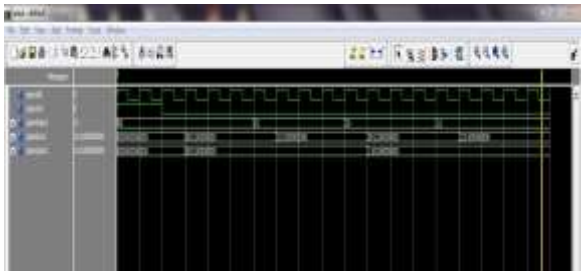


**Fig.10 Simulation result of QAM Encoder**

***2) Output of Receiver block***

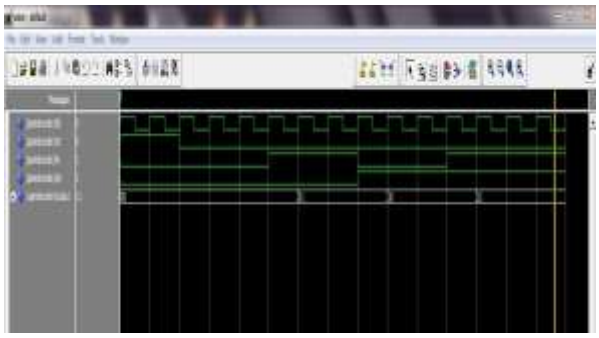


**Fig.11 Simulation result of QAM Decoder**

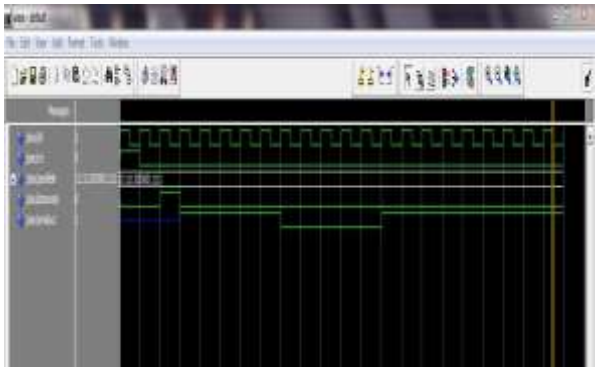


**Fig.12 Simulation result of P/S Converter**

***3. Output of Overall Transmitter & Receiver Block***

**Fig.13 Simulation result of Overall Transmitter Block**

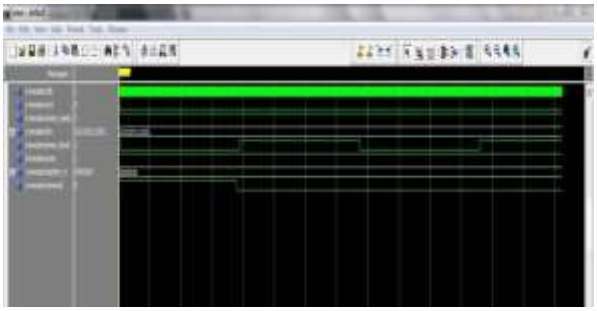


**Fig.14 Simulation result of Overall Receiver Block.**

***D. Synthesis phase***


**Fig.15 Output of Synthesis phase on FPGA Kit**

Device Utilization Summary

| Logic Utilization | Used | Available | Utilization | Note(s) |
|---|---|---|---|---|
| Number of Slice Flip Flops | 48 | 9,312 | 1% | |
| Number of 4 input LUTs | 96 | 9,312 | 1% | |
| Number of occupied Slices | 51 | 4,656 | 1% | |
| Number of Slices containing only related logic | 51 | 51 | 100% | |
| Number of Slices containing unrelated logic | 0 | 51 | 0% | |
| Total Number of 4 input LUTs | 64 | 9,312 | 1% | |
| Number used as logic | 96 | | | |
| Number used as a route-thru | 0 | | | |
| Number of bonded IOBs | 10 | 232 | 4% | |
| Number of BUFGMUXs | 1 | 24 | 4% | |
| Average Fanout of Non-Clock Nets | 2.71 | | | |

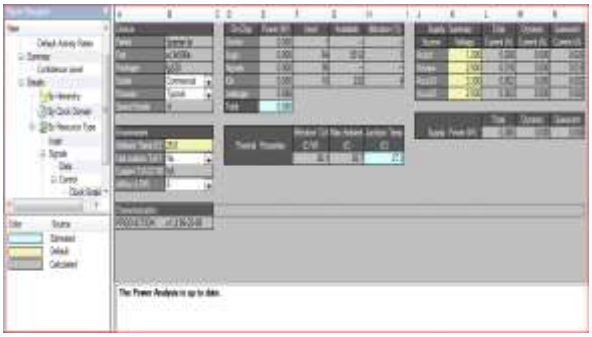
**Fig.16 Devise Utilization summary**

```
Timing Summary:
---------------
Speed Grade: -4

   Minimum period: 5.418ns (Maximum Frequency: 184.570MHz)
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: 6.283ns
   Maximum combinational path delay: No path found

Timing Detail:
--------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 5.418ns (frequency: 184.570MHz)
  Total number of paths / destination ports: 991 / 86
-------------------------------------------------------------------------
Delay:               5.418ns (Levels of Logic = 3)
  Source:            ofdm_1/offt_control_1/counter_1/count_aux_5 (FF)
  Destination:       ofdm_1/offt_control_1/counter_1/count_aux_6 (FF)
  Source Clock:      clk rising
  Destination Clock: clk rising
```

**Fig. 17 Timing Report Summary**

**TABLE II**
**POWER ANALYSIS**



***E. Performance Comparison of previous papers:-***

**TABLE III**
**PERFORMANCE COMPARISON OF PREVIOUS PAPERS:-**

| Sr. No. | Parameters | Previous | This Project |
|---|---|---|---|
| 1 | No of cycles to perform | 16 cycles | One cycle |
| 2 | Modulation | BPSK | 16-QAM |
| 3 | BER | High | Low |
| 4 | SNR | Low | High |
| 5 | Power Consumption | High | Low up to 0.088 W |
| 6 | Type of input given | Analog so A/D converter is required | Direct digital input is given .So A/D converter is not required |
| 7 | Delay | 63.543ns[7] | 5.418ns |

## V. CONCLUSION

We are expecting that the simulations will work out well and follow closely the theoretical results. The following conclusions have been asserted during the realization of this project:-

[1]. VHDL is programming language that has been some particularities , one of this particularities is that during the execution of the code most of the parts are not executed sequentially , are executed in a concurrent way .
[2]. IFFT/FFT Xilinx blocks are very sensitive to delays and input data format .The input data to the FFT block should arrive two clock cycles after the start signal is assigned to the block.
[3]. Some elements in the implementation schemes introduce a little bit of distortion but the obtained result from the simulation phase fits the theoretically expected result.
[4]. The result obtained in the hardware phase corresponds to the result obtained in the Simulation phase.

## VI. APPLICATIONS

[1]. OFDM forms the basis for the Digital Audio Broadcasting (DAB) standard in the European market .OFDM modulation is presently used in a no. of commercial wired and wireless applications .
[2]. In Digital Video Broadcasting (DVB) .It is a standard for broadcasting Digital Digital Television over satellite , cables and through terrestrial (wireless) transmission .[12]
[3]. The OFDM based multiple access technology OFDMA is also used in several 4G and pre-4G cellular networks and mobile broadcast standard

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