Noise Tolerant Dynamic Logic Design Techniques: A Survey

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***Abstract*— The limitation of the dynamic logic is the reduced noise immunity compared to the CMOS logic. Moreover, this noise immunity is further degrading with each technology due to scaling of the devices. Hence, technique is required to improve the noise immunity of the dynamic logic so that bulkier CMOS circuits can be replaced by the smaller dynamic circuits. This will result in significant reduction in the cost of device and simultaneously improve the performance of the device. This work explores the existing noise immunity techniques. In order to evaluate the effectiveness of these techniques, all these techniques are implemented in Tanner and extracted netlist is simulated with 45nm PTM technology node. The simulation results using TSPICE shows merits and demerits of each technique so that they can be effectively utilized in different applications.**

***Keywords*— Dynamic Logic, Noise Tolerant Logic, Noise Margin, Noise Immunity.**

I. INTRODUCTION

The recent exploration of the portable devices is posing severe challenges to the VLSI designer by requiring high performance energy efficient circuits. Different circuit and architectural approaches are used to improve the performance of the VLSI designs where the dynamic logic has shown it pivotal role [1]. The dynamic logic especially in case of large fan-in circuits improves the performance significantly. The principle for this high performance in dynamic logic is the due to the storing ability of the node even after removal of the supply. These nodes exhibit capacitance due to pn junction and oxide layer. These internal nodes that hold the charge are also known as soft nodes [2]. However, these stored charges at the soft nodes gradually leaks away after some time due to charge sharing problem and sub-threshold leakage current [3]. The major drawback of the dynamic logic is its poor noise immunity which further reduces with each scaled technology due to reduced threshold voltage. Therefore, noise tolerant improvement techniques are required to improve the robustness of dynamic logic.

Significant work has been reported in the literature to achieve high noise immune dynamic logic [4]. From the traditional approach of simple keeper logic and pre-charging internal node to high performance delayed logic, conditional clocking etc. A keeper transistor [5] is a weak transistor which supplies small amount of current to the dynamic node of the circuit. PMOS transistor's base is tied to the ground and is therefore always on. This is advantageous as the keeper makes up for the loss of charges at the dynamic node during evaluation phase and increases the noise tolerance of the circuit. However, it creates a direct DC path through the PDN and thus increases the DC power consumption of the circuit. Sometimes, the gate of the keeper is connected to the output of the circuit as feedback network to prevent a direct DC path through PDN to ground. Whenever the internal node of the circuit Qint is high, the keeper transistor is turned on and thus maintains the required charge level which otherwise reduces due to charge sharing problem.

The conditional clocking technique is proposed by Mazumdar et al [6], which comprises of two transistors M1 and M3 and an AND gate to conditionally clock the lowermost transistor MN2. The delayed logic comprises of an additional delay circuitry which provides sufficient delay between CLK and DCLK signals. MN1 has been used as a stacking transistor and no input or clock signals have been used to pre-charge any internal node in order to avoid additional capacitive loads. During pre-charge phase, the dynamic node is charged to logic high. DCLK remains low in stage I and transistor MP1 is on and MN1 is off which prevents the charge sharing at this stage. In stage II, CLK goes high turning the transistor MN1 on which initiates the evaluation phase. However, the DCLK signal is still low at this stage which keeps the transistor MN2 off ensuring that the charge at dynamic node is maintained. The rest of the paper is organized as follows:

Section II, provides review on dynamic logic and the problem of the charge sharing whereas the different noise immunity techniques are discussed in Section III. Section IV provides comparative analysis of different existing noise immunity techniques using simulation. Finally, Section V concludes the paper.

II. DYNAMIC LOGIC AND ITS NOISE TOLERANCE

This section provides detailed analysis of different dynamic logic design approaches and their noise immunity.

A. Design and Challenges of Dynamic Logic

The characteristics of static logic circuit is defined by the steady state behavior of simple NMOS and PMOS devices i.e., the required output logic level entirely depends on their steady state operating points. Also, the presence of comparatively large capacitance at the output node due the use of PMOS devices in the pull-up network as in the pull-down network increases the charging and discharging time of the output node. Large number of transistors results in consumption of more silicon area in static CMOS circuits. Also, it provides certain time delay which in-turn limits the performance of the circuit in terms of speed and in some cases even consumes more power. On the other hand, dynamic CMOS logic circuits [2] offer significant advantages as compared to their static counterparts. The generalized architecture of the dynamic logic is shown in Fig. 1

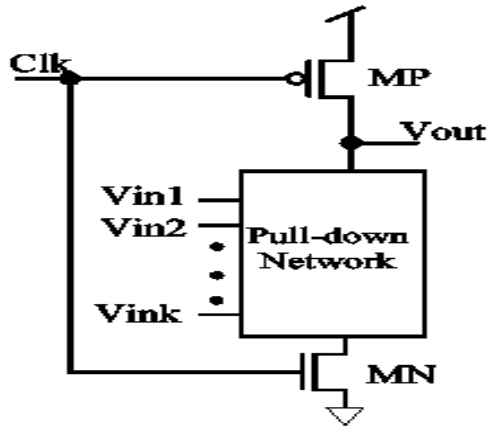

Fig. 1: Circuit diagram of dynamic logic

It can be observed from the figure that difference between static and dynamic logic architecture lies in pull-up logic where in static logic it is driven by the expression while in dynamic logic it is driven by the clock.

Dynamic logic operation [1], [2] is based on first pre-charging the internal node and then subsequently evaluating the node depending on the combination of the inputs applied. These operations of pre-charging and evaluating the output node are synchronized by a single clock signal, which drives single PMOS and single NMOS transistor in the logic structure as shown in Fig. 2. Pre-charging the output node starts when the clock signal is low which ensures that PMOS transistor is on and NMOS transistor is OFF. This stores logic '1' at the output node. However, evaluation starts when the clock signal is high, thereby making the PMOS transistor OFF and NMOS transistor ON. During evaluation phase, the output node may remain either at logic '1' or may discharge to logic '0' depending on the input combination.

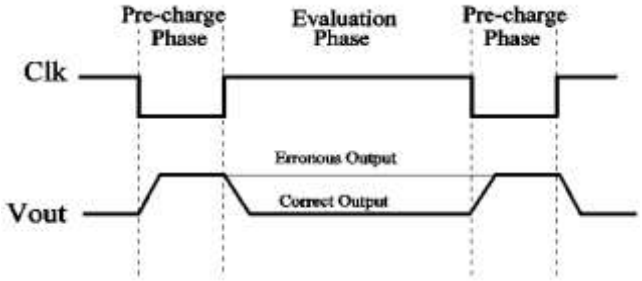

Fig. 2: Working principle of dynamic logic

Dynamic logic exploits the charge storage capability of the CMOS devices even after removal of the power supply. The charge storage phenomena exist primarily due to various capacitances present in the internal nodes of the circuit. However, these stored charges at the internal nodes gradually leaks away after some time due to charge sharing and sub-threshold leakage current. Various techniques have been proposed and effectively utilized to prevent these stored charges from leaking away to drive the circuits at the next stage.

Further, due to the rapid scaling of CMOS devices, threshold voltage is also scaling with the supply voltage. This is a severe concern as the reduction in threshold voltage directly affects the noise immunity of the circuit more in dynamic logic. This is due to the fact that the switching threshold depends on the threshold voltage (Vth) of the MOS transistors in the pull down network (PDN) as compared to Vdd/2 in the static circuit. In other words, the noise margin of the dynamic logic reduces significantly which in turn degrades the faithful operation of the circuit.

B. Domino Logic

The addition of a static inverter at output node of simple dynamic CMOS logic as shown in Fig. 3 makes it suitable for practical multistage applications and is known as Domino CMOS logic [2].

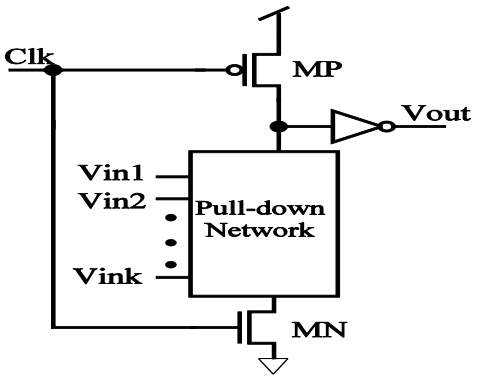

Fig. 3: Domino CMOS Logic

In the domino logic, Pre-charge mode starts when the clock signal is low and at this time the output node is pre-charged to logic high which in turn makes the output of the inverter (buffer) low. At the beginning of the evaluation phase, the clock signal goes high which gives two possibilities: the output node is either discharged to a low logic level via the NMOS circuitry, or it maintains its high logic level depending on the available input combinations. Therefore, the inverter can at the most make only one transition i.e. from logic 0 to logic 1 during the evaluation phase. This property of the circuit makes it suitable for multistage operation whereby all the input transistors of the subsequent stages are turned off during the pre-charge phase as the inverter output is logic 0 during that phase.

Limitations of domino CMOS logic includes, 1) It can only be used to implement non-inverting structures and if required, inversion needs to be carried out by using conventional CMOS logic and 2) charge sharing between the intermediate nodes of NMOS logic block and the output node may cause erroneous output during evaluation phase. Charge sharing is a noise that affects the performance of dynamic CMOS logic circuits as explained in the next section.

C. Charge Sharing

The noise that occurs due to the redistribution of charge present at the output node to some intermediate node within the PDN. This redistribution of the charge reduces the amount of charge at the output node which in-turn reduces the voltage level and node may false change its state [2].

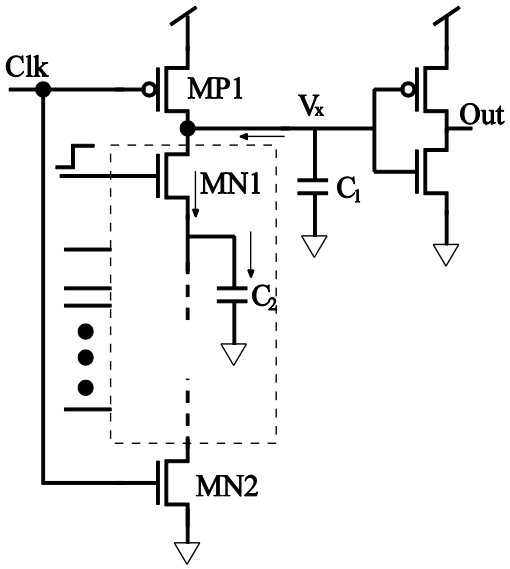

Fig. 4: Illustration of charge sharing phenomena

Consider a domino CMOS logic gate as shown in the Fig. 4, here node C2 is comparable to node C1 capacitance in size. Initial conditions are assumed to at low logic levels and the initial value of C1 capacitance is 0V. The output node C1 is pre-charged to Vdd via PMOS transistor. The evaluation phase begins when the clock goes high and if the input to NMOS connected to the output node in the pull-down network goes high as shown in Fig. 4, the charge accumulated at node C1 during the pre-charge phase gets shared by C2 which leads to the phenomenon famously known as charge sharing. Therefore, after charge sharing, the output node voltage becomes:

$$V_x = V_{dd} * \left[{}^{C_1}/_{C_1 + C_2} \right] \quad (1)$$

$$= {}^{V_{dd}}/_{(1 + {}^{C_2}/_{C_1})} \quad (2)$$

In case C1 = C2, the voltage at output node becomes Vdd/2 and unless the switching threshold at C1 is less than Vdd/2, the output of the inverter ahead will inadvertently switch to logic high, producing a logic error. This puts a restriction to keep the capacitance C2 as smaller as possible than C1.

III. NOISE IMMUNITY TECHNIQUES

This section discusses different noise immunity circuits in detail starting from simple keeper logic through to the twin transistor technique.

A. Keeper Logic

Massimo et al. [5] presented a simple logic that reduces the delay variations in the domino logic as shown in Fig. 5. Since it is observed there is feedback loop formed by keeper transistor where that inverter of the domino logic is responsible for the delay variations. The proposed technique is based on the technique to reduce the loop gain while maintaining the keeper ratio which in turn reduces the delay variations. This technique guarantee that it will maintains the noise immunity while reducing the delay variability. It is observed from the simulation results that the delay variations reduce by 50% with keeper logic insertion without penalty on area, power and delay metrics. Thus, it can be effectively utilized to the performance of the dynamic logic.

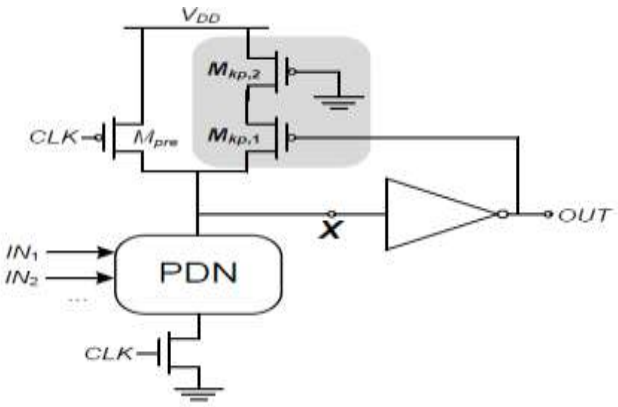

Fig. 5: Reduced delay variation keeper topology.

B. Conditional clocking Technique

Mazumdar et al. [6] presented a new noise tolerant dynamic logic technique that reduces the average noise threshold energy and delay normalized noise threshold energy significantly. In the proposed technique two MOSFETs (M2 and M3) with a AND gate is used as shown in Fig. 6. This circuit improves the noise immunity in three ways namely stacking, raising source voltage and conditional clocking. From the Figure it can be seen that the circuit exhibits transistors in stacking and further there is raise in the source potential of the M1 due to addition of transistor M2. Further the conditional clocking is achieved by having AND gate which in turn reduces the evaluation time. Thus significantly improves the noise immunity. The design is implemented and simulated where the simulation results show that this technique increases the noise immunity even at scaled supply voltage where the other noise immunity circuits fail. This technique improves the noise immunity by 18% over the mirror technique in terms of noise tolerance.

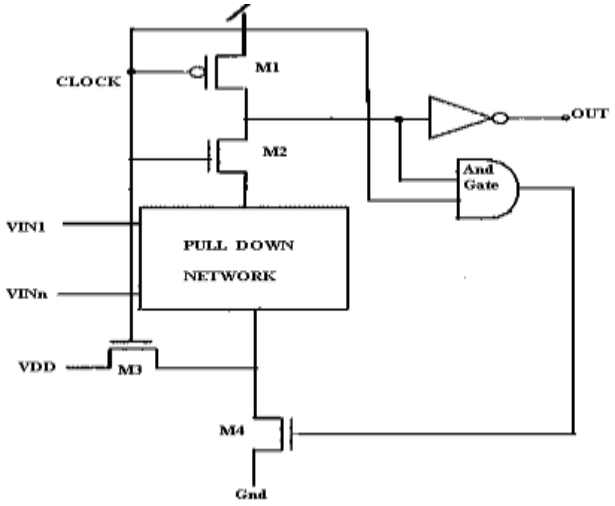

Fig. 6: Conditional Clocking Technique

C. Mendoza Technique

Mendoza et al. [7] introduces a new noise tolerance improvement technique as shown in Fig. 7 which improves the noise immunity of the TSPC and domino logic significantly. In this diagram an NMOS is inserted between pre-charge transistor and pull-down network. This transistor driven by the delayed clock which is generated by considering a chain of inverter (three cascaded connected inverters). Moreover, a PMOS transistor MP2 is added between delay clock input and the pull-down network. This PMOS is driven by the clock supply.

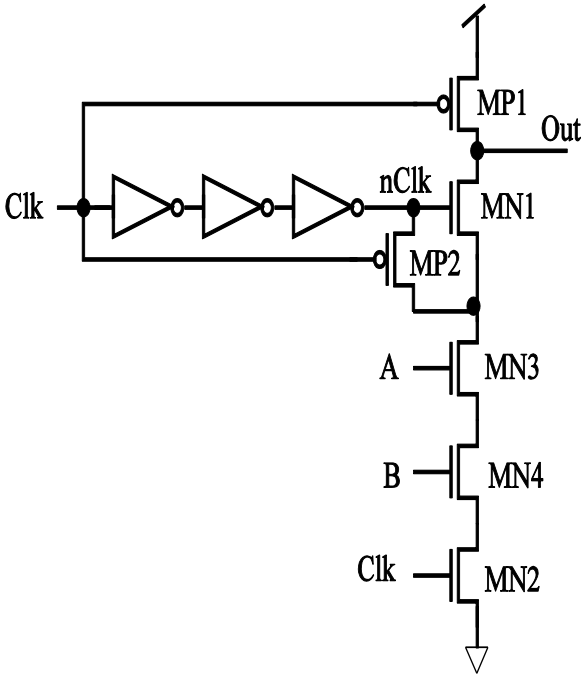

Fig. 7: Mendoza Technique

The working of this technique can be understood by the diagram as shown in Fig. 7. The circuit operates in four stages. In the first stage, the clock cycle is zero and transistors MP1, MP2 and MN1 are in ON state while MN2 will be in OFF state. This will result in pre-charging of output node.

D. Mirror Technique

Wang [8] presented that two identical NMOS circuits in series are used for evaluation and both these circuits receive the same set of inputs as shown in fig. 8. An additional transistor M3, connected in between the identical nets, is driven by the output node of the circuit. Transistor M1 charges the output node to logic high during the pre-charge phase. This results in charging the common node V_X to value $V_{DD} - V_{tn}$.

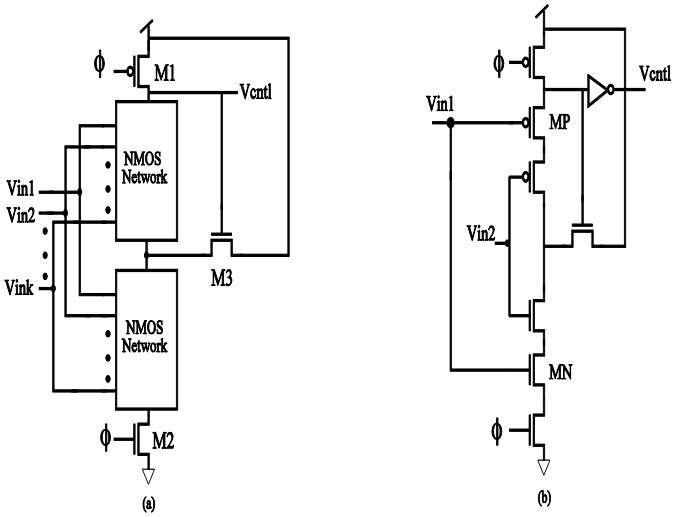

Figure 8: Mirror Technique (a) Block diagram, and (b) AND gate implementation.

The switching threshold of the uppermost evaluation network is raised due to the phenomena of body effect. However, the presence of additional NMOS network adds delay to the signal propagation. This highlights the careful sizing of transistors in the NMOS evaluation network. Also, the implementation of a wide fan in dynamic circuit requires a large number of transistors thereby consuming more silicon area.

E. Twin Transistor Technique

A new method to make the dynamic circuits immune to noise variations was proposed by Ganesh et al [9]. A two input AND gate implementation of the circuit is shown in Fig. 9.

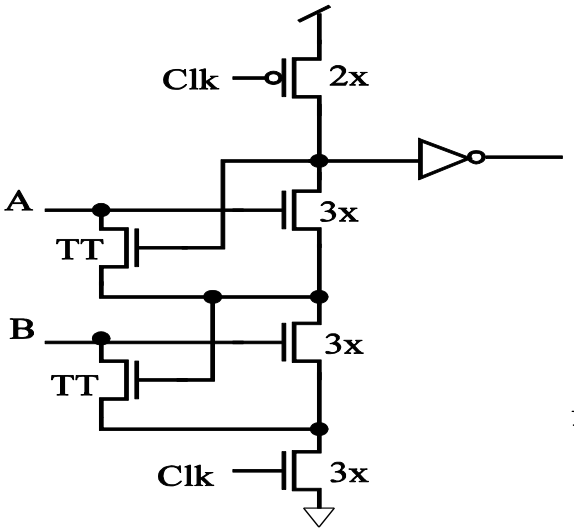

Fig. 9: Twin transistor technique.

Twin-transistor results by the use of an additional transistor in a cross-coupled manner. This arrangement raises the switching threshold of the input transistor thereby increasing the noise immunity by raising its source voltage. This configuration also solves the charge sharing problem and charging of the internal nodes is only invoked when the input combination in the PDN (pull-down network) leads to a potential charge sharing problem. However, the use of additional transistor at the input of the circuit increases the internal node capacitance and hence the delay of the circuit which is to be traded-off by increasing the size of the transistors in the pull-down network. This again leads to a compromise between delay and area of the circuit.

IV. SIMULATION RESULTS AND ANALYSIS

This section first provides simulation environment and then presents comparative analysis of results of different noise immunity techniques. The circuit designs are implemented on Tanner and simulated with 45nm technology file [10].

A. Simulation Environment

To evaluate the design metrics, all the existing designs are first implemented in Tanner 14.1 with similar sizing of the transistors. The 2 input NAND gate is utilized and implemented with dynamic logic employing different noise immunity improvement techniques. The spice netlist is extracted from the schematic diagram implemented on Tanner. All these netlists are simulated using Tanner tool for various input pattern with 45nm PTM technology file.

B. Simulation Results

The schematic of the 2-input NAND gate implemented using domino logic is shown in Fig. 10. Whereas Fig. 11 and Fig 12 shows twin transistor and keeper logic implemented on Tanner.

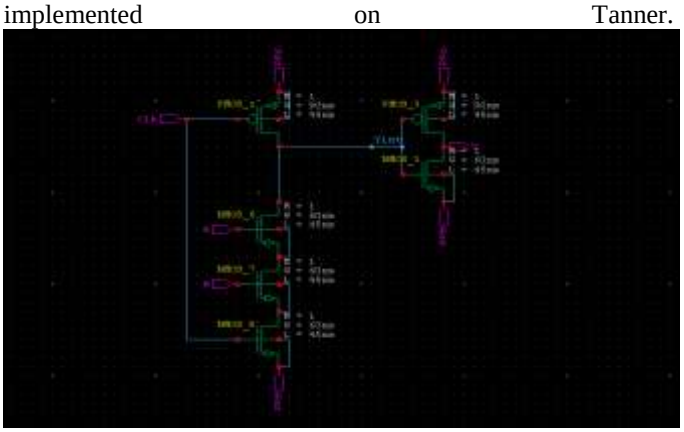

Fig. 10: 2-input NAND gate using domino logic.

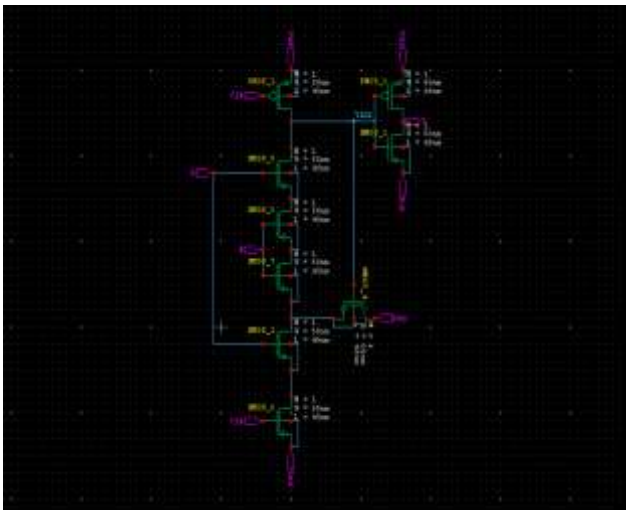

Fig. 11: Schematic Mirror technique

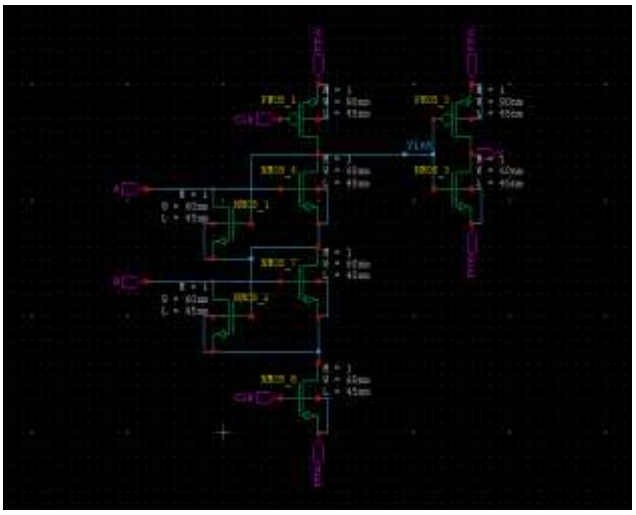

Fig. 12: Schematic Twin transistor technique.

Similarly, schematic for the other logic are also implemented and spice netlists are extracted. The various

noise immunity techniques implemented on Tanner are simulated to compute design metrics. Further, noise of different amount is supplied at the input and corresponding output is computed to measure the noise tolerance. A pulse which works are noise with increasing pulse width (increasing time of applied noise) and increasing value of noise (increasing the amplitude of the noise) and the flip in the output node is observed. A point at which node value changes, the value of noise pulse width and height is measured. These values are used to computed noise threshold energy (NTE) and average noise threshold energy (ANTE) as shown in Table 1.

TABLE I: DESIGN AND NOISE IMMUNITY METRICS FOR DIFFERENT NOISE IMMUNITY TECHNIQUES.

Immunity Techniques	Performance Parameters			Noise Immunity	
	Area (#Tran)	Power (nW)	Delay (ns)	Noise Immunity (ANTE)	Voltage
Keeper Technique	7	69.4	0.163	0.88	0.61 V
Mirror Technique	9	52	0.17	0.88	0.61 V
Twin Tran. Technique	8	48.4	0.166	0.98	0.67 V

From the simulation results it can be observed that Mirror technique requires more area whereas Keeper logic requires more power overhead. On the other hand, Twin transistor logic provides highest noise immunity with low power and moderate area overhead.

The area and power overhead over the different existing design are shown in Fig. 13 and Fig. 14, respectively.

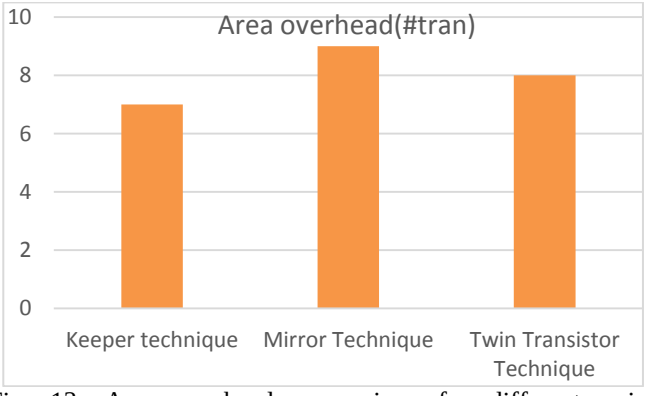

Fig. 13: Area overhead comparison for different noise immunity techniques.

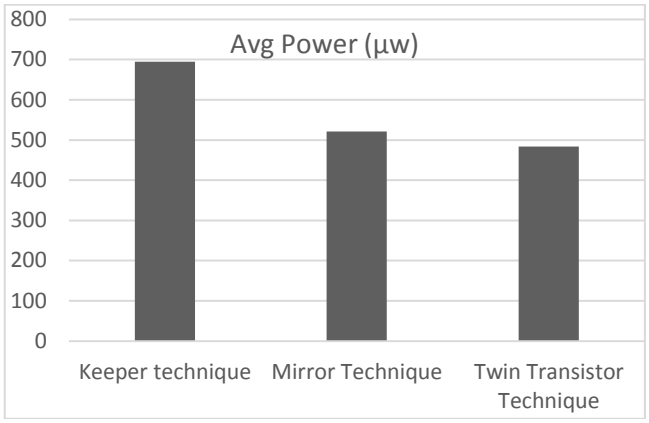

Fig. 14: Power comparison for different noise immunity techniques

Finally, the noise immunity measured in terms of average noise threshold energy is compared in Fig. 15. It can be seen from the figure that twin transistor approach provides highest noise immunity over the other existing design techniques.

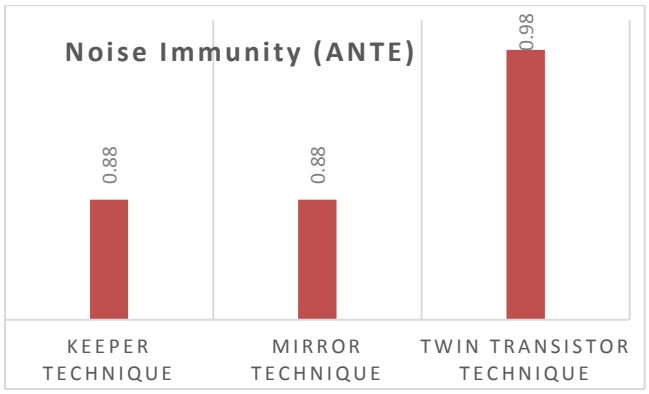

Fig. 15: ANTE for different techniques.

CONCLUSION

Dynamic logic improves the area efficiency and performance significantly but exhibits poor noise immunity. This demands a logic/technique that improve the noise immunity of the dynamic logic so that bulkier CMOS circuits can be replaced by the smaller dynamic circuits. This paper presents exhaustive review on the work done to improve the noise immunity. In order to evaluate the efficacy of the existing noise immunity techniques, all the different existing noise immunity techniques are implemented in Tanner and extracted netlist is simulated with 45nm PTM technology node. The noise immune techniques are implemented on a 2-input AND gate which was considered a logic. The simulation results using TSPICE shows that the twin transistor technique provides highest noise immunity technique over the other existing techniques.

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