An Efficient 32-bit Multiplier Design for High Speed Applications using Urdhav-Tiryagbhyam Algorithm

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Abstract: The use of Vedic mathematics lies in the fact that it reduces the typical calculation in the conventional mathematics to very simple once. This is because the Vedic formulae have been claimed to be building on the natural principles on which the human mind works. Vedic mathematics is a several effective algorithms, which has spread over to various branches of engineering such as computing. In computers, typical central processing unit devotes a considerable amount of processing time in implementing arithmetic operations, particularly multiplication operation. In this work, I have studied different multipliers, which give low power requirement and high speed, also give information of 'urdhva-Tiryagbhyam' algorithm of ancient Indian Vedic mathematics, which has utilized for multiplication to improve speed of multipliers. For Improving our generated result we used the concept of pipelining and design 4-bit, 8-bit, 16- bit & 32-bit pipeline Multiplier. The multiplier is implemented using Verilog HDL, targeted on Spartan-3E and Virtex-6 FPGA.

Keywords: VHDL, Urdhav -Tiryagbhyam.

1.INTRODUCTION

Consent of using multiplier in today's scenario is quite effective & highly advantageous in digital signal processing & all other applications[4]. With highly advancement in technology, many researchers had tried & trying to design multipliers which can offer either of the following design targets – higher speed, consumption of lesser power, layout regularity & small area or equal fusion of these all in single multiplier therefore making them fit for varied high speed, low power and compressed VLSI implementation. The ordinary multiplication method is "add & shift" algorithm. In parallel multipliers number of partial products to be added is the main parameter that determines the performance of the multiplier. To reduce the number of partial products to be added, Modified Booth algorithm is one of the most popular algorithms[6]. To achieve speed improvements Wallace Tree algorithm can be used to reduce the number of sequential adding stages. Further by combining both Modified Booth algorithm and Wallace Tree technique we can see advantage of both algorithms in one multiplier. However with increasing parallelism, the amount of shifts between the partial products and intermediate sums to be added will increase which may result in reduced speed, increase in silicon area due to irregularity of structure and also increased power consumption due to increase in interconnect resulting from complex routing. On the other hand "serial-parallel" multipliers compromise speed to achieve better performance for area and power consumption. The selection of a parallel or serial multiplier actually depends on the nature of application. In this lecture we introduce the multiplication algorithms and architecture and compare them in terms of speed, area, power and combination of these matrices. There are different types of multiplier: serial multiplier, serial/parallel multiplier, shift and Add multiplier, array multiplier, booth multiplier, Baugh wooley multiplier, Wallace tree,4-bit multiplier,8-bit multiplier,16-bit multiplier,32-bit multiplier, etc.

2. URDHAV TIRYABHYAM

Now here we will discuss about 32bit multiplier using vedic mathematics algorithm Urdhav Tiryagbhyam. The basic Sutras and Urdhva Tiryagbhyam Sutra in the Vedic Mathematics helps to do almost all the numeric computations in easy and fast manner[2]. The Sutra which we use in this project is Urdhva Tiryagbhyam (Multiplication). Urdhva Tiryagbhyam is "Vertically and Crosswise" multiplication. 16x16 **multiplier** generating a **32 bit** signed product and in 32 bit vedic it will result in 64 bit.

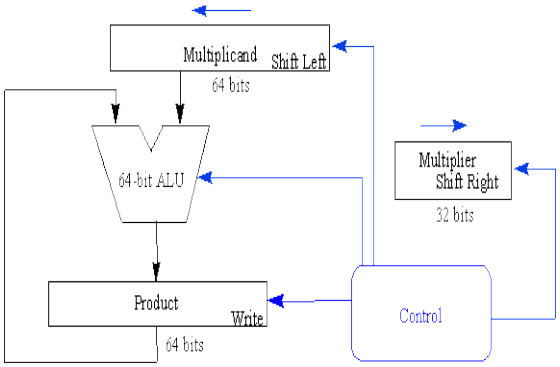

Fig 1: 32 bit multiplier

VEDIC MULTIPLIER is Urdhva Tiryagbhyam is "Vertically and Crosswise"[2][3]. Vedic multiplier is based on the algorithm, called Urdhva Tiryagbhyam which is one of the 16 Vedic sutras. The Urdhva refers to vertical and the Tiryagbhyam refers to the cross wise. This Sutra specifies how to handle the n*n order multiplication by smaller order multipliers. The first basic multiplier block required for the implementation of Vedic multiplication is 2x2 multiplier. From this basic 2x2 multiplier the 4x4, 8x8, 16x16, 32x32 are developed.

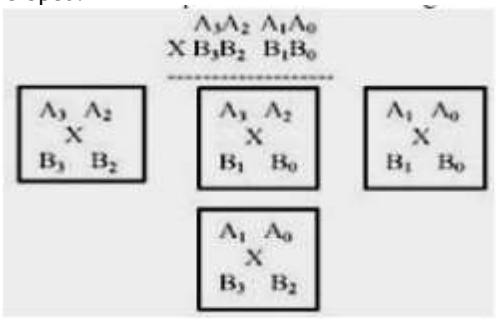

Fig 2: 4x4 bit Vedic multiplier

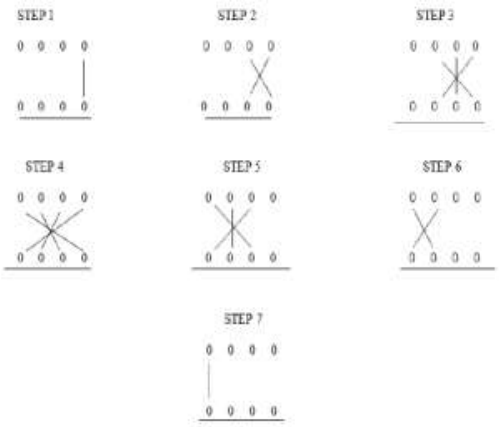

Fig 3: 4x4 Bit line diagram

3.BLOCK DIAGRAM

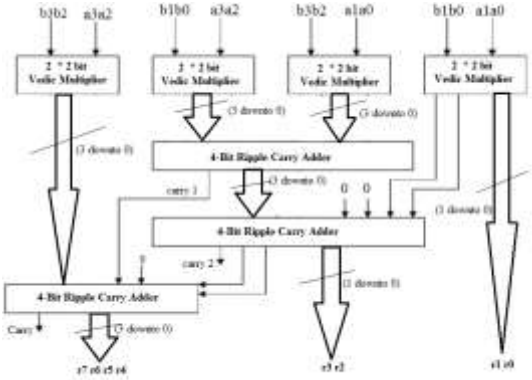

Fig 4: 8x8 vedic multiplier

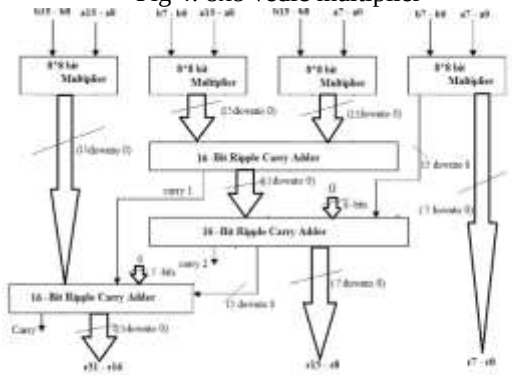

Fig 5: 16x16 vedic multiplier

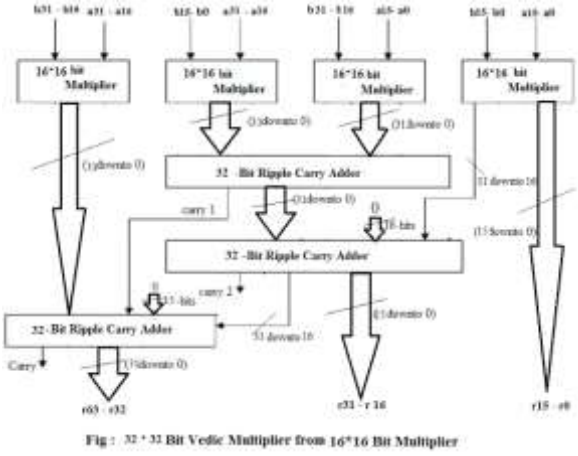

Fig 6: 32x32 vedic multiplier

1. In Fig 4 through 4-bit multiplier, 8-bit multiplier is developed,
2. In Fig 5 through 8-bit multiplier, 16-bit multiplier is developed ,
3. In Fig 6 through 16-bit multiplier, 32-bit multiplier is developed

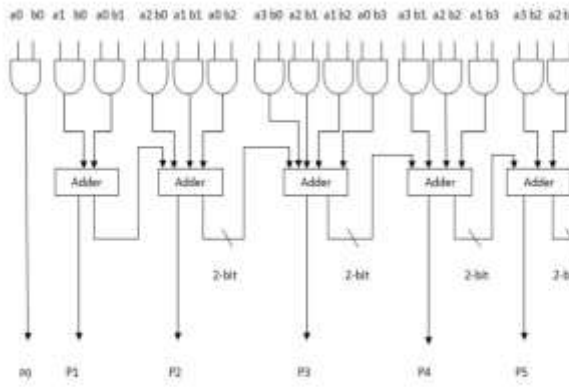

Fig 7: Combination of 8-bit, 16-bit & 32-bit multiplier using urdhav tiryagbhyam Algorithm.

In **Fig 7** is combination fig 2,3,4 of all the bits to get 64-bit as an output.

32-Bit Multiplier:

Presently here we will examine around 32bit multiplier utilizing vedic arithmetic calculation Urdhav Tiryakbhyam. The essential Sutras and Urdhva Tiryakbhyam Sutra in the Vedic Mathematics does all the numeric calculations in simple and quick way. The Sutra which we use in this venture is Urdhva Tiryakbhyam (Multiplication). Urdhva Tiryakbhyam is "Vertically and Crosswise" duplication[5]. 16x16 multiplier creating a 32 bit marked item and in 32 bit vedic it will bring about 64 bit.

Procedure of solving Urdhav-tiryagbhyam. Let us consider 8bit number inputs are a7,a6,a5,a4,a3,a2,a1,a0 and b7,b6,b5,b4,b3,b2.b1,b0 and products are p15,p14,p13,,…,p0 and temporary partial products t15,t14,….,t0.To slove it is divided into 4-4 bits then apply vedic vertical and cross wise multiplication to get 8 bit result.

Step1: to= b0a0.
Step2: t1= b0a1+b1a0.
Step3: t3= b0a2+b1a1+b2a0.
Step4: t4= b0a3+b1a2+b2a1+b3a0.
Step5: t5= b0a4+b1a3+b2a2+b3a1+b4a0.
Step6: t6= b0a5+b1a4+b2a3+b3a2+b4a1+b5a0
Step7:
t7= b0a6+b1a5+b2a4+b3a3+b4a2+b5a1+b6a0
Step8:
t8=
b0a7+b1a6+b2a5+b3a4+b4a3+b5a2+b6a1+b7a0.
Step9:
t9=b1a7+b2a6+b3a5+b4a4+b5a3+b6a2+b7a1.
Step10: t10= b2a7+b3a6+b4a5+b5a4+b6a3+b7a2.
Step11: t11=b3a7+b4a6+b5a5+b6a4+b7a3.
Step12: t12= b4a7+b5a6+b6a5+b7a4.
Step13: t13= b5a7+b6a6+b7a5.
Step14: t14= b6a7+b7a6.
Step15: t15= b7a7.

p0=b0a0
p1= LSB(4bit shift)
=LSB of(b0a1+b1a0)
p2= LSB(4bit shift)
=LSB of (b0a2+b1a1+b2a0)
.
.
p15= LSB(4bit shift) =LSB of (b7a7).

In 32bit multiplier steps consists of 15 steps of 32 bit and In this it includes 15 steps and then all 15 steps are being shifting 4-4 bit with an every single step and then added to get **64 bit** as a result.

4.IMPLEMENTATION AND RESULT

The main objective is to design and implement 32 bit multiplier which is efficient in terms of delay and area. Multiplication is the most important and complex operation in binary arithmetic, we designed a multiplier which can operate at high speed and increase in delay and area is significantly less with increase in number of bits. 32 bit multiplier is implemented using Verilog and tested.

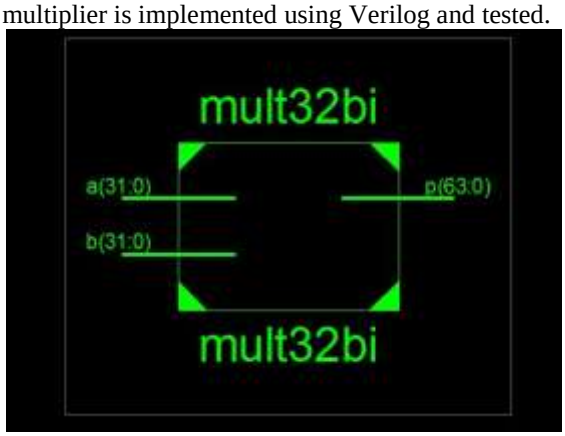

Fig8. block diagram of 32bit multiplier

In above diagram it consists of two inputs and one output.

Fig9: Technical view of 32bit multiplier

In fig 7 there is 64 , 8-bit multiplier which will gives a result in 64-bits.

Table1: Performance Analysis

	Ref[6]	Ref[7]	Ref[8]	Ref[1]	Proposed
Width	8-bit	8-bit	8-bit	8-bit	8-bit
Delay	28.27 ns	15.050 ns	23.973 ns	9.396 ns	9.00ns

Table2:Delay comparison of various 8-bit multipliers with proposed Urdhva Multiplier

	Ref[12]	Ref[5]	Ref[1]	Proposed
Width	16-bit	16-bit	16-bit	16-bit
Delay	13.452ns	27.148ns	11.514ns	11.25ns

Table 3: Delay comparison of various 16-bit multipliers Urdhva multiplier

	8-bit Ref[1]	16-bit Ref[1]	32-bit Ref[1]	32-bit proposed
Slices	113	410	1389	1407
IOBs	33	65	129	128
Delay	9.396ns	11.514ns	13.141ns	17.77ns

Table 4: Delay and area comparison of 32-bit multipliers with proposed Urdhva multiplier

	LUTs	Delay
Ref[1]	1545	13.141ns
Ref[13]	313	35.76ns
Proposed multiplier	251	17.77ns

4.CONCLUSION:

In this paper we have shown how to effectively we have worked in delay and area of a 32-bit multiplier by using Urdhva-Tiryagbhyam algorithm. In 32-bit multiplier results in 64-bit . In this design it is taken care about delay and area how delay is reduced and area is also reduced,, i.e., high speed, reduced delay and lesser area. The design has been synthesized on XILIN 14.5 Spartan 3E, and Virtex-6.

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