Design and Performance Anaysis of Sequential Circuit Using Clocking Techniques

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***Abstract*— The major issue of the VLSI design are area,cost,performance and reliability.But in the last few years power in the circuit is the major problem which is being faced by the very large scale integration industries.The power dissipation usually increased by the clocking system which includes the clock distribution system and sequential element(Flip-flop and Latches).The amount of power dissipation by clocking system in any chip is about 30% to 60% of the total chip power dissipation.So a new paradigm is introduced for clock distribution that uses current rather than voltage to distribute a global clock signal with reduced power consumption.So a new high performance current mode pulsed clock gate enable(CMPCGE)is designed using 45nm CMOS technology in tanner EDA tool**.

Keywords— Clock distribution network,Crosstalk,Current mode,Flip-flop,Low power.

I.INTRODUCTION

PORTABLE electronic devices require long battery life times which can only be obtained by utilizing low-power components.Recently,low-power design has become quite critical in synchronous application specific integrated circuits (ASICs) and system-on-chip(SOCs) because interconnect in scaled technologies is consuming an increasingly significant amount of power.Researchers have demonstrated that the main consumers of this power are global buses,clock distribution networks(CDNs),and synchronous signals in general[1].The CDN in the POWER4 microprocessor,for example,dissipates 70% of total chip power[2].

In addition to power,interconnect delay poses a main obstacle to high-frequency operation.Technology scaling reduces transistor and local interconnect delay while increasing global interconnect delay[3],[4].Moreover,conventional CDN structures are becoming increasingly damanding for multi-GHz ICs because skew,jitter and variability are often proportional to large latencies[5].

Prior to and in early CMOS technologies,current-mode(CM) logic was an interesting high-speed signaling scheme[6].CM logic,however,consumes significant static power to offer these high speeds.Because of this, usual CMOS voltage-mode(VM)signaling has been the de facto standard logic family for several decades.

Low-swing and current-mode signaling,however,are highly inviting solutions to help address the interconnect power and variability problems.Traditionaliy,the static power dominates dynamic power consumption in a CM signaling scheme.However,the static power is often much less than VM dynamic power latency is much improved over VM in global CM interconnect.

II.RELATED WORKS

All of the past CM signaling schemes perform current-to-voltage conversion and then use the buffered VM clock signal.However,driving the lowest level of a CDN with a full-swing voltage results in large dynamic power in inclusion to significant buffer area to drive the clock pin capacitances. Our CM scheme is highly integrated into the FFs that directly receive the CM signal to reduce overall power consumption and silicon area.

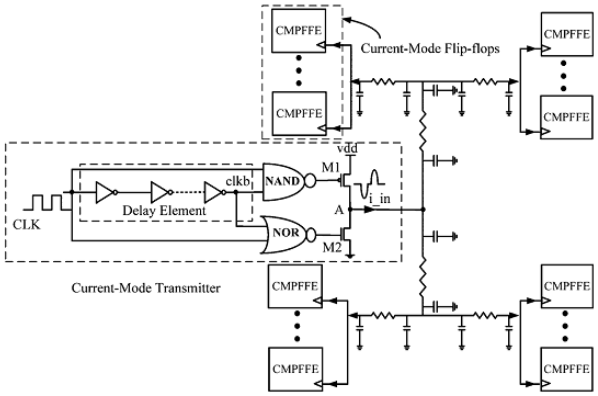
A.Current-Mode Pulsed Flip-Flop With Enable(CMPFFE)

The CMPFFE is similar to our previously published CMPFF,but uses an active-low enable(EN) signal.The CMPFFE uses an input current-comparator(CC) stage,a register stage and a static storage cell.The CC stage correlate the input push-pull current with a reference current and conditionally amplifies the clock to a full-swing voltage pulse that triggers the data to latch at the register stage.The feedback pulsed FF is in stark contrast to the past CM schemes which utilized expensive Rx circuits and buffers to drive the final FFs.

The choice of push-pull current implement a simple Tx circuit while maintaining a constant bias voltage on the CDN interconnect.The CMPFFE is only sensitive to unidirectional push current which provides the positive edge trigger operation of the FF.This design is efficiently modified using a complementary current comparator into negative clock edge FF using the pull current.

B.Current –Mode Transmitter and Distribution

In order to integrate the CMPFFE,a Tx provides a push-pull current into the clock network and distributes the required amount of current to each CMPFFE.Our proposed CM CDN with Tx, interconnect and the CMPFFE.The Tx receives a tranditional voltage CLK from a PLL/clock divider at the root of the H-tree network an a supplies a pulsed current to the interconnect which is held at a near Constant voltage.The clock distribution is a symmetric H-tree with comparable impedances in each branch so that current is distributed equally to each CMPFFE leaf node.



III.CLOCK GATING

Clock tree consume more than 50% of dynamic power.The components of this power are:

- Power consumed by combinational logic whose values are changing on each clock edge
- power consumed by flip-flop
- The power consumed by the clock buffer tree in the design.

Its good design idea to turn off the clock when it is not needed.Automatic clock gating is supported by modern EDA tool. They identify the circuits where clock gating can be inserted.RTL clock gating works by identifying groups of flip-flops which share a common enable control signal.Traditional methodologies use this enable term to control the select on a multiplexer connect to the D port of the flip-flop or to control the clock enable pin on a flip-flop with clock enable capabilities.

A.Latch free clock gating

The latch-free clock gating style need a simple AND or OR gate (depending on the edge on which flip-flop are triggered).Here if enable signal goes inactive in between the clock pulse or if it multiple times then gated clock output either can discharge prematurely or generate multiple clock pulse.This restriction makes the latch-free clock gating behavior in appropriate for our single-clock flip-flop based design.

B.Latch based clock gating

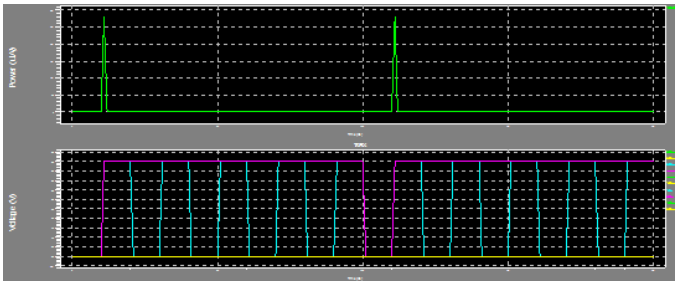
The latch-based clock gating styles adds a level-sensitive latch to the design to hold the enable signal from the active edge of the clock until the inactive edge of the clock.Since the latch taking the state of the enable signal and holds it until the entire clock pulse has been generated,the enable signal need only be stable around the rising edge of the clock,just as in the popular ungated design style.Specific clock gating cells are required in library to be utilized by the synthesis tool.Availability of clock gating cells and automatic insertion by the EDA tools makes it simpler design of low power technique.Advantage of this method is that clock gating does not require modifications to RTL description.

IV SIMULATION RESULTS

4.1 TRANSMITTER OUTPUT

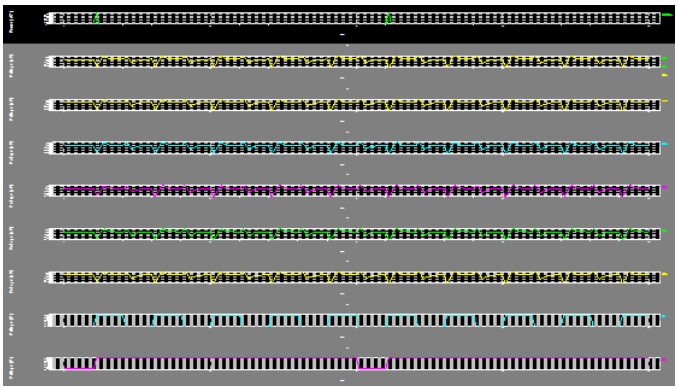
This screenshot (fig4.1)shows output of transmitter output for CMPCGE.

4.2 POWER OUTPUT



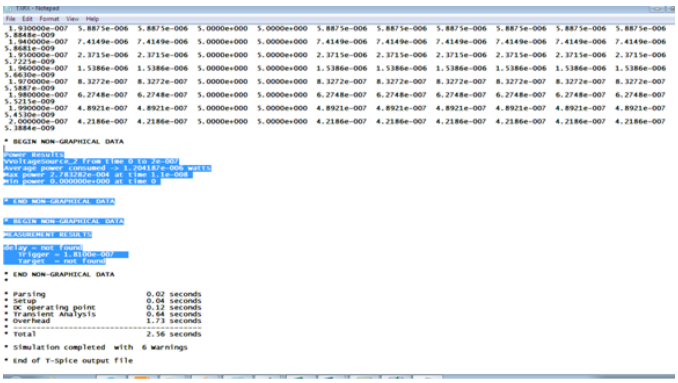
This screenshot (fig 4.2) shows the required power for CMPCGE.

4.3 OVERALL OUTPUT



This screenshot(fig 4.3) shows the output waveform is over all output of transmitter and receiver in the CMPCGE.

4.4 TIME DELAY



The time delay (fig 4.4) gives the amount of time taken for CMPCGE.

IV. CMPCGE TABLE

S.NO	PARAMETERS	SIGNAL RANGE
1	POWER CONSUMPTION	0.0027 miW
2	TIME DELAY	9.67 ns
3	SUPPLY VOLTAGE	5V
4	TRANSIENT TIME	1.17 S
5	OVERHEAD	1.56S
6	OVERALL TIME	2.98 S

VI .CONCLUSION

In this proposed implememtation,current mode clock gating enables transmitter and receiver circuit.The proposed current mode pulsed clock gate enable (CMPCGE) is much faster than existing sequential circuits with same silicon area and consumes only 7% more power compared to a traditional PFF at 5GHz.The transmitter section consists of proposed PFF which feed into the interconnect network followed by a receiver unit.The CMPCGE also eliminates the need for complex CM receiver circuitry and/or local VM buffers to drive high capacitive clock signal as in existing CM signaling schemes.The proposed scheme combines the best performance and greatest energy savings,with the best reliability.Reducing the swing on interconnect is an effective and powerful tool for the minimization of energy recreation,but requires a judicious optimization with respect to robustness,design complexity and energy reduction.

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