Design of High Performance Edge Detector and Its VLSI Implementation

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***Abstract*— VLSI design of the image processing cores is the main focus of the designers due to increase in image and video processing applications within most of the devices. Moreover the advancement in the VLSI technology with nano-scale transistors dimensions results in further increase in complexity of these devices. In several image processing applications edge detection is the commonly used operation to extract edge information available in the image. This information is further used to evaluate other parameters very efficiently. In this paper a novel low complexity and high performance edge detector is proposed and implemented. The proposed design is evaluated and compared over the existing architectures. The simulation results show that the proposed edge detector reduces area by 53.17% and delay by 2.04% compared to the existing architecture.**

***Keywords*— Digital Signal Processing (DSP), Edge Detector, Image Processing, Integrated Circuits, VLSI, Low Power Design.**

I. Introduction

The high performance designs are the prime requirement for the modern portable devices that are able to process real time applications. The software implementation of the computational units within computers are becoming inefficient, therefore, hardware implementation of the core computing units are the area of research these days. With the continuous scaling of CMOS technology, billions of transistors can be fabricated on the same chip to implement the functionality. All the circuits on these portable devices demand highly energy efficient designs as user cannot manage with rapid discharge of battery [1]. The low computational complexity designs not only reduce power consumption and increase the battery lifetime but also increases the reliability of the system. Further, these designs also reduce the cost associated with cooling the chip. Thus, the modern devices demands high performance and reduced complexity designs.

In the VLSI designs, the primary design parameters are the area, power and delay that form a tradeoff triangle i.e. improving one parameter damages the other. The conventional approach of VLSI design provides accurate results i.e. follow the given specification. But in real scenario it is not always required. There are many applications where minor error can be tolerated called as error tolerant applications. The multimedia applications such as image/video processing are error tolerant applications. In these applications, small error is tolerable as these applications produce output for human consumption [2] as human have limited visual perception. Along with the multimedia applications, several other applications such as that exhibit probabilistic computation and iterative computation also exhibits error tolerance. Thus, the accurate designs for these applications are the waste of power/area and performance. For these applications, accuracy can be seen as the new design parameter that can be traded to improve all design parameters.

In several image processing, machine, computer vision and feature extraction applications, edge detection is commonly used operation. The performance of the applications depends on the performance of the edge detector. Several existing edge detection operators [3-10] such as Canny, Sobel, Kayyali etc. existing in the literature are not efficient. This demands an energy efficient edge detector. This paper proposes a novel edge detector that can be effectively utilized in the image processing applications. In the proposed edge detector less significant coefficients are eliminated and only significant coefficients are considered. Further the efficacy of the proposed edge detector is evaluated over the well-known existing architectures by designing and computing the design metrics. The simulation results shows that proposed edge-detector provides significantly improved design metrics and simultaneously provides images of acceptable quality by most of the applications.

II. Literature Review

There are several approaches in the literature that are used to enhance the quality of an image. The edge detection is the preprocessing that is commonly employed in several image enhancement techniques. Further the edge detection has several applications from medical imaging to automation in the industries. Fig. 1 illustrates an image and corresponding edge.

(a) (b)

Fig. 1: Illustration of original image and its edge

In the literature, there are several techniques that are used to find the edge including Canny [11], Kayyali, Robert, Laplacian of Gaussian and Sobel etc. Sobel, Prewitt and FreiChen are 3x3 masks operators. Although the Prewitt kernels is computationally simple over the Sobel, but the Sobel operator provides superior noise suppression

over the Prewitt. Further, the complexity of the LOG is larger than previous mentioned operators. Following subsections provides different operators that are commonly used within edge detectors.

2.1 Robert operator:

The simplest and the computationally efficient operator is Robert's Cross operator which computes 2-D spatial gradient of an image. The pixel values at each coordinate represent the gradient in spatial domain. The operators are very simple and compute the gradient in the diagonal direction. The two operators (G_X and G_Y) are orthogonal to each other and can be used to compute gradient separately. The overall gradient and the orientation are given by the Eq. (1) and Eq. (2).

$$|G| = \sqrt{(G_X^2 + G_Y^2)} \quad (1)$$

$$\theta = \tanh^{-1}\frac{G_X}{G_Y} - 3\frac{\pi}{4} \quad (2)$$

The two gradients can then be combined to achieve the overall gradient which reflects the edge of the image. The advantages of the Robert's operator is its simple architecture and low complexity of implementation but it shows poor noise immunity therefore, cannot be used in the highly noisy environment.

2.2 Sobel operator:

The Sobel operator whose pair of 3x3 kernels is shown in Fig. 2 [12-16] overcomes the limitation of the Robert operator. The Sobel operators computes maximum gradient in horizontal and vertical directions which are then combined to achieve overall gradient. Further one operator can be achieved by rotating 90° the other.

$$G_x = \begin{bmatrix} -1 & 0 & 1 \\ -2 & 0 & 2 \\ -1 & 0 & 1 \end{bmatrix}$$

$$G_y = \begin{bmatrix} 1 & 2 & 1 \\ 0 & 0 & 0 \\ -1 & -2 & -1 \end{bmatrix}$$

Fig. 2: Kernels for the Sobel edge detector

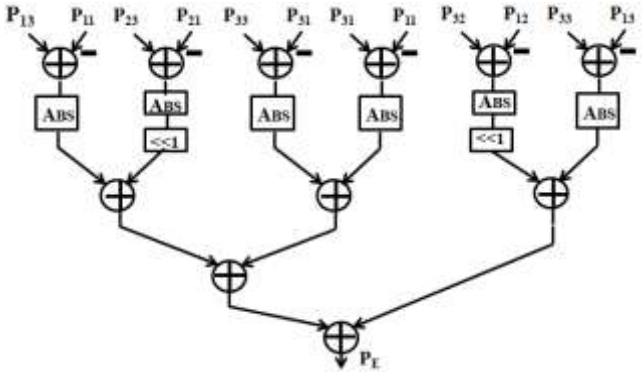


Fig. 3: Circuit diagram of Sobel edge detector

The gradient magnitude and its orientation is given by Eq. (3) and Eq. (4).

$$\theta = \tanh^{-1}\frac{G_X}{G_Y} \quad (3)$$

Further, to reduce the complexity of the gradient magnitude can be computed using sum of absolute values which is given by Eq. (4).

$$|G| = |Gx| + |Gy| \quad (4)$$

The advantage of the Sobel edge is its higher noise immunity i.e. it provide less sensitivity the noise and provides higher sensitivity to the edges. Therefore it most commonly used operator in the edge detector.

Most of the existing techniques suffer from the higher computational complexity and area inefficiency. The proposed filter given in the next section overcomes this limitation.

III. Proposed edge detector

This section presents the proposed novel algorithm for edge detection and its architecture.

3.1 Proposed mask for edge detection

The less significant coefficients from the Sobel kernel can be eliminated to reduce the implementation complexity without significantly affecting the quality of the output image. As we can see that there are 10 non-zero terms in the 5x5 Sobel operator for each gradient i.e. G_X and G_Y, this will requires seventeen adder to implement the whole Sobel edge detector. The hardware can be reduced significantly without much distortion in the output images by eliminating some of the non-zero terms. The proposed edge detector masks for G_X and G_Y are given below:

$$Gx = \begin{bmatrix} 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & -1 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 \end{bmatrix}$$

$$Gy = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & -1 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

The approach computes horizontal gradient and then vertical gradient by using of proposed horizontal (G_X) and vertical mask (G_Y). Input image is applied and image is convert into number of 5x5 matrix, then it will convolved with horizontal mask and generates the vector directional derivates, in same way the vertical mask is applied to generate vertical gradient. The main assumption of masking is made by considering the concept of inter pixel correlation. The pixel values in an image are very close to each other and the variation is almost equal to one. Instead of processing the entire pixel in 5x5 kernels, a suitable mask is applied as a filter which passes horizontal and vertical pixels as shown in below Fig 4.

3.2 Proposed diamond shaped kernel:

The overall proposed edge-detector mask as given below is consists of few values which are to be processed that results in fast computation and low area and power consumption at architectural level. The new filter mask consists of negative and positive values. By applying absolute on the result values and summing up them generates the same conventional function with reduces complexity.

$$\begin{bmatrix} 0 & 0 & 1 & 0 & 0 \\ 0 & -1 & 0 & -1 & 0 \\ 1 & 0 & 0 & 0 & -1 \\ 0 & 1 & 0 & 1 & 0 \\ 0 & 0 & -1 & 0 & 0 \end{bmatrix}$$

Fig. 4: Proposed diamond shaped mask

The gradients in horizontal and vertical directions are evaluated based on the proposed masks which are then used to compute final value of pixel of the edge image as given by the expression below.

$$G_{x1} = Abs(G_x) \quad (13)$$

$$G_{y1} = Abs(G_y) \quad (14)$$

$$Edge = G_{x1} + G_{x2} \quad (15)$$

3.3 Proposed edge detector circuit diagram

The proposed edge detector as shown in Fig. 5 below consists of only adders. The proposed edge-detector requires least hardware over the existing designs. The sizes of first two adders are 8-bit whereas for the last one is 9-bit. Due to the reduce hardware, the proposed design provides significant improvement in area, power and delay metrics.

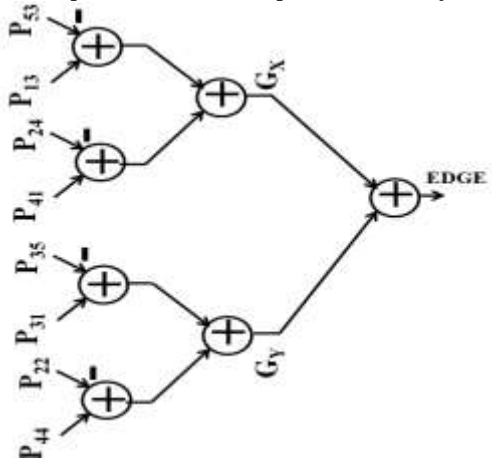


Fig. 5: Proposed edge detector circuit diagram

The efficacy of the proposed edge detector over the existing by implementing and simulating using EDA tools is detailed in next section.

IV. Simulation results analysis

The MATLAB tool is to model proposed and existing edge detectors to evaluate the quality metrics [17], [18]. These implemented designs on MATLAB are then simulated with standard test images such as Lena, Baboon, and Airplane etc. On the other hand, to evaluate the design metrics designs are implemented and Verilog HDL and simulated on ModelSim EDA tool. Further, the functionality of the proposed design is rigorously verified on ModelSim. Finally, the design is implemented on the Tanner 14.1 and simulated to extract design metrics such as area, power and delay.

4.1 Analysis of quality metrics

Table 1 shows the simulation results extracted by simulating designs benchmark input images on MATLAB.

Table I: Error metrics comparison

Metric	Image	Acc.	Abs.	Prop.
PSNR (dB)	Lena	13.87	12.35	13.95
	Camera man	14.67	12.05	16.82
SSIM	Lena	0.6423	0.5871	0.6502
	Camera man	0.6987	0.5887	0.7040
FSIM	Lena	0.778	0.735	0.8490
	Camera man	0.8501	0.8142	0.8556

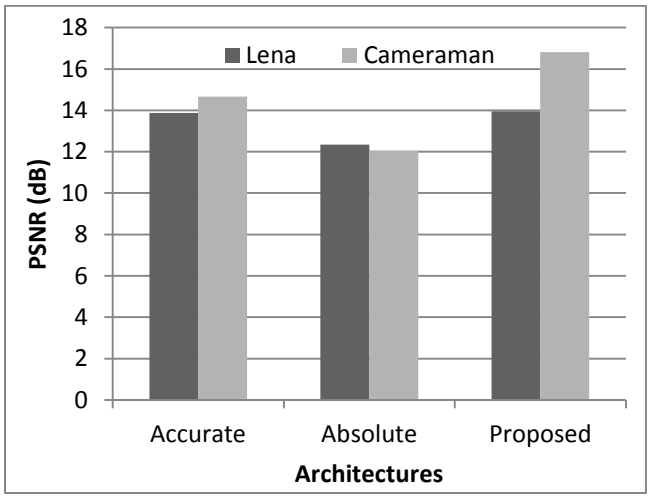


Fig. 6: PSNR comparison for different ED

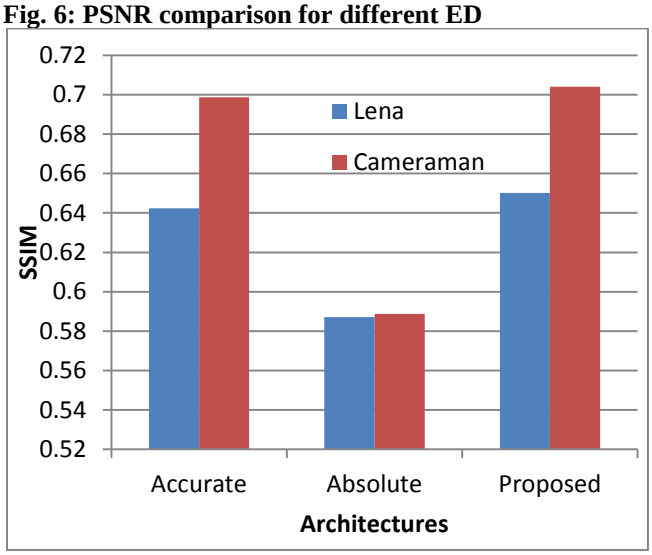


Fig. 7: PSNR for various ED architectures

It can be observed from Fig. 6 and Fig. 7 that the proposed design provides higher PSNR for Cameraman

image over the Lena image. The kernel for the accurate and the absolute mask considered are 3x3 while for the proposed mask is 5x5.

4.2 Architectural level analysis

All the existing and the proposed edge-detector architectures are implemented in Verilog to evaluate design metrics. Further the designs are synthesized and are implemented in FPGA (Spartan 6). The simulation results as summarized in Table 2 shows that proposed design requires very less area over the existing accurate design. The number of logic block required in the proposed design is only 59 as compared to the 126 in the accurate design. Further it can also be observe that proposed design significantly reduces delay and time/frame.

Table 2: FPGA results for various architectures

Parameter	Absolute	Proposed
Logic Block	126	59
Delay (n Sec)	5.061	4.536
Frequency (MHz)	196.98	260.5
Time/frame (µSec)	518.24	121.4

The comparison of different design metrics as shown in Fig. 8 and Fig. 9 reveals that proposed design requires less logic block, less delay and higher frequency.

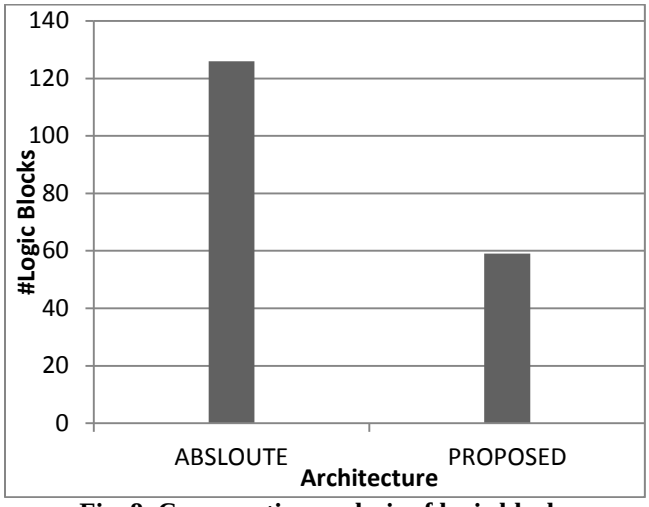


Fig. 8: Comparative analysis of logic block

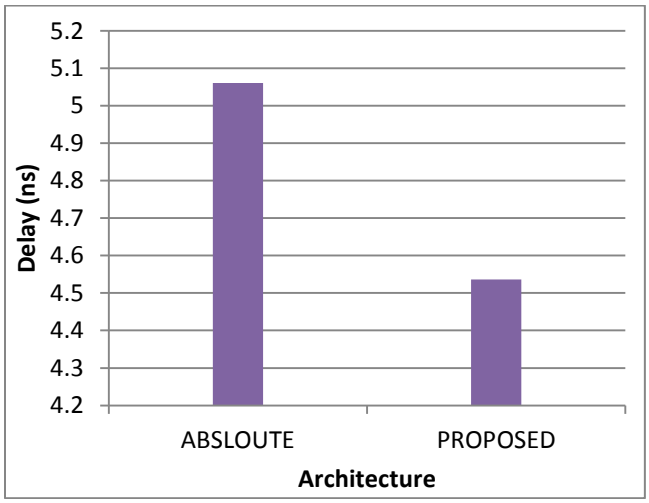
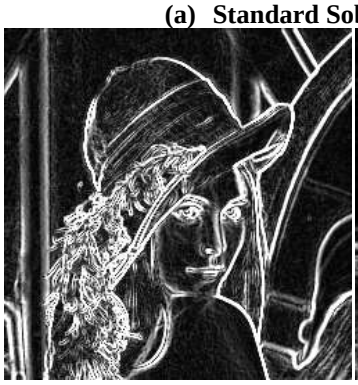
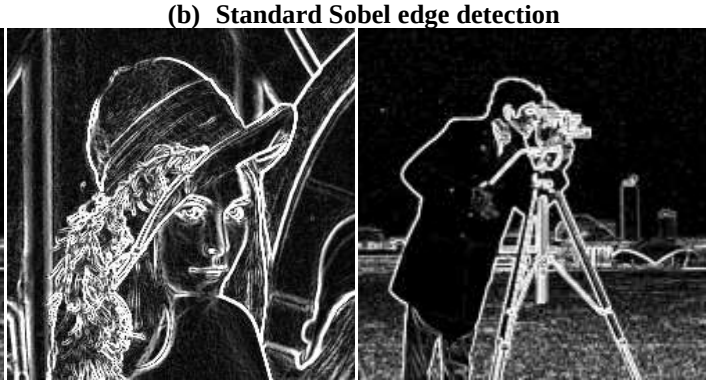


Fig. 9: Comparative analysis of delay

(a) Standard Sobel edge detection

(b) Standard Sobel edge detection





(c) Absolute Sobel edge detection **(d) Proposed edge detection**

Figure 10: Edge images using various edge detectors

V. Conclusion

A novel 2D Gaussian smoothing filter is proposed in this paper that provides improved power, delay and area with small loss in accuracy. The novel 2D Gaussian smoothing filter provides high the speed by the approximating the kernel coefficient. Comparisons with conventional Gaussian smoothing filters showed that the proposed novel 2D Gaussian smoothing filter performed better than the all conventional Gaussian smoothing filters in both power consumption and speed performance. Novel 2D Gaussian smoothing filter can be utilized in all those applications where there is no exact requirement of accuracy or where ultra-low power and high-speed are more important than accuracy.

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