OSTBC Encoder design with less BER on FPGA

1Pankaj Shingh Kshatriya, 2Vivek dubey
SRIT, Jabalpur

Abstract: **An orthogonal space-time block code (OSTBC) along with a minimum-BER and high SNR is Proposed and analyzed. the aim is to reduce the BER with new fully orthogonal fading matrix . The total number of branches that is being used for processing at the receiver is compared and computed. This paper works with Field Programmable Gate Array (FPGA) designing of an entire digital wireless communication for baseband system. The proposed BER tester also can be said BERT integrates the modules of a conventional communication system along with an AWGN channel into a FPGA. The BER is calculated for a 4x4 MIMO system.**

Index **- orthogonal space-time block code (OSTBC), generalized selection combining (GSC), multiple input multiple output (MIMO). AWGN, Field Programmable Gate Array (FPGA), Multi Input Multi Output (MIMO), Single Input Single Output (SISO), VHDL (VHSIC Hardware Description Language).**

I-Introduction

Need for mobile communication systems with high data rates and improved link efficiency for a variety of applications it dramatically increased in recent years. New concepts and methods are necessary in order to cover this huge need, which counteract or take advantage of impairments of mobile communication channel and optimally exploit limited resources such as bandwidth and power. Multiple antenna systems are an efficient means for increasing rendering. In order to utilize huge potential of multiple antenna concepts, it is necessary to resort to new transmit strategies, referred to as Space-Time Codes, which, in addition to time and spectral domain, also use spatial domain. Rendering of such Space-Time Codes is examined in this thesis with and without conventional channel coding strategies. Properties of equivalent SISO-channels were key results in order to examine rendering of OSTBC [1][3]. Determination of structure of equivalent channel is also a matter of vital importance in this work. To this end, proposed work show that MIMO-channel in case of Space-Time Codes from quasi-orthogonal designs is transformed into an equivalent block-diagonal MIMO-channel with identical blocks having constant eigenvectors, independent of channel realization. Furthermore, proposed work show that Eigen values of each block are pair wise independent and follow a non-central chi-square distribution, where number of degrees of freedom equals four times number of receive antennas. By relaxing requirement of full diversity one arrives at second group of Space-Time Codes from quasi-orthogonal designs. MIMO systems with multiple antenna elements at both link ends are an efficient solution for future wireless communications systems as they provide high data rates by exploiting spatial domain under constraints of limited bandwidth and transmit power. Space-Time Block Coding (STBC)[2] is a MIMO[2] transmit strategy which exploits transmit diversity and high reliability. Space–time coding is a technique used in wireless communications to transmit multiple copies of a data stream across a number of antennas and to exploit various received versions of data to improve reliability of data-transfer

These codes represent a generalization of Space-Time Codes from orthogonal designs. Particularly, proposed work show in this work, that not only Alamouti-scheme[2], a OSTBC[1][3] for two transmit antennas, but also its generalized version achieves capacity in case of one receive antenna. Drafted codes are then examined with respect to error rate rendering and spectral efficiency with optimal as well as suboptimal receiver structures. In second part of this work combination of Space-Time Codes with conventional channel coding techniques is considered. New receiver structures are presented and rendering of Space-Time Codes with iterative algorithms for soft-input-soft-output-decoding is examined and optimized with help of new analytical tools, so called EXIT-charts [4]. Furthermore, some criteria for optimal mapping strategy are derived in case of OSTBC [1][3].

The Alamouti Code: Consider designing a square space-time codes utilizing two transmit antennas. The most general form of this space-time code is given by

y=Sx+n

$$\begin{bmatrix} y_1 \\ y_2 \end{bmatrix} = \begin{bmatrix} s_{11} & s_{12} \\ s_{21} & s_{22} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} n_1 \\ n_2 \end{bmatrix}$$

y= is output signal

x= is input signal

n= is noise

S= is Fading Matrix

For orthogonality $|S^H S| = 0$

II. Tool used

We used Xilinx ISE 9.2 - Web-PACK for our programming and considered VHDL[1] as our primary language. VHDL[1] is the Hardware Description Language can be used to design a digital system at multiple levels of abstraction, ranging from the gate level to the algorithmic level.

III. Proposed design

Figure below shows a design for PSK module which we are using for generation of symbols for the Orthogonal Encoder it's been developed and Verified on Xilinx EDA.

Module 'clkcounter' is there for generating control signals and these control signals provides proper synchronisation between other modules.

Module 'tr' receives four bit input of digital signal which can be any one quantized level of digital input signal, because a complete cycle of any signal can have 16 time intervals so it receives total 64 input bit and ones it receives 64 bit it consider it as one cycle and pass these 64 bits to next module and starts receiving next inputs.

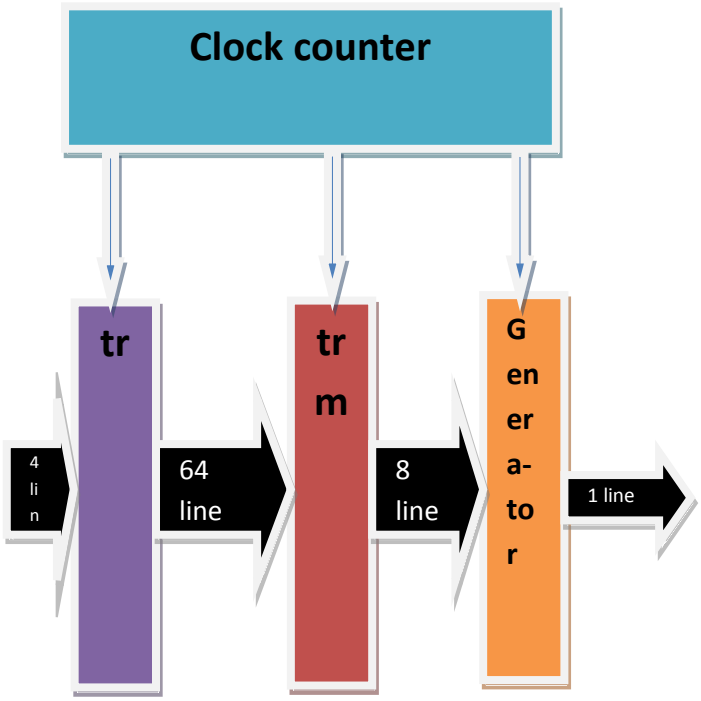

Figure 1: the proposed simulink modal

Module 'trm' gets 64 bit input which is a complete cycle of input it observe the patterns and recognise the phase difference from the last received cycle as per that observation it generates a 8 bit encoded output signal which is actually a patterns of phase difference in 8 bit parallel form of PSK.

Module 'generator' gets 8 bit encoded input and it simply converts that 8 bit parallel form of PSK into serial single line PSK output.

Figure below is the proposed modal to be implemented on FPGA, the designing will be hierarchal design which will have six modules, first module is been developed and been explain above

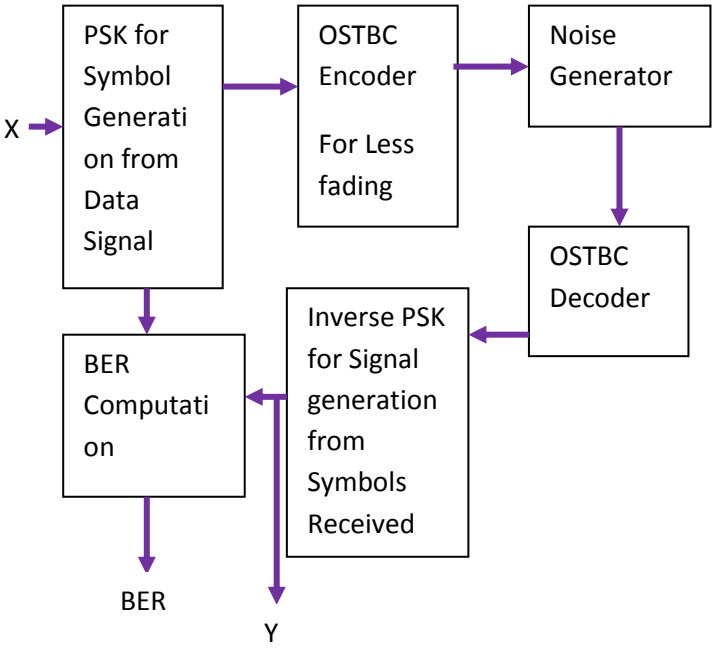

Figure 2: Proposed Modules and its interfacing

From the figure 2 the first block is for developing symbols from given signal we are using 4-PSK module hence there will be 4 symbols with phase shift of 90^0 , 180^0 , 270^0 and 360^0 , nest block is Proposed OSTBT module which will used propose fading orthogonal fading matrix to Encoding the Symbols, third module will a channel it will introduce noise into the encoded output from the Encoder the noise type will be adaptive white Gaussian noise, forth module is OSTBC decoder which will again used the proposed fading matrix for decoding the received symbols the forth module will convert those symbols into received signal 'Y' it will be inverse 4-PSK design.

The last module will compute the BER between the actual signal and received signal

IV. Results

Till the designing of PSK is been done figure show below that the 16 PSK for any signal x.

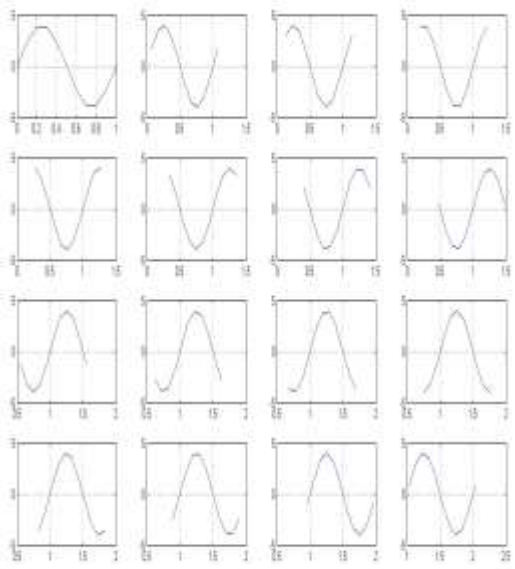

Figure 3: 16-PSK for signal x

16-PSK module is been simulated with the help of Xilinx EDA tool and its Integrated Simulation environment is been used for generation of waveforms, the design used 274 slices and 466 LUTs the time delay observer for the design is 4.040 ns and maximum frequency is 107.083 Mhz.

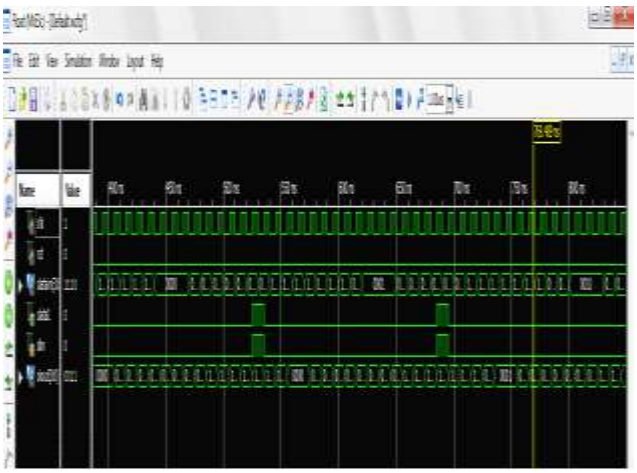

Figure 4: Simulation for PSK module

IV. Conclusion

At the end one can conclude that OSTBC is the best approach when MIMO- OFDM data is being transmitted from wireless channel like AWGN, it can also be concluded it provides high SNR and less BER as compare to other techniques, the proposed model is to implement whole design on FPGA with VHDL language and the observed results for PSK module are as was expected. In future the rset of module will be design for implementation of full proposed modal for OSTBT encoder and decoder.

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