Design and Implementation of Low Complexity Sharpening Filter for Image Scaling Applications

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***Abstract*— There is significant use of portable devices in recent years that employ multimedia applications. The image processing has become a prominent part in several applications from medical to entertainment. In order to improve the efficiency of these application hardware implementation of core computational unit is required. As the cost of the device increases with increasing complexity, low complexity architecture is the prime requirement. In this paper, new sharpening filter architecture is proposed that can be effectively utilized in the different portable devices. The proposed design is implemented in the MATLAB and Verilog to compute the quality and design metrics respectively and compared over the existing architectures. The simulation results show the proposed sharpening filter reduces area and delay by 0.787X and 47.7% respectively over the conventional sharpening filter.**

***Keywords*— Sharpening Filter, Digital Signal Processing (DSP), Image Scalar, Image Processing, Integrated Circuits, VLSI.**

I. Introduction

The modern VLSI technology allows us to build an Integrated circuit (IC) that can have thousands of transistors into single chip. This integration of huge functionality is imposing several challenges to the VLSI designer as increasing functionality increases the complexity which in turn increases failure probability. Further as area, power and delay are main area of concern and at the same time it is very difficult to achieve optimal value of these parameters. Image processing application is the prime component of the multimedia applications. The huge power and energy requirement in these processing worsen the performance of these devices. Thus, low complexity image processing is the demand for modern battery operated portable devices [1] which can be achieved designing low computational complexity processing cores.

It can be observed from the literature that the primary design parameters which include area, power and delay form a tradeoff triangle i.e. improving one parameter damages the other. There are many applications where minor error can be tolerated called as error tolerant applications. The multimedia applications such as image/video processing are error tolerant applications. In these applications, small error is tolerable as these applications produce output for human consumption [2] as human have limited visual perception. Thus, the accurate designs for these applications are the waste of power/area and performance. For these applications, accuracy can be seen as the new design parameter that can be traded to improve all design parameters.

Various image processing techniques such as image restoration, image enhancement, image scaling etc enable the user to tune the image according to his needs. Among these techniques, image sharpening is one which has wide variety of applications ranging from medical imaging to mobile imaging. Image sharpening is a process of increasing details of the objects within the image over the background. The increase in the details increases the deceivability of the image. Further, image sharpening is commonly used as preprocessing in several other image enhancement/ processing techniques such as image scaling. The image sharpening severely affects the performance of the applications due to high computational requirements. Therefore a low complexity sharpening filter is required.

This paper proposes a novel low complexity image sharpening filter. The existing and proposed designs are implemented and then evaluated design and error metrics and compared with the well-known existing architectures. The simulation results shows that proposed sharpening filter provides significantly improved design metrics and simultaneously provides acceptable quality.

II. Literature Review

The sharpening filter is designed to improve the visual perception of the object in the image with respect to the background. The sharpening filter eliminates the low frequency noise therefore acts as a high-pass filter. It removes noise and also enhances the edges. The sharpening filter is governed by the kernel i.e. increases the intensity of the center pixel over the neighborhood.

2.1 Conventional sharpening filter

In general the sharpening operation is given by the kernel with different weights and the operation of sharpening is the convolution of input image with that kernel [1]-[4]. Although the sharpening is done with respect to its neighbor pixels and consideration of large number of neighbor pixel will remove more noise, a 3x3 sized kernel is commonly used to sharpen the image. The 3x3 kernel mask is also called neighbor-8 mask as it considers 8-neighbour to compute the sharpened pixels. An example of 3x3 size kernel is given by the Equation (1).

$$K_S = \begin{bmatrix} -1 & -1 & -1 \\ -1 & S & -1 \\ -1 & -1 & -1 \end{bmatrix} \qquad (1)$$

Similarly a 5x5 size kernel is given by the Equation 2.

$$K_S = \begin{bmatrix} -1 & -1 & -1 & -1 & -1 \\ -1 & -1 & -1 & -1 & -1 \\ -1 & -1 & S & -1 & -1 \\ -1 & -1 & -1 & -1 & -1 \\ -1 & -1 & -1 & -1 & -1 \end{bmatrix} \quad (2)$$

Here, S is the sharpening parameter which is defined by user based on the image property. The value of S determines the degree of sharpening. The sharpening filter improves the appearance of the image by increasing the demarcation between the darker and the brighter part of the image. The computational complexity of the 5x5 kernel is very higher and therefore not commonly used. Further, the computational complexity of 3x3 is large of some applications, therefore to reduce the computational complexity of the sharpening filter further, different kernels are proposed in the literature. Following subsection further provides different low complexity sharpening filter masks.

2.2 Neighbour-4 sharpening filter

In this filter, four less significant coefficients are eliminated from the mask to reduce the computational complexity of the filter [5].

$$K_S = \begin{bmatrix} 0 & -1 & 0 \\ -1 & S & -1 \\ 0 & -1 & 0 \end{bmatrix} \quad (3)$$

In this kernel only five coefficients are non-zero; therefore its complexity is much smaller than the complexity of the original 3x3. The number of adder required in the conventional 3x3 kernel and neighbor-4 are 8 and 4 respectively. The multiplier required by both the designs is one only. Since the number of adders required implementing the neighbor-4 kernel is nearly half over conventional, it reduces power and area metrics significantly. Further, the reduction in the quality due to elimination of the corner coefficients is not significant and the output image is completely acceptable.

The above mentioned kernel requires two line buffers while using it in the applications for real-time implementations. The line buffer

2.3 T and inverse-T shaped sharpening filter

In this filter only two row are considered instead of three to reduce line buffer from 2 two 1. As the line buffer is very costly, the reduction in line buffer significantly reduces the cost of the sharpening filter in the application [6]. Further, if only two row are considered, it requires two kernels such that neighbor pixels from both upper and lower row of the reference pixels are considered. The resulting two matrixes are given by Eq. (4) and Eq. (5).

$$K_S = \begin{bmatrix} -1 & S & -1 \\ 0 & -1 & 0 \end{bmatrix} \quad (4)$$

$$K_S = \begin{bmatrix} 0 & -1 & 0 \\ -1 & S & -1 \end{bmatrix} \quad (5)$$

These matrixes are generated from kernel of neighbor-4 kernel. The coefficients of the kernel are forming the shape of T and inverse-T, therefore the sharpening filter is called as T and inverse-T kernel base sharpening filter. The computational complexity of this filter is very small, as it requires only two adders to implement the filter.

III. Proposed work

This section presents the proposed sharpening filter. The working principle and analysis on the complexity reduction of the proposed architecture is detailed in this section.

4.2 Proposed sharpening filter

It is observed that sharpening filter have large computations and that consumes huge power and provides large delay. Reducing the complexity of the sharpening filter also provides significant reduction power and delay. Therefore, this work proposes a new sharpening filter kernel that has very small non-zero value.

4.2.1 Proposed sharpening kernel

As the conventional sharpening kernel of 3x3, all the kernel coefficients value is -1 except center coefficient as given by Eq. (1). S is the sharpening parameter and is specified by the user depends of the required sharpening. In order to reduce the complexity without significant reduction in the quality, outer coefficients are eliminated. The proposed sharpening kernel (K_{ps}) is given by Eq. 6.

$$K_{pS} = [-1 \quad S \quad -1] \quad (6)$$

It can be observed from the Eq. (6) that proposed kernel requires only two adders and one multiplier. Further in order to maintain the brightness level, the kernel is divided by its gain which is (S-2). Therefore a divider is also required to implement the proposed kernel. In order to reduce the complexity of the divider, parameter S is selected such that the results term (S-2) will be in the form of power of two (2^x) which can be easy implemented by right shift operation. Therefore, it can be seen that the proposed design requires two adders and a multiplier.

4.2.2 Proposed sharpening filter architecture

The architecture of the proposed sharpened filter which implements the functionality of the Eq. 6 is shown in Fig. 1. On the other hand, the conventional sharpening kernel requires eight adders for implementation. Only three pixels will be the input to the sharpening kernel and P_{22} is the reference pixel which will be replaced by the sharpened pixel P_S.

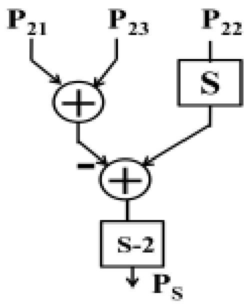

Fig. 1: Circuit of the proposed sharpening kernel.

The proposed sharpening kernel requires only single adder and a multiplier as the divider complexity can be reduced by selecting appropriate sharpening parameter. The proposed sharpening kernel reduces number of adder significantly over the conventional design thus requires very small implementation area and consumes less power over the conventional design. The simulation results illustrated in the next section shows the effectiveness of the proposed image scalar of the existing.

IV. Simulation results and analysis

The proposed and existing architectures of the sharpening filters are modeled on MATLAB to evaluate the quality metrics. These implemented designs on MATLAB are then simulated with standard test images [7] such as Lena and Baboon as shown in Fig. 9. The blurred images are first created by using inbuilt function. The images passing through Gaussian smoothing provides the burring. These blurred images are then filter using proposed and existing sharpening filter architectures. These filtered images are extracted and compared. On the other hand, to evaluate the design metrics designs are implemented and Verilog HDL and simulated on ModelSim EDA tool. Further, the functionality of the proposed design is rigorously verified on ModelSim. Finally, the design metrics such as area, power and delay are extracted for the proposed and existing designs and compared.

Fig. 2: Benchmark image

4.1 Quality and Design Metrics

Various quality and design parameters are used to evaluate the design. This subsection introduces the different quality parameters which are used in our design.

4.1.1 Mean Error (μ)

The mean error (μ) for an input image I and noisy output image K, is defined by the expression given below.

$$Mean(\mu) = \frac{1}{mn}\sum_{i=0}^{m-1}\sum_{j=0}^{n-1}[I(i,j) - k(i,j)] \quad (7)$$

Where, variables m and n represent the number of row and column of the image.

4.1.2 Mean Square Error (MSE)

In order to find out the error present in the output image, a most commonly used parameter called mean square error (MSE) is used. The MSE for an input image I and noisy output image K, is defined by the expression given below.

$$MSE = \frac{1}{mn}\sum_{i=0}^{m-1}\sum_{j=0}^{n-1}[I(i,j) - k(i,j)]^2 \quad (8)$$

Where, variables m and n represent the number of row and column of the image.

4.1.3 Peak Signal to Noise Ratio (PSNR)

The peak-signal-to-noise-ratio is the parameter used widely in image/video processing applications to quantify the amount of the noise present in the image and it is equal to the maximum signal power to the noise power. It is usually expressed in terms of decibel where signal and noise ratio is represented in logarithmic scale, as the signal can have wide dynamic range. For example in lossy image compression, the reconstructed images do not have the exact replica of the original image and therefore, there PSNR is generally used to represent amount of noise. The higher the value of the PSNR better the image is as it reflects higher value of desired contents over the undesired (noise). The mathematical expression that computes the PSNR in decibel is given by the equation below.

$$PSNR_{db} = 10.\log_{10}(\frac{Sig_I^2}{MSE}) \quad (9)$$

Where, Sig_I reflects the maximum signal value which for an image is 255.

4.2 Simulation results on MATLAB

To evaluate the efficacy of the proposed sharpening filter, the proposed sharpening filter and existing sharpening filters are implemented on the MATLAB and simulated with benchmark image such as Cameraman. The error metrics such as mean error, mean square error and PSNR are extracted for all these sharpening filter architectures by considering conventional sharpening filter as the reference filter. The quality metrics of the existing low complexity sharpening filter and proposed sharpening filter over the conventional are shown in Table 1.

Table 1: Error metrics comparison

Parameter	N-4	T-shaped	Prop.
Mean	1.8	1.8	2.1
MSE	14.2	14.2	18.8
PSNR (dB)	84.2	84.2	81.5

It can be observed from the Table 1, that neighbor-4 and T-shaped sharpening filter architecture provides same quality metrics as number of coefficients and their positions are same. Further the quality metrics of the proposed sharpening kernel is little poor over these technique as in the proposed technique two rows are eliminated which significantly reduce computational complexity. Finally, Fig. 3 compares the quality metrics for the proposed and existing filter architectures. Although, the quantitative metrics of the proposed filter are poor, the image output from the proposed filter will have the same quality and will be acceptable to all the image processing applications.

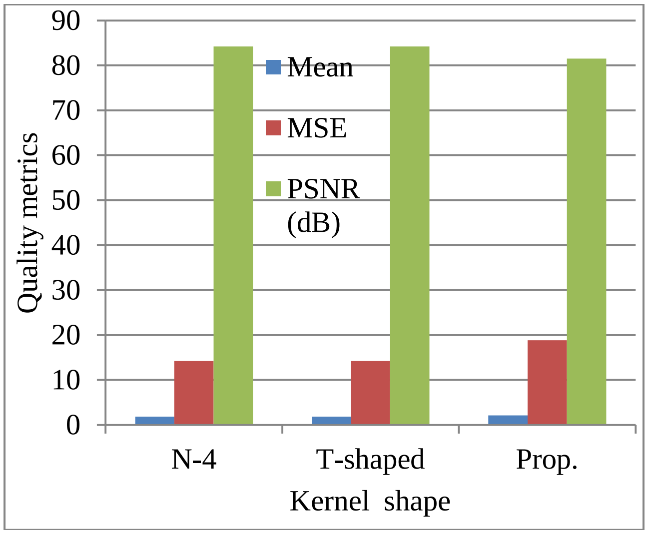

Fig. 3: Comparison of mean square error.

The filters are simulated with Cameraman image and the output sharpened images are shown in Fig. 4.

(a) Original Cameraman image

(b) Sharpened image via conventional sharpening filter

(c) Sharpened image via neighbor-4 (N-4) sharpening filter

(d) Sharpened image via T and inverse-T sharpening filter

(e) Sharpened image proposed sharpening filter

Fig. 4: Original and sharpened image via different sharpening filters

It can be observed from these images that proposed sharpening filter also provides sharpened image of good quality.

4.3 Simulation Results on FPGA

To compute the hardware results of the proposed sharpening filter, all the designs are implemented in Verilog and processed through Xilinx ISE tool chain. The designs are synthesized and are implemented in FPGA. The simulation results for the proposed and accurate sharpening filters are summarized in Table 2. The simulation results show that proposed sharpening filter requires very less area over the accurate design.

Table 2: Sharpening filter results on FPGA

Parameter	Filter architecture	
	Accurate	Proposed
Area (#LUTs)	1385	296
Max comb path delay	132.6	69.1

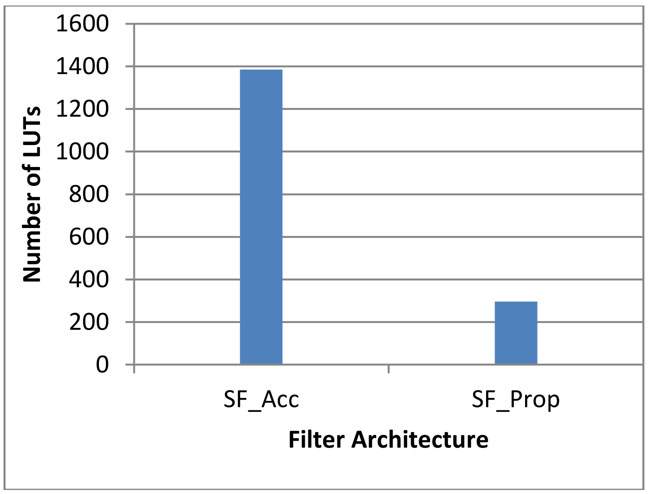

Figure 5: Area comparison of the filters.

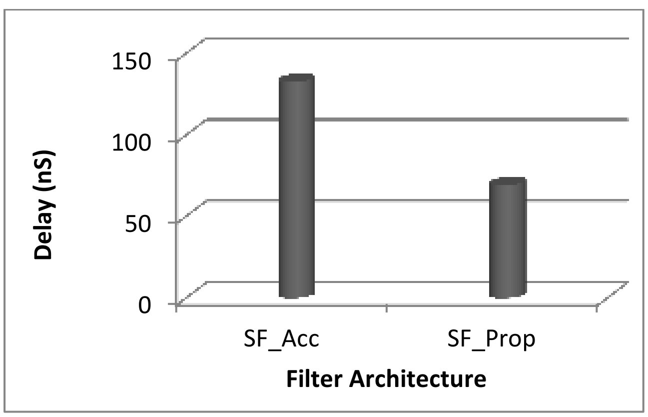

Figure 6: Delay comparison of different filters

V. CONCLUSION

New low complexity architecture for sharpening filter is proposed in this paper that provides higher performance without compromise in the quality. To evaluate the effectiveness of the proposed filter over the existing, all the existing image scalar architectures are implemented in MATLAB and Verilog. The designs on the MATLAB are simulated with benchmark input images and corresponding sharpened image and quality metrics are extracted. The designs implemented on the Verilogy are synthesized with Xiling tool chain and simulated with benchmark inputs. The simulation results on FPGA shows that the proposed filter requires **0.213X** area over the existing. Further the proposed filter shows **47.7%** improved performance over the conventional designs.

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